Low Complexity Reconfigurable Fast Filter Bank for Multi-Standard Wireless Receivers

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Abstract:

In this paper, we propose a new uniform filter bank (FB) based on the improved coefficient decimation method (ICDM). In the proposed FB's design, the ICDM is used to obtain different multi-band frequency responses using a single low pass prototype filter. The desired sub bands are individually obtained from these multi-band frequency responses by using low order frequency response masking filters and their corresponding ICDM output frequency responses. We show that the proposed FB is a very low complexity alternative to the other FBs in literature, especially the widely used discrete Fourier transform based FB (DFTFB) and the CDM based FB (CDFB). The proposed low-pass MFT-VDF offers unabridged control over the cutoff frequency on a wide frequency range thereby, improving the cutoff frequency range of existing VDFs. The design example shows that the RFFB is easy to design and offers substantial savings in gate counts over other filter banks.

1. INTRODUCTION:

A multi-standard wireless receiver (MSWR) enables different air interfaces to be implemented on a single generic hardware platformby replacing conventional analog signal processing with the digital signal processing. Operations such as spectrum sensing and channelization for MSWRs are usually performed using a filter bank. The filter bank must be dynamically reconfigurable with minimum hardware overhead to support multiple communication standards with different channel bandwidth and center frequency specifications. Moreover, the filter bank should be hardware-efficient in terms of area and power.

A number of different filter bank design approaches are available. The discrete Fourier transform filter bank (DFTFB) is an amplitude modulated filter bank that consists of a low-pass prototype filter followed by DFT operation and widely used for various communication applications. However, DFTFBs have the drawbacks of uniform sub-band bandwidth and fixed center frequency for each sub-band. An improved DFTFB using coefficient decimation method (CDM) has been proposed in which allows changing sub-band bandwidths using a fixed-coefficient filter at low reconfiguration overhead. However, it provides only coarse control over sub-band bandwidth because the decimation factor in the CDM is restricted to be integers. Also, center frequency of sub-bands in CDM-DFTFB is fixed. Low-complexity, reconfigurable filter banks based on frequency response masking and CDM for MSWRs are proposed. As the decimation and interpolation factors are limited to integer values, a fine control over the bandwidth is difficult to achieve using these filter banks.

The fast filter bank (FFB) is a low complexity alternative to DFTFB and is suitable for applications requiring sharp transition bandwidth (TBW). However, the FFB in has the same drawbacks as that of DFTFB, i.e., the inability to provide nonuniform bandwidth sub-bands and the constraint of fixed center frequency for each sub-band. Further extensions and improvements of FFBs have been suggested. In particular, multi resolution FFB provides coarse control over sub-band bandwidth by changing the filter bank resolution. However, all filter banks mentioned above fail to provide fine control over the bandwidth and center frequency of sub-bands.
In this brief, we propose a new approach of reconfigurable filterbank design by combining FFB and a variable digital filter (VDF). First, a modified second-order frequency transformation-based lowpass VDF (MFT-VDF) that offers wide cutoff frequency range than existing VDFs is proposed. Then, the proposed reconfigurable FFB (RFFB) is designed by replacing fixed-coefficient low-pass subfilter in the first stage of FFB with the MFT-VDF. The RFFB provides fine control over the sub-band bandwidth on the desired bandwidth range. This makes RFFB suitable for MSWRs where wideband input signal consists of channels of distinct bandwidths. The RFFB also offers fine control over the centre frequency of fixed bandwidth subbands. This unique property is useful where wideband input consists of channels of fixed bandwidth but dynamically varying locations.

2. RELATED WORK:
In [1] L. Pucker presents Channelization techniques for software defined radio. Digital Down Conversion, Frequency Domain Filtering, and Polyphone FFT Filter Banks. The analysis begins by presenting a base architecture for a wideband transceiver, and then explores each channelization method within the context of this architecture. These include the computational complexity of the channelization approach, the applicability of the approach in supporting a given frequency plan, and processor selection for the proposed implementation.
In [2] F. Sheikh and B. Bing, presents Cognitive spectrum sensing and detection using poly phase DFT filter banks. A computationally efficient, signal processing scheme to simultaneously sense and detect multiple active channels for a cognitive radio operating in licensed and unlicensed frequency bands. This new scheme employs a combination of prolate window filter and polyphase DFT filter bank (DFB). A frequency domain power detection scheme is deployed with polyphase DFB to detect multiple active channels based on the sensing output of the DFB.
In [3] R. Mahesh and A. P. Vinod presents Reconfigurable discrete Fourier transform filter banks for variable resolution spectrum sensing. A modified DFTFB is presented which can be reconfigured with minimal overhead to extract channels of different bandwidths and thus enables variable resolution spectrum sensing.
The proposed DFTFB consists of a prototype filter realized using the coefficient decimation technique for obtaining different passband widths. From the analysis of the architecture, it is clear that the reconfiguration overhead to obtain different sensing resolution is the proposed filter bank is only a few adders whereas reconfiguration of a conventional DFTFB involves reconfiguration of the prototype filter and DFT which is an expensive task.

3. TWO PARALLEL FIR FILTER:
We propose a new uniform filter bank based on the improved coefficient decimation method. The improved coefficient decimation method is used to obtain different multi-band frequency
responses using a single low pass prototype filter. We propose a new approach of reconfigurable filter bank design by combining FFB and a variable digital filter. The reconfigurable Fast filter bank provides fine control over the sub-band bandwidth on the desired bandwidth range. This makes reconfigurable Fast filter bank suitable for multi-standard wireless receivers where wideband input signal consists of channels of distinct bandwidths. Reconfigurable Fast filter bank also offers fine control over the center frequency of fixed bandwidth sub bands. This unique property is useful where wideband input consists of channels of fixed bandwidth but dynamically varying locations.

4.PROPOSED THREE-PARALLEL FIR FILTER:

A three-parallel FIR filter can also be written as below equation. shows implementation of the proposed three-parallel FIR filter. When the number of symmetric coefficients N is the multiple of 3, the proposed three-parallel FIR filter structure presented based on below equation and enables four sub filter blocks with symmetric coefficients in total, whereas the existing FFB parallel FIR filter structure has only two ones out of six sub filter blocks.

\[ Y_0 = \frac{1}{2} [(H_0 + H_1)(X_0 + X_1) + (H_0 - H_1)(X_0 - X_2)] + \frac{1}{2} [(H_0 + H_2)(X_0 + X_2) + (H_0 - H_2)(X_0 - X_2)] - \frac{1}{2} [(H_0 + H_1)(X_0 + X_1) + (H_0 - H_1)(X_0 - X_1)] + H_1X_1 \]

\[ Y_1 = \frac{1}{2} [(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_2)] + \frac{1}{2} [(H_0 + H_2)(X_0 + X_2) + (H_0 - H_2)(X_0 - X_2)] - \frac{1}{2} [(H_0 + H_1)(X_0 + X_1) + (H_0 - H_1)(X_0 - X_1)] + H_1X_1 \]

\[ Y_2 = \frac{1}{2} [(H_0 + H_2)(X_0 + X_2)] - (H_0 - H_2)(X_0 - X_2) + H_1X_1 \]

5.PROPOSED FILTER BANK DESIGN:

In MSWRs, the FB specification varies depending on the communication standards in operation at a specific time. In the conventional multi-standard FB channelizer reconfigurability is achieved by switching among different FBs, each designed for a particular standard. But this approach leads to inefficient resource utilization and increased hardware complexity. In this paper, we present a method to realize reconfigurable FB which will allow receivers to extract multiple radio channels of different BWs from the received wideband signal. An introductory idea of using the proposed FB for uniform and non-uniform channelization in MWCRs is discussed in and it is noted that parts of the material in this paper have been presented in the conference paper. However, in this paper, the idea discussed in has been extended by including the complete design details, actual implementation results on FPGA and comparison with other FBs.

6.DESIGN OF MODAL FILTER:

The first stage of the proposed FB architecture consists of a modal filter whose passband width can be changed using a suitable decimation factor D employing CD-II. The resultant filter is interpolated by a factor of
M resulting in an (M+1)-band filter response (i.e. \( H_a(z^{M/D}) \)) as shown in with a BW and TBW which is D/M times that of the BW and TBW of the modal filter frequency response. [4] Thus, the first stage provides variable BW subbands, whose design steps are as follows:

Step-1 Determine the minimum subband BW (B) and maximum TBW, TBW(filterbank)(max) of the FB taking into account of the specifications of multiple communication standards under consideration.

Step-2 The value of M decides the number of subbands in the FB and is fixed to a single value. The proposed FB is based on interpolation, CD to obtain multi-band response and frequency masking technique to extract each band. Two techniques namely coefficient decimation-I (CD-I) and coefficient decimation-II (CD-II) are proposed for the realization of reconfigurable FIR filters. In CD-I, every Dth coefficient of an FIR filter is kept unchanged and all other coefficients are replaced by zero to get multiband response with identical passband width and transition-band width (TBW) as that of the original filter. By changing the value of D, different number of frequency response replicas located at integer multiples of \( 2\pi/D \) can be obtained. This shows the frequency response of filter obtained using CD-I from the modal filter. In the proposed FB, the CD-I approach is used for the design of masking filters and is explained in detail.

In CD-II, every Dth coefficients of an FIR filter are grouped together discarding in between coefficients to obtain a decimated version of the original frequency response whose passband width and TBW are D times that of original filter. The frequency response of filter obtained using CD-II from the modal filter. In CD-II, stopband attenuation (SA) reduces as D increases. Hence, original modal filter should be designed with larger SA taking into account of the deterioration caused by decimation.

7. IMPROVED COEFFICIENT DECIMATION METHOD:

The combination of CDM-I and MCDM-I operations as improved coefficient decimation method I (ICDM-I), and the combination of CDM-II and MCDM-II operations as improved coefficient decimation method II (ICDM-II) respectively. Multiplexer for modal filter and complementary filter to produce different multiband frequency response. From them, multiband frequency responses obtained after ICDM-I operations, individual frequency bands with identical BWs can be isolated by the use of frequency response masking filters and spectral subtraction.

8. IMPLEMENTATION RESULTS:

A 16×16 bit multiplier, a 2:1 multiplexer, 16 bits of memory and 32 bit adder were synthesized on TSMC 0.18 μm process. The “synopsys design compiler” was used to estimate cell area. The area in terms of gate count is obtained by normalizing the cell area values by that of a two input NAND gate from the same library. The total estimated gate count in Table I is the sum of gate count of all the components.
9. CONCLUSION

An RFFB using a MFT-VDF was presented in this brief. The RFFB allowed fine control of the sub-band bandwidths and their center frequencies. The implementation results showed that the RFFB using VDFs required 99%, 42%, and 74% higher gate counts, respectively, when compared with the proposed RFFB using MFT-VDF. Possible future work includes the design of an area- and power-efficient two-stage spectrum sensing system. Here, the RFFB could be used to minimize dynamic power consumption by reducing the rate of activation of the second sensing stage.

REFERENCE