AN EFFICIENT PROPAGATION DELAY REDUCTION FOR NANOMETER CMOS IC

R. UMA, M.E VLSI design, Roever engineering college

Mr. S. Rajendra Prasad M.E MBA, Assistant professor of ece, Roever engineering college

Elambalur.

ABSTRACT

The design complexity of systems on chip drive the need to reuse legacy is used for gate level implementation needed. It’s used for design of 65 nm technology is tested in one of benchmark circuit C880 testing circuit. It’s used for analyze single path delay estimation in circuit. Its used for analyze multiple path delay estimation in the circuit. This delay path estimation is analyzed one of the benchmark circuit. Its tested under various multi path technology 65, 90, 135 nm technology

Index terms: C880, reuse legacy, 65nm, delay estimation, path finding algorithm

1. INTRODUCTION

Fast time-to-market satisfies industry designers to keep up with newly created standards, and configurability provides flexible hardware on demand of both standards without fabricating a new chip. The long-term reliability of nanometer integrated circuits can reach the noteworthy order of 103 FITs (failures in 109 hours). Some of the main challenges driving the design of reliable system (design for reliability) encompass soft error, process variation and device aging phenomena, with the continuous scaling of transistor dimension, device aging which cause the significant loss in the circuit and life time becoming increasing dominant for temporal reliability Concerns, therefore an early stage design optimization in this problem.

Traditional design methods add guard bands or adopt worst case margins to account for aging phenomena which in
refer to over design and may be expensive Conservative design, the mitigation of aging induced, Aging effects. Recent aging aware techniques basically follow this formulation. The proposed a gate sizing algorithm based on lagrangian relaxation. An Average of 8.7 % area penalty is required to ensure reliable operation for 10 years.

A Novel technology mapper considering signal probabilities NBTI was developed. The technique takes signal probabilities as one of the argument when searching for best matching in given standard cell library. On average 10% area recovery and 12 % power saving are accomplished as compared to the most pessimistic case assuming static NBTI an all PMOS transistors design .A Frame work using join logic restricting and pin reordering can mitigate NBTI induced performance

Traditional design methods add guard–bands or adopt worst case margins to account for aging phenomena, which in practice refer to over design and may be expensive .To avoid overly conservative design ,the mitigation of aging induced performance degradation problem is used for conservative design .The area minimization of problem with consideration of aging effect.

In some works, complex gates are converted to primitive gates prior to time analysis thus applying the test. Delay model is designed model to basic gates .This methodology may be a source of in accuracies since the circuit used for simulation has a topology that differs from the actual circuit structure being finally manufactured .Other works analyze the delay of complex gates through a transistor level approach or using a current source model, providing good accuracy at cost of very complex expression that result in a slow computation time at the circuit level or using current source model providing good accuracy at the cost of very accuracy.

The C88O is the one of the combinational digital circuitis used for analyze the number bench mark analysis the delay in the circuit. The delay is computed independently of specific input vector is used for path sensization scheme.Most of the paper analyze the delay in the bench mark circuit.
In this used for analyze the C880 propagation delay in the bench mark circuit, We analyze the impact of sensization input vector on the propagation delay for complex gates showing that delay variations may get up to 53% depending on the technology used. We provide an insight root causes variation through the careful transistor

2. COMPLEX GATES DELAY VARIATION

All complex logic cell have more than one vector input that sensitzes the propagation of each input and output. This paper only analyze the delay variation between each of one stage. We only consider the cases with steady values in all inputs except the input being propagated toward the output state.

.Circuit level analysis is used for fault in the circuit, The rest of the paper is used for analyze testing of bench mark circuit, path delay estimation in the bench mark circuit Section three explain the path delay estimation in the circuit the next section bench mark circuit

2.1 GATE-LEVEL ANALYSIS

Without loss of generality delay dependence with sensization input vector using four logic complex gates. All this process analyzed one of standard logic library cell the circuit. Four logic gates consider the input and its function out the two output.

Out = A * B + C * D (1)

Out = (A + B) * C

Fig 1: AA022

Fig 2: OA12
Table 1: Propagation table

2.2 Propagation Table

During the each phase the input is analyzed without consider the path delay in the circuit. May have significant impact on delay due to errornous in the circuit. Many logic gate function analyzed for different input and output. Truth table is analyzed for each vector propagation. The other two gates are the CB416 and the AO1212 (also known as A02ON and A010, respectively) their logic functions are given respectively given.

2.3 Circuit level relevancy

Multiple circuit level analysis is used for slowest path analysis; We take the C880 bench mark circuit at the circuit level. Its used for multiple sensation in the input side and compute the how many vectors at the input side. This bench mark circuit analyzed on of the commercial tool is 65 nm. This gates have the number of logical bench mark function. This is due to fact that technology libraries include many complex gates. This synthesis is used for reduce the area delay and power algorithm.

2.4 Transistor level analysis

To analyze the impact of multiple vector sensization at the circuit level, the slowest pathes of ISCA85 bench mark circuits and compute the how many paths in this circuit using CMOS technology. Its have multiple input gates and high lighting the relevancy that this phenomenon might have circuit level. This synthesis algorithm is used for reduce the area and delay in the circuit.
3. DELAY MODEL, HEURISTIC AND TOOL

A timing analysis tool that combines a specific delay model and algorithm to find the true paths in a combinational circuit. The delay model is analytical through a polynomial model is used to estimate both the gate propagation delay and the output transition time. Since latter is required to compute the propagation delay of the next gate with in path .The Second component of the timing analysis tool is the algorithm developed to find the true paths in Combinational circuit. Such an algorithm is based RESIST algorithm and was specifically consider the dependent delay between input and output complex vector counts.

3.1 Delay model

The delay model includes multiple variables like input transition time, output load, temperature and supply voltage and easily extended to accommodate additional variables. The analytical nature of the model provides some advantages over the widely used LUT (Look-Up Table) based approaches .The main advantages area faster computation time due to interpolations required by LUT methods and less memory space required to the model data.

The electrical simulations from which the model parameters are obtained are done systematically for a given technology library and consist of a set of iterative of values for each variable considered ,for which the propagation delay and output transition time for rising and falling input transition are between the stages of input and output vector monitoring. The maximum order each variable adjusted to during the extraction process to provide the desired accuracy in the estimation. An application to perform the whole process automatically determine the all sensization vectors for each gate input generating the
scripts for the iterative electrical simulation and finally extracting the model parameters from simulations.

In this work path finding algorithm that sensitizes the path while computing that its traversing through the circuit. The algorithm preserves as different paths those having the same course traversing the same sequence but using preserve sensization input and output circuit.

This algorithm starts at a circuit and advances node to node until an output is reached. If the node being analyzed has a fan out greater than 1 or the next gate has multiple sensitization vectors, the process state is saved. If a logic in compatibility is found, all the paths that sharing the current sub-path are discarded and the algorithm jumps to the last saved point. If no incompatibility is found, then the output node of the sensitized gate becomes the new current node and process is repeated.

To perform this logic propagation step efficiently the algorithm uses a logic system with semi-undetermined values that allow identifying a logic incompatibility before all implied nodes are set to an input. A of an AND2 gate with an undetermined value to the B inputs leads to a state that starts with an unknown logic value represent. This method leads to an increase in the algorithm speed to trace all true paths and avoids passing twice through the same paths. In this proposed system input vector monitoring using bench mark circuit C880. This algorithm is used to explore all possible input and output in the circuit. The input vectors for each path, unlike the commercial tool that only gives one input vector for each input vector each true path.

![Test circuit](image)

**Fig 5: Test circuit**
RESULTS

The simulation the delay variation due to the sensitization vector to the delay variation caused by other effects like process parameter fluctuation or the interconnect system. Such analysis is key to determine the relative significance of this phenomenon compared to other important delay variation sources. We carried this comparison for various combinational to estimate the circuit, C880 circuit level.

Fig 6: C880 testing circuit

CONCLUSION

The importance of considering the input vector used to sensitize a complex gate in the delay estimation. The delay variations up to 15 for a 65nm technology.
References


