A NOVEL DESIGN AND IMPLEMENTATION OF A SINGLE BIT LINE SRAM WITH INCREASE IN READ NOISE MARGIN WITH ADIABATIC CHANGE OF WORD LINE VOLTAGE

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Abstract - The rapid development in VLSI fabrication in recent years has led to reduced device geometries and increased transistor densities of integrated circuits and very high frequency operation. Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems for embedded multimedia and communication applications realized using system on a chip (SoC) technology. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules. SRAM (static random access memory) is high speed memory fabricated on a chip made from semiconductor material. A low power SRAM has many uses. It can be used as an embedded memory in processors or as a standalone SRAM integrated as an external memory during board design stage. The aim of this project is the Design and VLSI Implementation of a low power SRAM in time-wise change in DNM revealed that the read noise margin of this circuit was 1.9 times larger than that of a conventional two-BL circuit, according to the IEEE standards, including Longest Path Calculations, Schematic, Layout, Verification and Simulations, as well as Cost Analysis. The design constraints are memory speed, silicon area, power consumption, data retention, and economic constraints.

Index Terms – System on Chip, Read Noise Margin, Bit Line, Word Line

I. INTRODUCTION

A technique is to accurately estimate the stability of a conventional SRAM cell without modifying the cell structure. The main idea is to measure the specific cell’s currents with variant supply levels via the bit lines. The measured currents are used to estimate the read stability and the write ability through a nonlinear regression. A technique to accurately estimate the stability of a conventional SRAM cell without modifying the cell structure. The main idea is to measure the specific cell’s currents with variant supply levels via the bit lines. The measured currents are used to estimate the read stability and the write ability through a nonlinear regression. Low power memory is required today most priority with also high stability. The power is most important factor for today technology so the power reduction for one cell is vital role in memory design techniques. In this paper, we introduced some design circuit techniques for low power design. Leakage current in standby mode is the major part of power loss. We concentrate on the technique that to reduce the leakage current in standby mode. The one CMOS transistor leakage current due to various parameter is the vital role of power consumption.

The most research on the power consumption of 6T SRAM has been focused on the static power dissipation and the power dissipated by the leakage current. On the other hand, as the current VLSI technology scaled down, the sub-threshold current increases which further increases the power consumption. In this paper we have proposed 6T (8 X 8) SRAM cells using MCML technology which will reduce the leakage power.
in SRAM cell and will control the sub-threshold current.

II. CONCEPTS INCLUDE IN 6T SRAM CELL

Technology scaling has led to increasing challenges in designing higher density static random-access memory (SRAM). In the past few decades, although 6T-SRAM cells have been the most common cell architecture, they are increasingly limited due to inherent device variations. The increasing device fluctuation has made precise estimation of the SRAM-cell stability increasingly important. Conventionally, SRAM yield is predicted either by a static-read margin or a write-noise margin (WNM).

The SRAM yield based on these metrics can be rapidly estimated through stochastic simulation techniques such as response surface model or importance sampling. A few efforts address alternative stability metrics that introduce additional stability information. Although many papers are published for estimating the noise margins during design stage, most of these estimation techniques cannot be directly applied to in situ measurements of active SRAM cells. This paper suggests a technique to estimate the read stability and the write ability of 6T cells from peripheral measurements of the physical SRAM cells without changing the array structure.

Reducing computation energy is therefore a serious issue [3]. Particularly, the power consumed by SRAM circuits contributes dominantly to the total power consumption. Therefore, nanoscale SRAM circuits have been widely researched for low-energy operation. In such SRAM circuits, the threshold voltage $V_T$ varies very largely because the number of dopant atoms fluctuates statistically. This $V_T$ variation would make it impossible for a nanoscale SRAM to write and read data. To resolve the $V_T$ variation problem in an SRAM, Zhang et al. proposed that the voltage of the memory cell power line (MCPL) be decreased when writing.

A review on different adiabatic approach for the 8t SRAM cell is presented in this paper. In this paper, 8T SRAM cell to perform the write and read operations which employs a single bit line scheme. An SRAM is considering in the most development stage today, with its different variations as well as to support low power application [4]. Stability factor and Leakage power is becoming the most important factor on SRAM (Static Random Access Memory) cells. A novel 8T SRAM cell design is considering reducing the leakage and also reducing the stability issues as compare to 6T SRAM cell.

III. ADIABATIC TECHNIQUE – A BETTER PERFORMANCE IN SRAM

Adiabatic switching is a new approach for reducing power dissipation in digital logic. When adiabatic switching is used, the signal energies stored on circuit capacitances may be recycled instead of dissipated as heat. For energy recovery circuit, the ideal energy dissipation when a capacitance C is charged from 0 to $V_{dd}$ or discharged from $V_{dd}$ through a circuit of resistance R during time T is given by

$$E = \frac{(RC)}{T}(V_{dd})^2$$

(1)

When $T >> RC$, the power consumption is much smaller than the conventional CMOS circuit, for which an energy of $\frac{1}{2} C (V_{dd})^2$ is required during a charge or discharge cycle. If circuits can be made to operate in an adiabatic regime with consequently low energy dissipation, then the energy used to charge the capacitive signal nodes in a circuit may be recovered during discharge and stored for reuse. The efficiency of such a circuit is then limited only by the `adiabaticity’ of the energy transfers.

The term digital system includes the various systems from low level component to complete system over a chip and board –level design. Considering a digital system and its complexity it is not possible to understand such a complex system completely, so to make design of a system less complex and understandable VHDL is used. This paper describes the implementation of full adder using VHDL technology which meets less complexity requirement, it also shows how efficiently digital system i.e., Full Adder is implemented upt to layout level results shows technological map, RTL view, chip floor plan, chip layout, output waveforms showing Voltage Vs. Time relations and verification of truth table.

IV. EXISTING METHODOLOGIES

In a SRAM design and implementation using several ‘T’ in a circuit, the following techniques
were used to increase its result parameters. They are as follows:

- N-Curve technique
- Nonlinear regression technique
- Sub threshold technique

In N-Curve Technique, normally stability of the SRAM bit cell measured by the Static Noise Margin (SNM) and the Write Trip Point (WTP). N-Curve gets information about both read stability, write stability at one simulation process.

In Nonlinear regression technique, the main idea is to measure the specific cell’s currents with variant supply levels via the bit lines. The measured currents are used to estimate the read stability and the write ability through a nonlinear regression. The $R^2$ (coefficient of determination) of the stability estimation is as high as 0.95 when applied to an arbitrary data set. As typical stability definitions require an access to the internal node of a 6T-SRAM cell, alternative measurable stability metrics for read and write are surveyed and modified to improve the correlation with the conventional stability definition. With this alternative stability and the cell currents, the conversion rules from currents to the stability can be found from the measurement data.

In sub threshold technique, A design technique for (near) sub threshold operation that achieves ultra-low energy dissipation at throughputs of up to 100 MB/s suitable for digital consumer electronic applications.

**Fig. 1 Circuit structure of an Existing SRAM cell system during read failure test.**

Static noise margin (SNM) is a widely used term to quantify static logic’s stability in terms of the tolerable amount of dc noise voltage injected at the data storage nodes without changing the stored states. The figure 1 shows the circuit formation of earlier SRAM during read failure test. Read SNM (RSNM) and WNM are extended definitions of the SNM. These two terms are defined as the maximum tolerable noise that can be injected into the internal nodes of the SRAM cells without disturbing the intended operation.

**Fig. 2 Circuit structure of an Existing SRAM cell system during write failure test.**

Similar to the concept of RRV, the write ability of a cell can be expressed as the marginal voltage of the BWTV or the WWTV during the write operation. As they are strongly correlated, we focus on the BWTV. The BWTV is defined as the maximum tolerable voltage on the low bit-line side for the successful writing of the wanted data bit. If the BLB voltage is not fully low, the internal state of the 6T cell will resist against the forced state reversal by the write access. The maximum tolerable nonzero bit-line voltage effectively represents how easily the cell can change its state during the write access and how the cell is robust against noise injected at the low-side bit line. It has clearly analysed from the figure 2.

Similar to the SRRV measurement, the BWTV can be measured without the change of the cell layout. One of the bit lines storing “0” is tied to VDD, and other bit line storing “1” is swept from high to low.

Our approach employs i) architecture-level parallelism to compensate throughput degradation, ii) a configurable $V_t$ balancer to mitigate the mismatch of nMOS and pMOS transistors operating in sub/near threshold, and iii) a fingered-structured parallel transistor that exploits VT mismatch to improve current drivability.

**Fig. 3 Simulation steps for dynamic SRRV measurement**
The figure 3 shows an example of the pulsed read access with different cell supply levels. If the given cell is sufficiently stable at a high \( V_{\text{CELL}} \), the internal nodes will not flip during the access time (\( T_{\text{W}} \)), as shown in Fig. 4. Similarly, figure 5 shows a read failure when \( V_{\text{CELL}} \) is lowered and the cell becomes unstable. As is done for the static SRRV, the dynamic SRRV with a fixed \( T_{\text{W}} \) can be defined by the change in \( V_{\text{CELL}} \) required to flip the cell’s state. From the definition, the dynamic SRRV with infinitely long \( T_{\text{W}} \) is equivalent to the static SRRV.

V. PROPOSED TECHNIQUE

In the proposed system, the 6T SRAM with MCML circuit designed with the help of 9 transistors (4 PMOS, 5 NMOS transistors) is shown in figure 6. MCML gates behaving like differential and steer current between the two criticize resistances. Fig. 3 shows that PMOS transistor (M1, M2) works as resistors when supply voltage is zero. The NMOS transistor (M9) behaves like a current supply. The current source is an NMOS transistor with fixed ref2 (gate) working in saturation state. The load resistor behaves like PMOS devices with fixed gate voltage (ref1) and is created to be operator in the linear region in order to model resistors. The goal of NMOS differential pair is to switch the current provided by the current source from one side to the other. The current source for MCML circuits is designed with a single NMOS transistor.

We used the memory cell circuit layout in Fig. 6. C1 (C2 or C3) is a contact between metal 1 (2 or 3) to the diffusion layer. P (N) is the P (N)-diffusion area. G is the gate area (poly-Si). M1 (M2 or M3) is the metal 1 (2 or 3) area. In Fig 6, the MCPL and WL are set in the upper and lower side of the cell in the row direction, respectively. The GND and BL are set at the edge and center in the column direction, respectively.

The MCML technology is used for the following notable advantages.

- Differential circuit operation.
- Low voltage swing - suitable for high speed.
- Weak dependence of propagation delay on fan-out load capacitance (compared to CMOS)
- Robust performance and better noise immunity.

“Asynchronous SRAM” are available from 4 Kb to 64 Mb. The fast access time of SRAM makes asynchronous SRAM appropriate as main memory for small cache-less embedded processors used in everything from industrialelectronics and measurement systems to hard disks and networking equipment among many other applications.
A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices (as opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors. The principal drawback of using 4T SRAM is increased static power due to the constant current flow through one of the pull-down transistors. This has illustrated in the figure 7.

If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

Reading

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by precharging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and Q are transferred to the bit lines by leaving BL at its precharged value and discharging BL through M1 and M5 to a logical 0 (i.e. eventually discharging through the transistor M1 as it is turned on because the Q is logically set to 1). On the BL side, the transistors M4 and M6 pull the bit line toward VDD, a logical 1 (i.e. eventually being charged by the transistor M4 as it is turned on because Q is logically set to 0). If the content of the memory was a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then the BL and BL lines will have a small voltage difference between them while reaching a sense amplifier, which will sense which line has the higher voltage thus determining whether there was 1 stored or 0.

Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in.
Bus behaviour

RAM with an access time of 70 ns will output valid data within 70 ns from the time that the address lines are valid. But the data will remain for a hold time as well (5–10 ns). Rise and fall times also influence valid timeslots with approximately 5 ns. By reading the lower part of an address range bits in sequence (page cycle) one can read with significantly shorter access time (30 ns).

VI. CONCLUSION

To conclude that design a new SRAM with a small-capacitance BL that employs a shared read port and adiabatic WL charging for reading. Using the proposed circuit, an SRAM that consumes much less energy than a conventional one is possible. Next, we compared the RNM, speed, and energy consumption of the proposed circuit with those of a conventional SRAM. Also, there is no doubt and clearly to say the technology will improve to increase the speed and efficiency by means of increasing and process the transistor level.
VII. REFERENCES

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