HIGH SPEED AND LOW POWER MULTIPLIER DESIGN USING MTCMOS TECHNIQUE

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Abstract—MTCMOS is an effective circuit level technique which has multiple threshold voltages in order to optimize delay and power. Low threshold voltage MOSFETs enhance the speed performance, while the high threshold voltages MOSFETs minimize the static leakage power. The above technique is adopted in parallel multiplier with level shifter interface which gives supply voltage for MTCMOS transistors. By implementing 65-nm technology, the parallel multiplier shows on average propagation delay of 2.41ns and average power of 1.82mW. Using Tanner EDA Tool schematic simulation is done by S-edit, propagation delay is calculated by the W-edit and the power is calculated by the T-spice, layouts and 3D model are done by the Micro wind.

Keywords—MTCMOS, Level shifter, Parallel Multiplier

I. INTRODUCTION

Multipliers play an important role in today’s digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets—high speed, low power consumption, regularity of the layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation[1]. In parallel multipliers the number of partial products to be added is the main parameter that determines the performance of the (speed) multiplier. More number of partial products will consume maximum amount of power. Lowering the supply voltage is the most effective way to achieve low-power performance because power dissipation in digital CMOS circuits is approximately proportional to the square of the supply voltage [14]. To maximize the speed, we have to compensate the power and in order to improve the performance we choose the MTCMOS technique.

This paper deals with high speed and low power circuits designed by MTCMOS technique. MTCMOS technique has been emerged as a promising alternative to build logic circuits operating at a high speed with relatively low power dissipation when compared to traditional CMOS. Its unique feature is that it uses both low threshold and high threshold voltages in the same chip. Multiple supply voltage technique is popular in low power circuits. It is a circuit technique that exploits the difference in propagation delays along different delay paths by selecting threshold voltages. One of the most important methods to achieve multiple supply voltage is the level shifter. Level shifter operates in a wide range of supply voltages and it is based on the Differential cascade voltage switch (DCVS) topology for up conversion. This level Shifter is designed to interface two MTCMOS’s threshold voltages. MTCMOS technique and the level shifter are applied to the parallel multiplier to improve their performances [3]. Finally, the high speed, low power parallel multiplier and level shifter are designed based on 65nm CMOS technology. The rest of this brief is organized as follows: Section II describes the MTCMOS technique, level shifter and parallel multiplier. Section III presents the Simulation results and Discussion, Section IV concludes this brief.

II. MTCMOS TECHNOLOGY

A. MTCMOS Design

The scaling of CMOS technology in nanometre technology effectively reduces supply voltage and threshold voltage. Lowering of threshold voltage leads to an exponential increase in the sub-threshold leakage current. Multi threshold CMOS (MTCMOS) transistors have multiple threshold voltages in order to optimize delay or power. Low threshold voltage devices switch faster, therefore useful on the critical delay paths to minimize the clock periods but it has higher static leakage power. High threshold voltage devices are used on the non-critical paths to reduce the static leakage power without incurring a delay penalty [7]. Typical high threshold voltage can be assigned to some transistors on non-critical paths so as to reduce the leakage current 10 times when compared with low threshold devices.

Due to the complexity of logic circuits, not all the transistors on noncritical paths can be assigned a high threshold voltage; otherwise, the critical path may change, thereby increasing the critical path delay. The threshold voltage is selected based on the supply voltage, critical path delay, and noise considerations. [16] The design of the power switch which turns on and off the power supply to the logic gates is essential to low-voltage, high-speed circuit techniques such as MTCMOS. The speed, area, and power of a logic circuit are influenced by the characteristics of the power switch.
B. Level shifter using MTCMOS

Level shifter is the most important sub circuit for multi supply voltages and it is preferred to operate in the wide conversion range and it is hard to achieve up conversion from sub-threshold to the supply voltage. In some cases, some part of the circuit can operate at low voltages and other may operate higher than that, in that case there is a necessity for a level shifter. The level shifter should be an interface circuit to any module. During the voltage fluctuation, level shifter is used to convert the voltage drop to the required input which will perform actual operation of the circuit without any voltage drop.

The level shifter design is based on Differential Cascode voltage switch (DCVS) topology in which the NMOS diode current limiter reduces the current contention. Normally current limiting diodes are having very low reverse leakage current, so we are using NMOS transistor as current limiting diode by its gate is shorted with the drain of the same transistor. Fig.1 shows the DCVS Level shifter with NMOS diode current limiter. [8]

![Fig.1. NMOS diode current limiter Level shifter](image1)

In Fig.1 MTCMOS technique is shown clearly the setting of high threshold voltage to the pull up network to reduce the static leakage current (i.e.) pull up devices are active for more time due to high threshold voltage, so there is less leakage current at the supply voltage. The low threshold voltage is set to the pull down network to avoid critical path delay (i.e.) pull down devices switch faster due to low threshold voltage, so that the delay will be minimized. One of the inputs for DCVS is given directly and another is feed through the inverter at the low threshold transistor with low supply voltage.

Due to the current limiter performances pull up strength is weakened and the current contention is significantly mitigated. When the input X goes from low to high node N can be pulled to ground even though the weak strength of pull down device. The complementary level shifter part helps to ensure correct functioning of level shifter as a result the node N waveform is not full swing due to voltage drop across NMOS diode. By inverting the node N will get the full swing similar to high to low transition. The output inverter set high threshold transistor to avoid short circuit power dissipation. [8]

C. Parallel Multiplier with Level Shifter interface using MTCMOS technique

It is difficult to design parallel multiplier with minimum delay. The structure shown in Fig.2 contains mainly AND gate, half adder and full adder which reveal relationship between the array and basic multiply steps. [14]. When multiplying manually, partial products are found in rows and accumulated in columns, with the partial products shifted by the appropriate amount. Each partial product is formed by AND function and the partial products are all added together [3]. The carry from the adders will propagate along the second stage to the last stage of the multiplier. The last adder of the parallel multiplier has a carry chain. The earlier stages are performed by full adder which reduces three 1 bit -two 1 bit output. Only in the last stage all the values are accumulated with carries.

![Fig.2. Parallel Multiplier with critical path delay](image2)

The 4 bit A and 4 bit B are given as the input to the parallel multiplier. MTCMOS technique is adapted to the parallel multiplier to improve their performances. Fig.2 also shows the critical path of the circuit, that causes the maximum delay in the circuit which should be reduced by placing low threshold transistors on critical path and remaining block of the circuits are formed by regular threshold voltage transistors and high threshold voltage transistor which are set to the pull up devices to reduce the static leakage current.
Whenever a logic gate operating at a low voltage is driving a logic gate operating at a higher voltage, level shifter are required. Such a level shifter may not be required when a logic gate operating at a higher voltage drives logic operating at a lower voltage. A DCVS level shifter is used here to interface the two threshold voltages of MOSFET [16]. Supply voltage (Vdd) for critical path transistors are taken from level shifter’s input voltage 500mV (low Vdd) and supply voltage required for non critical path transistors choose the level shifter’s output voltage 1.2 V (high Vdd). [15]

III. SIMULATION RESULTS AND DISCUSSION

The NMOS-diode current limiter level shifter was implemented in a 65-nm technology. Fig.3 shows the waveform of the level shifter up-conversion from sub threshold to supply voltage with minimum delay using MT CMOS technique. Fig.4 shows the schematic view of the parallel multiplier, in that P7 be the last stage carry and also be the critical path. level shifter circuit gives their voltage value to the parallel multiplier and their output voltage levels are show in the Fig.5. In the Fig.5 level 1 is indicated as 21.4mV and the level 0 is indicated as 6.0mV and the layout views of the parallel multiplier are shown in Fig.6 which occupies 276.36 μm² silicon area.

In Fig.7 3D model of the Parallel multiplier is shown. This model shows how the chip could be designed before fabrication. The steps in the fabrication process are followed in the above model

Fig.3. Measured waveform of the level shifter with 500mV to 1.2V conversion

Fig.4. Schematic view of the Multiplier with level shifter of the parallel multiplier are shown in Fig.6 which occupies 276.36 μm² silicon area.

The Table I describe about the comparison of the proposed multiplier with the normal multipliers performance.

| TABLE I | MEASUREMENT COMPARISON |

Fig.5. Transient analysis of the multiplier

Fig.6. Layout view of the Multiplier

Fig.7. 3D model of the Multiplier
Multiple threshold voltage CMOS (MTCMOS) circuit technology has been used to achieve a high speed and low power parallel multiplier. Level shifter interfaces the parallel multiplier to set the two threshold voltages of the MTCMOS. It is mainly used for Digital and Analog Signal Processing applications. In addition to that proposed parallel multiplier shows an average propagation delay of 2.41ns, average power of 1.82mW occupying 276.36 μm² silicon area.

### References


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<table>
<thead>
<tr>
<th>Multiplier</th>
<th>Delay (ns)</th>
<th>Power(W)</th>
<th>Static power (W)</th>
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</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>3.32</td>
<td>0.62</td>
<td>2.64×10⁻⁷</td>
</tr>
<tr>
<td>MTCMOS</td>
<td>2.41</td>
<td>1.82m</td>
<td>6.774×10⁻⁸</td>
</tr>
</tbody>
</table>

$P_s = \sum \text{leakage current} \times \text{supply voltage}$

IV. CONCLUSION

Static power dissipation ($P_s$) is due to leakage current or other current drawn continuously from the power supply. Fig.5 and Fig.6 reveal that the MTCMOS technique circuit is superiority in terms of minimizing the delay and power consumption over the CMOS circuit.

![Fig.8. Power consumption with varying supply voltage](image_url)

![Fig.9. Delay with varying supply voltage](image_url)