FAT TREE BASED CROSSTALK ANALYSIS IN OPTICAL NETWORKS

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Abstract- Fat tree based Networks on chip (NoC) have the potential of higher bandwidth and efficient power consumption which is better suitable for electronic Networks on Chip. The key components of optical network on chips are optical devices which experience crosstalk noise and power loss that in turn reduces the network scalability. The 3D based Network on Chip (NoC) architectures represent a promising design paradigm to cope with increasing communication requirements in digital systems. 3D Network on chip (NoC) has emerged as a vital factor that determines the performance and power consumption of many core systems. A novel switching mechanism, called virtual circuit switching, is implemented with circuit switching and packet switching. A path allocation algorithm is used to determine high priority based adaptive circuit switching connections and circuit-switched connections on a Fat-Tree-connected 3D-NoC such that both communication latency and power are optimized. The goal of this paper is to investigate the runtime adaptation of the 3D-NoC resources, according to the QoS requirements of each application running in the MPSoC. This paper adopts an NoC architecture with duplicated physical channels, adaptive routing, support to flow priorities and simultaneous packet and circuit switching. This work is to analyse the destination position level for 3D-layer based hierarchal NOC structure and to select the path using circuit switching technique. This process is to optimize the overall 3D-NOC architecture complexity level and to reduce the path delay time and clock latency time compare to existing methodology.

Key words: Fat tree based Networks on chip, Electronic networks on Chip, Multiprocessor System on Chip.

I. INTRODUCTION

Future system-on-chip (SoC) architectures will consist of hundreds of processing and memory elements communicating at several gigabytes per second, and will be implemented in Nano scale technologies. Communication architecture will be a key determinant of the overall performance and power consumption of these architectures. Network-on-chip (NoC) has emerged as the dominant solution for the interconnection architecture design problems of SoC design in Nano scale technologies and the industry. This paper addresses the design of a NoC in the context of application specific SoC architecture. Application specific SoC design offers the opportunity for incorporating custom NoC architectures that are optimized for the target problem domain ,and do not necessarily conform to regular topologies such as mesh. Large-scale MPSoCs are mostly combinations of few subsystems. One IP core may only communicate with several cores in such a large system. Network partitioning (NP) decomposes a large system into several smaller subsystems in which highly communicating cores are grouped in the same partition. Based on this knowledge, NP may be done prior to the application mapping to narrow down the search space and to reduce the core mapping complexity. A good initial mapping can be loosely defined as one that increases the probability to reach near optimum mapping. With the integration of tens to possibly a hundred of cores on a chip, multiprocessor system-on-chips(MPSoCs) have been provided with tremendous opportunities for parallel execution .A key challenge of the parallel paradigm is the design of high performance on-chip network that can connect various IP blocks or tasks running on different cores. However, as the network sizes continue to grow, traditional NoC topologies such as mesh or concentrated mesh have been facing serious performance issues due to their inherent nature of hop-by-hop packet forwarding. Multiprocessor systems-on-chip(MPSoCs) in order to meet the requirements of real-time applications. The complexity of these SoCs is increasing and the communication medium is becoming a major issue of the MPSoC. Generally, integrating a network-on-chip (NoC) into the SoC provides an effective means to interconnect several processor elements (PEs) or intellectual properties (IP)(processors, memory controllers, etc.). The NoC medium features a high level of modularity, flexibility, and throughput. A NoC comprises routers and interconnections allowing communication between the PEs and/or IPs. The NoC
relies on data packet exchange. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm. Therefore, the path that a data packet is allowed to take in the network depends mainly on the adaptiveness permitted by the routing algorithm (partially or fully adaptive routing algorithm), which is applied locally in each router being crossed and to each data packet. To achieve a reconfigurable NoC, an efficient dynamic routing algorithm is required for the data packets.

In this paper, we present a new reliable dynamic NoC. The proposed NoC is a mesh structure of routers able to detect routing errors for adaptive routing based on the $XY$ algorithm. Our approach includes data packet error detection and correction. The originality of the proposed architecture is its ability to localize accurately error sources, allowing the throughput and network load of the NoC to be maintained. In our case study, we consider a reliable approach based on the adaptive routing module proximity algorithm. The considered routing algorithm is based on the adaptive turn model routing scheme and the well-known $XY$ algorithm. This adaptive algorithm is live lock and deadlock-free and allows data packets to pass around faulty regions.

II. RELATED WORK

In basic photonic devices many efforts have been proposed to lighten the crosstalk noise and power loss. Zhang et al. [2] this paper presented a waveguide crossing for Submicron silicon waveguides. Tsarev et al. [3] this paper demonstrated an efficient silicon wire waveguide crossing by means of vertical coupling of tapered Si wire with an upper polymer wide strip waveguide through a silica buffer 98% efficiency for through pass and 99.9% efficiency to provide for cross pass. Ding et al. [4] this paper presented a waveguide crossing mechanism based on impedance matched meta materials with large absolute values of negative refractive indexes and obtained a very low insertion loss and crosstalk noise. Xia et al. [5] this paper presented compact, photonic-wire-based coupled resonator optical waveguide structures, including up to 16 racetrack resonators on a silicon-on-insulator (SOI) substrate and indicated a drop port loss of less than 3 dB. In [6], this paper presented the same group presented ultra compact fifth-order ring resonator optical filters based on Submicron silicon photonic wires. Li et al. [7] this paper designed and fabricated a compact third-order coupled-resonator filter on the SOI platform with focused application for on-chip optical interconnects and obtained a drop port loss. Xie et al. [8] this paper demonstrated the worst-case crosstalk noise and SNR in mesh-based ONoCs using an optimized optical crossbar router. This introduces a novel compact optical router, called Crux, to outperform the SNR in ONoCs. In the same work, it was proved that the worst-case SNR link in mesh-based ONoCs is not the longest optical link, which suffers from the maximum power loss in the network. In [1] and [9], this paper proposed formal methods to analyze the worst-case signal power, crosstalk noise power, and SNR in arbitrary mesh-based and folded-torus based ONoCs. Chan et al. [10] described a methodology for modeling and analyzing optical interconnection networks at both the physical- and system level. In [11], Ding et al. this paper presented GLOW, a hybrid global router, to provide low power optoelectronic interconnect synthesis while considering thermal reliability and various physical design constraints such as optical power, delay and signal quality. Lin et al. [12] this paper developed an analytical model to characterize the crosstalk noise level in a micro ring-based optical interconnection network.

III. PROPOSED METHODOLOGY

3D many-core NoCs are emerging architectures for future high-performance single chips due to its integration of many processor cores and memories by stacking multiple layers. In such architecture, because processor cores and memories reside in different locations (center, corner, edge, etc.), memory accesses behave differently due to their different communication distances, and the performance (latency) gap of different memory accesses becomes larger as the network size is scaled up. This phenomenon may lead to very high latencies suffered from by some memory accesses, thus degrading the system performance. To achieve high performance, it is crucial to reduce the number of memory accesses with very high latencies. However, this should be done with care since shortening the latency of one memory access can worsen the latency of another as a result of shared network resources. Therefore, the goal should focus on narrowing the latency difference of memory accesses. FAT-TREE network process is to effectively connecting all edge to edge router section. This section is to control the 3-layer of network architecture.
A. Single router architecture:

The router architecture is used to store the input data bits and to maintain the data bits using the clock signal. The router architecture is a type of data storage and storage control process. The router section is used to maintain the signal energy level due to the long data transmission process.

B. 4*4 fat-tree network noc design:

To design the 4*4 router architecture and to apply the Fat-Tree topology connection between 4*4 NOC design. The 4*4 NOC design is to reduce the energy consumption level for inter and intra chip communication process. So we use the destination calculation for every router placement position in 4*4 NOC design. We develop a 3 layer NOC design and to implement the flow priority algorithm for 3 layer bidirectional communication. Our NOC design consists of 3D-layer based NOC architecture and to apply the ADAPTIVE CS algorithm for shortest path identification in top layer NOC design.

![Fat Tree Topology](image)

Fat tree is a complete binary tree. In this network number of links going down to its siblings is equal to the number of links going up to its parent in the upper level. Therefore, the links get “fatter” towards the top of the tree.

C. Adaptive circuit switching technique:

A given flow goes to HIGH priority or CS due to disturbing traffic in the NoC. This paper adopts watchdog timers, for each communicating pair, keeping the communication mode active for a given amount of time. This paper adopts an NoC architecture with duplicated physical channels, adaptive routing, support to flow priorities and simultaneous packet and circuit switching. This work is to analysis the destination position level for 3D-layer based hierarchal NOC structure and to select the path using circuit switching technique.

D. Neighbor router estimation:

The data transfer process is to analysis the all router position level and to find the shortest path between the source and destination router. So we check the low weighted bit level for nearest neighbor router estimation process. This process is to analysis the minimum router weighted bits. The neighbor router estimation control is used to check the shortest path identification control.

E. Qos scheme process:

The goal of this paper is to investigate the runtime adaptation of the 3D-NoC resources, according to the QoS requirements of each application running in the MPSoC. The QoS adaptation corresponds to change the communication flows priority or the switching mode of a given pair of communicating tasks. The change of priorities alters the physical channel used for communication (high or low), and explores the adaptability of the Hamiltonian routing algorithm (high priority flows are routed adaptively).

![Router Design](image)

Proposed method is to design a fat tree network topology based 4 * 4 NOC architecture using hop to hop router data transfer technique and this technique to reduce the path selection time. Proposed system is to implement the master and slave router condition for data transfer process and to optimize the path selection complexity level. This proposed architecture is to optimize the internal connectivity level and to reduce path allocation process level. This technique is to reduce data transfer time between source and destination.

IV. PERFORMANCE ANALYSIS

Xilinx tool has been used to evaluate the performance of proposed scheme. Xilinx is a tool that offers a broad range of development systems tool
collectively called the ISE Design Suite. The analysis is evaluated and it is implemented in VHDL. Xilinx ISE[1] (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize (“compile”) their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

Fig 4 Initial setup

Fig 5 Shortest path selection

Fig 6 Parallel searching

Table 1. Comparison of existing and proposed methodology

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXISTING SYSTEM</th>
<th>PROPOSED SYSTEM</th>
</tr>
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<tbody>
<tr>
<td>CLOCK DELAY TIME (ns)</td>
<td>5.115</td>
<td>1.268</td>
</tr>
<tr>
<td>SPEED (MHz)</td>
<td>195.90</td>
<td>792.205</td>
</tr>
<tr>
<td>POWER (mW)</td>
<td>70.23</td>
<td>18</td>
</tr>
<tr>
<td>LATENCY TIME (ns)</td>
<td>5.9</td>
<td>1.875</td>
</tr>
<tr>
<td>FLIP FLOP COUNT</td>
<td>647</td>
<td>156</td>
</tr>
<tr>
<td>SLICES COUNT</td>
<td>1040</td>
<td>204</td>
</tr>
</tbody>
</table>

Fig. 8 Power Result

Fig. 7 Final Destination

Power Report:

Fig.4 shows the initialization of input values where the parameters like reset, clock are initialized. After initialization of input, the analysis to find the shortest path to destination is performed as predicted in Fig.5. The path selection analysis is done using circuit switching algorithm. Fig.6 shows the way by which the path selection analysis is performed in parallel. Using this technique destination is
found out and the packet is routed through this chosen path as shown in fig.7. Table 1 represents the comparison between existing and proposed methodology in terms of delay, speed and power.

V. CONCLUSION

Finally a FAT-TREE network is designed based on 4*4 NOC architecture using adaptive circuit switching technique to increase the network performance. Finally, the proposed system consumes less power and reduces the circuit complexity level. This system reduces the latency level.

References