Design of High Speed ADC for Digital Communication: A Survey

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Abstract—Analog-to-Digital Converters (ADCs) are useful building blocks in many applications such as data storage, read channel and an optical receiver in digital communication because they represent the interface between the real world analog signal and the digital signal processors. The standard CMOS technology with low cost VLSI implementation can be used to design ADC with low optimal delay by using double edge triggered D-flip flops (DETDFF) which offers the combination of high accuracy and low-power consumption. ADC using scaled CMOS technology can be used in wireless applications and the implantable or portable bio-medical applications which are operated with limited amount of power in a battery.

Index Terms - ADC, DETDFF.

I. INTRODUCTION

With the development of digital communication, sensors, portable devices and high speed computing systems, comparable growth is seen in the optimization of Analog to digital converters (ADC) to assist in the technology growth. All the natural signals are analog and the present digital world require the signal in digital format for storing, processing and transmitting and thereby ADC becomes an integral part of almost all electronic devices. This leads to the need for power, area and speed optimized design of ADCs. There are different ADC architectures like Flash ADC, SAR ADC, sigma-delta ADC etc., with each having its own pros and cons. The designer selects the desired architecture according to the requirements.

In a recent survey article on data conversion, it was pointed out that the most popular type of analog-to-digital (A/D) converter in use today is the one employing the successive-approximation (SA) logic [8]. The main reason for its popularity lies in its inherently fast conversion time which is a constant n clock periods for an n-bit converter. When compared to other A/D schemes such as the dual-slope integrating method and the servo-type method, the successive-approximation scheme offers much higher conversion rates. Successive Approximation ADC is often considered as one of the most popular A/D conversion technique because it offers the combination of high accuracy and low-power consumption. Basically, the successive-approximation A/D converter consists of three main components: an analog comparator, a DAC, and a successive-approximation register (SAR) all of which are connected in a feedback arrangement shown in Fig. 1.

Fig.1. Successive Approximation A/D Converter.

In a conventional single edge-triggered (SET) flip- flop, data moves from input to output in synchrony with one edge of the clock. The use of double edge-triggered flip-flops has been already proposed for low-power circuit design. In a DET flip-flop, both rising and falling edges of the clock signal are used to transfer data from input to output. In this way, for a given throughput, the clock frequency can be halved with respect to a system using SET flip- flops, with a reduction of power consumption. Unfortunately, DET flip-flops require a more complex implementation with respect to SET flip flops. This results not only in larger silicon area but also requires higher number of internal nodes and transistors.

II. LITERATURE REVIEW

Amir Arian et al. presented process variation architectures developed by designing SAR ADC. Data converter SAR ADC architecture simulated on 1V, for 4 bit resolution in 0.18µm and 50nm having very low power consumption and high sampling frequency. This architecture can be used in on chip data converter in emerge digital systems, embedded microprocessor and for standalone ADC. It is observed that power consumption decrease as technology uses increases. [1]

For ultra-wide band applications a “Low power Flash ADC” is designed using CMOS 90nm technology. Flash ADC consists of a reference generator, array of comparators, 1-out- of N codegenerator, Fat tree encoder and output D latches. The demanding issues in the design of a low power flash ADC
is the design of low power latched comparator using 90nm technology at 0.8V DC voltage source using H SPICE tool. The Simulation results of a 6-bit flash ADC for a sampling frequency up to 1.2GHz showing an average power dissipation of 7.67mW. They designed a low power, high speed comparator by using three sections: a preamplifier stage, a decision circuit (latch) and a post amplifier stage. The pre-amplifier amplifies the difference between input voltage and the reference voltage generated by the resistive ladder of the ADC. The preamplifiers a circuit which is used to amplify the signal so that it can easily drive the load. Function of the latch in circuit is as an memory element, which is used to store the value. Latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. In the Post amplifier the amplifiers are self-biased, they are always ON by default. The working of the post amplifier depends on the working of the Latch. The back to back inverters used to remove the glitches present at the output of the buffer and also to provide an additional gain. Output of the post amplifier stage forms a thermometer code and this thermometer code is converted into a 1-out-of-N code generator. [2]

For data acquisition a Successive approximation analog to digital converter (ADC) designed using fully CMOS high speed self-biased comparator circuit. CADENCE virtuoso EDA tool in 180nm technology is used for the entire optimized design when area and speed optimization are major concern and here it was achieved. Author described the design of a fully customized 9 bit SAR ADC with input voltage ranging from 0 to 2.5V and sampling frequency 16.67 KHz. Successive approximation register and control logic divided into two stages: sequence generator and successive approximation registers. Sequence generator circuit implemented using positive edge triggered flip-flops of N+1 numbers and negative edge triggered flip-flops used for the successive approximation register. An EOC (end of conversion) signal goes high at the N+1th cycle and remains high till the next conversion starts. The sequence generator produce an output as that of a Johnson counter and successive approximation register stores the comparator output at each cycle according to the control logic. The output of SAR logic is the final ADC output and is same as the input to DAC and hence at the end of conversion, the output of DAC equals to the analog input voltage. Open loop self-biased comparator shows good resolution and conversion speed of operation. R-2R DAC architecture exhibits the performance comparable to an ideal DAC and has nearly zero INL and DNL. The overall power consumption of the circuit is 130mW. [3]

The converter is designed in CMOS 65nm technology with low power for array implementation in CMOS Imagers. New charge redistribution Successive Approximation A-D Converter (SA ADC) is presented. Sampling rate reached is more than sufficient for mobile applications (5Megapixels). The consumed silicon area was optimized in order to fit into the actual sensors die size with no major changes affected the other blocks, thus this new conversion system is readily usable in image sensors of next generation with pitches less than or equal to 1.1µm. The apparent resolution of the converter is 12-bits. It is obtained from a 9-bits converter, and it varies depending on the pixel noise value. For low resolution video rate applications, a single high speed ADC can be used. The ADC is shared by all pixels in the imager, and converts only one pixel at a time. This serial approach is no longer feasible in modern high resolution CMOS Image Sensor, as millions of pixels need to be converted all in a few milliseconds. Instead, a column-parallel approach is often employed, where an ADC is dedicated to each column (or a few columns) of pixels, and all ADCs operate in parallel. In this case, lowpower and low-to-medium speed ADCs can be used. The new converter is designed to process the data from 32 columns of the pixel array and the layout will be extended to 32 columns instead of 1 column. The proposed design provides a method of analog-to-digital conversion over 12-bits of an analog signal that includes comparing the amplitude of the analog signal with a threshold representing the amplitude of the full scale analogue signal divided by $2^3=8$ and then performing an analog-to-digital conversion by successive approximations of the analog signal over 9-bits to obtain. The 9 Most Significant Bits (MSB) of a binary word over 12-bits if the result of the comparison step indicates that the amplitude of the input signal is greater than the threshold. The 9 Least Significant Bits (LSB) of the 12-bits binary word otherwise. The choice of 3-bits for the coarse comparison is not random; it is based on the noise profile of CMOS Imagers. [4]

In the proposed SAR ADC design, register is made of double edge triggered D flip-flops (DETDF) connected in series. A single row of DETDF is used in each bit cell which functions both as sequencer and code register. These double-edge-triggered flip-flops (DET-FFs) have two major advantages. First, power dissipation is reduced. With the conventional SET-FF’s, one of the two clock transitions accomplishes nothing. However, this transition may cause changes in the output of some logic elements internal to the FF’s. In addition, extra energy is wasted to charge or discharge the capacitive load of the global clock line in a system using SET-FF’s. This is particularly true in CMOS where static power dissipation is small and the dynamic power dissipation is the main contributor of energy dissipation. Second, the speed of the system is accelerated. With both edges able to cause state transition, some redundant logic can be eliminated. Moreover, the clock period will be shortened because there is no need to wait for the clock signal to toggle up and down. This SARADC is designed in 0.18µM CMOS Technology with 4 bit resolution. It consumes 71.18uW of power. It rate of conversion is 25Ms/s. [5]

Sanjay G Talekar et al. presented the design and implementation details of a 4-bit time interleaved Successive approximation register (SAR) analog to digital converter (ADC) for UWB applications. The ADC implemented in 0.18µm CMOS technology and has total power consumption of 23.3mw at sampling frequency of 700MSPS for an input
swing of 1V peak to peak. In this work by detecting two bits per clock cycle low latency SAR ADC implemented. It uses only two capacitive DACs instead of three capacitive DACs. This is achieved by using Gilbert cell preamplifier in one of comparator detectors which reduces the power consumption by approximately 33%. In proposed ADC, input signal is distributed to individual ADCs. For N bit ADC, N/2 + 1 time interleaved ADC slices are required. Input signal is given to each of ADC slice (ADC-1, ADC-2, ADC-3) through time delayed signals. Operation of each of the ADC slices is started by the corresponding start signals. The start signals lag by one clock cycle compared to the corresponding signals. A multiplexer driven by an encoder is introduced to select the ADC slice from which the digital output has to be provided. [6]

For biomedical applications, a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) proposed. The proposed SARADC achieves rail–to–rail input range and low power consumption. The implantable or portable bio-medical applications are operated with limited amount of power in a battery. To guarantee long-life operation, it is important that the system should have low power consumption and hence, C-2C capacitor array and dynamic comparator used in Digital-to-Analog Converter (DAC) for low power consumption. In the proposed architecture DAC, comparator, S/H, SAR and clock control are used. The ADC is based on charge redistribution architecture in C-2C capacitor array. The proposed rail-to-rail comparator is n-type and p-type differential pairs are connected in parallel. These two types of comparator have different input common-mode range. To reduce the power consumption, the only one type of comparator operates in the proper input common-mode range. N-type comparator takes the high level of reference voltage, which is from middle of supply voltage to supply voltage. The P-type comparator takes the low level, which is from ground to middle of supply voltage. The enable switches are attached below the current source. The switches block the static current path and control the states of comparator. The unused comparator should be turned off during the operation. It is realized in 0.18μm standard CMOS technology. This ADC has signal to noise and distortion ratios (SNDR) of 53.8dB for 1.5V supply voltage. It consumes 13.4μW at sampling rates of 137ks/s. [7]

Mohamed O. Shaker et al. designed 6-bit flash Analog-to-Digital Converter (ADC) for a low power CMOS with maximum acquisition speed of 1 GHz, and implemented in a 1.2 V analog supply voltage. The results using H-Spice simulation for the proposed flash ADC shows that it consumes about 72 mW and minimized number of comparators in a commercial 90 nmCMOS process as compared with the traditional flash ADC. They designed flash ADC by using only 9 multiplexers and 10 comparators to generate the required binary code. In this design the input analog signals compared with half of the reference voltage(0.5 Vref) to generate the most significant bit. To generate the second most significant bit, reference voltages 0.75Vref and 0.25 Vref are used as inputs to amultiplexers controlled by most significant bit and the output is compared with the input analog signal. Here the most significant bit is high then the multiplexer passes 0.75 Vref otherwise passes 0.25 Vref. The proper fractions of the reference voltages are inputs to the multiplexer and multiplexer is controlled by the two most significant bits which passes the correct fraction which will be compared to the analog signal to generate the next most significant bit. Seven multiplexers which are connected to the inverting terminal of the comparators are controlled by the three most significant bits. These comparators have outputs that are encoded into appropriate values that represent the least significant bits. [9]

For improvement of 44% in the speed and 45% in the static leakage a new flip flop called double-edged triggered feedback flip-flop (DFF) is proposed. The Dynamic power consumption of DFF is reduced by node transitions occurred only when the inputs are different in two successive clocks. The double edge triggered flip-flops are used with lower clock frequency reduced power consumption as compared to other flip-flops. These two not only reduced power consumption as well as increases the speed. [10]

III. Conclusion

High performance ADC is essential in wide range of applications such as data acquisition, measurement, and digital communication system. In order to design one of good type of ADC, its parameter such as resolution, speed, area, power consumption, supply voltage etc. along with the key
parameters requirements must be compared with other proposed ADCs.

The techniques reviewed in this survey are applicable to design high speed ADC with low power consumption and SAR ADC using DETDFF which provides very low power consumption with high speed and high sampling frequency.

References


