A Power Quality Improved Voltage Controlled Adjustable Speed PMBLDC Motor Drive

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ABSTRACT—This paper is concerned with modelling of a Permanent Brushless DC motor (PMBLDCM) using a buck half-bridge DC-DC converter for feeding a conventional voltage source inverter (VSI). The DC-DC converter used is a single stage power factor correction (PFC) converter. The three-phase VSI is fed from dc link voltage. The speed of the PMBLDCM is controlled by the motor. Therefore the VSI operates on the commutation sequence of the motor. The proposed PMBLDCM is designed and modelled for a constant torque load through a 1.5kw, 1500rpm PMBLDC motor. The simulation of the proposed drive system is done.

Keywords—Modelling, PMBLDCM, voltage control, VSI.

1. INTRODUCTION

Brushless DC (BLDC) Motors can in many cases replace conventional DC Motors. Permanent Magnet Brushless DC (PMBLDC) motors are synchronous motors with permanent magnets on the rotor and armature windings on the stator. The most obvious advantage of the brushless configuration is the removal of the brushes, which eliminates brush maintenance and the sparking associated with them. Having the armature windings on the stator helps the conduction of heat from the windings. Because there are no windings on the rotor, electrical losses in the rotor are minimal. BLDC motors obtain life-long field excitation from permanent magnets mounted on the rotor surface. Advances in permanent magnet manufacturing and technology are primarily responsible for lowering the cost and increasing the applications of BLDC motors.

PMBLDC motors are also called as electronically commutated permanent magnet motors (ECPMs). The commutation of a BLDC motor is controlled electronically. To rotate the BLDC motor, the stator windings should be energized in a sequence [2]. It is important to know the rotor position in order to understand which winding will be energized following the energizing sequence. Rotor position is sensed using Hall Effect sensors embedded into the stator. Most of the BLDC motors have three Hall sensors embedded into the stator on the non-driving end of the motor. Whenever the rotor magnetic poles pass near the Hall sensors, they give a high or low signal, indicating the N or S pole is passing near the sensors. Based on the combination of these three Hall sensor signals, the exact sequence of commutation is determined [3].

Generally, The PMBLDCM drive, fed from a single-phase AC mains through a diode bridge rectifier (DBR) followed by a DC link capacitor, suffers from power quality (PQ) disturbances such as poor power factor (PF), increased Total Harmonic Distortion (THDi) of current at input AC mains and its high crest factor (CF). It is mainly due to uncontrolled charging of the DC line capacitor which results in a pulsed current waveform having a peak value higher than the amplitude of the fundamental input current at AC mains. Moreover, the PQ standards for low power equipment’s such as IEC 61000-3-2 [5]. Emphasize on low harmonic contents and near unity power factor current to be drawn from AC mains by these motors. Therefore, use of a power factor correction (PFC) topology amongst various available topologies [6-14] is almost inevitable for a PMBLDCM drive.

2. SINGLE-STAGE POWER FACTOR CORRECTION

To meet the requirements of the norms it is customary to add a power factor corrector ahead of the isolated dc/dc converter section of the switching power supply. Again another dc/dc converter is needed for output voltage regulation. Thus there are two converter is needed for single-phase active power factor correction for the requirement of high input power factor and tight output regulation. There are two approaches for single-phase active power factor correction:

(1) Two-stage approach
(2) Single-stage approach

Two-stage approach is commonly used approach in high power applications. In this approach, there are two independent power stages. The front-end PFC stage is usually a buck or boost or buck-boost (or fly back) converter. The dc/dc output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent PWM controller to tightly regulate the output voltage. The two-stage approach is a cost-effective approach in high power applications; its cost-effectiveness is diminished in
low-power applications due to the additional PFC power stage and control circuits.

A single-stage scheme combines the PFC circuit and dc/dc power conversion circuit into one stage. A number of single-stage circuits have been reported in recent years. The block diagram of single-stage approach, when Compared to the two-stage approach, the single approach uses only one switch and controller to shape the input current and to regulate the output voltage. Although for a single-stage PFC converter attenuation of input-current harmonics is not as good as for the two-stage approach. But it meets the requirements of IEC norms [5]. Again it is cost effective and compact with respect to two stage approach.

![Fig1 single-stage PFC](image1.png)

![Fig2 Two-stage PFC](image2.png)

Most of the existing systems use a boost converter for PFC as the front-end converter and an isolated DC-DC converter to produce desired output voltage constituting a two-stage PFC drive. The DC-DC converter used in the second stage is usually a fly back or forward converter for low power applications and a full-bridge converter for higher power applications.

However, these two stage PFC converters have high cost and complexity in implementing two separate switch-mode converters, therefore a single stage converter combining the PFC and voltage regulation at DC link is more in demand.

The single-stage PFC converters operate with only one controller to regulate the DC link voltage along with the power factor correction. The absence of a second controller has a greater impact on the performance of single-stage PFC converters and requires a design to operate over a much wider range of operating conditions. For the proposed voltage controlled drive, a half-bridge buck DC-DC converter is selected because of its high power handling capacity as compared to the single switch converters.

Moreover, it has switching losses comparable to the single switch converters as only one switch is in operation at any instant of time. It can be operated as a single-stage power factor corrected (PFC) converter when connected between the VSI and the DBR fed from single-phase AC mains, besides controlling the voltage at DC link for the desired speed. A detailed modeling and performance evaluation of the proposed system driven by a PMBLDC motor of 1.5 kW, 1500 rpm rating.

3. PROPOSED PMBLDC MOTOR DRIVE SCHEMATIC

The proposed PMBLDC motor speed control scheme controls reference voltage at DC link as an equivalent reference speed, thereby replaces the conventional control of the motor speed and a stator current involving various sensors for voltage and current signals. Moreover, the rotor position signals are used to generate the switching sequence for the VSI as an electronic commutator of the PMBLDC motor. Therefore, rotor-position information is required only at the commutation points, e.g., every 60°electrical in the three phase. The rotor position of PMBLDCM is sensed using Hall Effect position sensors and used to generate switching sequence for the VSI as shown in Table-I, the proposed speed adjustable PMBLDC motor drive scheme with embedded PFC buck converter has been shown in below fig3.

In the above shown figure the DC link voltage is controlled by a half-bridge buck DC-DC converter based on the duty ratio (D) of the converter. For a fast and effective control with reduced size of magnetic and filters, a high switching frequency is used; however, the switching frequency (fs) is limited by the switching device used, operating power level and switching losses of the device. Metal oxide field effect transistors (MOSFETs) are used as the switching device for high switching frequency in the proposed PFC converter. However, insulated gate bipolar transistors (IGBTs) are used in VSI Bridge feeding PMBLDCM, to reduce the switching stress, as it operates at lower frequency compared to PFC switches.
Fig 3 the proposed schematic of proposed PMBLDCM drive

The PFC control scheme uses a current control loop inside the speed control loop with current multiplier approach which operates in continuous conduction mode (CCM) with average current control. The control loop begins with the comparison of sensed DC link voltage with a voltage equivalent to the reference speed. The resultant voltage error is passed through a proportional-integral (PI) controller to give the modulating current signal. This signal is multiplied with a unit template of input AC voltage and compared with DC current sensed after the DBR. The resultant current error is amplified and compared with saw-tooth carrier wave of fixed frequency (fs) in unipolar scheme (as shown in Fig.4) to generate the PWM pulses for the half-bridge converter. For the current control of the PMBLDCM during step change of the reference voltage due to the change in the reference speed, a voltage gradient less than 800 V/s is introduced for the change of DC link voltage, which ensures the stator current of the PMBLDCM within the specified limits (i.e. double the rated current).

Fig 4 PWM control of the buck half-bridge converter.

TABLE-I
VSI switching signals based on the Hall Effect sensor signals

<table>
<thead>
<tr>
<th>Ha</th>
<th>Hb</th>
<th>Hc</th>
<th>Ea</th>
<th>Eb</th>
<th>Ec</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
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<td>0 0 1 0 -1 +1 0 0 0 1 1 0</td>
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<td>1 0 0 +1 0 -1 1 0 0 0 0 1</td>
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3.1 MATHEMATICAL MODEL OF THE PMBLDCM MOTOR

Modeling and simulation play an important role in the design of power electronics system. The classic design approach begins with an overall performance investigation of the system, under various circumstances through mathematical modeling.

\[ V_{an} = R_i a + P_{sa} + e_{an} \] \hspace{1cm} (1)

\[ V_{bn} = R_i b + P_{sb} + e_{bn} \] \hspace{1cm} (2)

\[ V_{cn} = R_i c + P_{sc} + e_{cn} \] \hspace{1cm} (3)

Where \( p \) is a differential operator (d/dt), \( i_a, i_b, i_c \) are three-phase currents, \( \lambda_a, \lambda_b, \lambda_c \) are flux linkages and ean, ebn, ecn are phase to neutral back emf of PMBLDCM, in respective phases, R is resistance of motor windings/phase. The flux linkages are represented as,

\[ \lambda_a = L_i a - M(i_b + i_c) \] \hspace{1cm} (4)

\[ \lambda_b = L_i b - M(i_a + i_c) \] \hspace{1cm} (5)

\[ \lambda_c = L_i c - M(i_b + i_a) \] \hspace{1cm} (6)

Where \( L \) is self-inductance/phases, M is mutual inductance of motor winding/phase. Since the PMBLDCM has no neutral connection, therefore,

\[ i_a + i_b + i_c = 0 \] \hspace{1cm} (7)

From Equations (14-21) the voltage between neutral terminal (n) and mid-point of the DC link (o) is given as,

\[ V_{no} = (V_{da} + V_{ko} + V_{co} - (e_{an} + e_{bn} + e_{cn})) / 3 \] \hspace{1cm} (8)

From Equations (18-21), the flux linkages are given as,

\[ \lambda_a = (L + M)i_{a}, \lambda_b = (L + M)i_{b}, \lambda_c = (L + M)i_{c} \] \hspace{1cm} (9)

From Equations (1-3 and 9), the current derivatives in generalized state space form is given as,

\[ p_{ix} = (V_{xm} - i_xR - e_{xm}) / (L + M) \] \hspace{1cm} (10)

Where x represents phase a, b or c.

The developed electromagnetic torque \( T_e \) in the PMBLDCM is given as,
\[ T_e = \left( e_{an} i_a + e_{bn} i_b + e_{cn} i_c \right) / \omega \]  \hspace{1cm} (11)

Where \( \omega \) is motor speed in rad/sec.

The back emf may be expressed as a function of rotor position (\( \theta \)) as,

\[ e_{xn} = k_b f_x(\theta) \omega \]  \hspace{1cm} (12)

Where \( x \) can be phase a, b or c and accordingly \( f(x) \) represents function of rotor position with a maximum value \( \pm 1 \), identical to trapezoidal induced emf given as

\[ f_a(\theta) = \begin{cases} 1 & \text{for } 0 < \theta < \frac{2\pi}{3} \\ \frac{6}{\pi} (\pi - \theta) - 1 & \text{for } \frac{2\pi}{3} < \theta < \pi \\ -1 & \text{for } \pi < \theta < \frac{5\pi}{3} \\ \frac{6}{\pi} (\theta - 2\pi) + 1 & \text{for } \frac{5\pi}{3} < \theta < 2\pi \end{cases} \]  \hspace{1cm} (13)

\[ f_a(\theta) = \begin{cases} 1 & \text{for } 0 < \theta < \frac{2\pi}{3} \\ \frac{6}{\pi} (\pi - \theta) - 1 & \text{for } \frac{2\pi}{3} < \theta < \pi \\ -1 & \text{for } \pi < \theta < \frac{5\pi}{3} \\ \frac{6}{\pi} (\theta - 2\pi) + 1 & \text{for } \frac{5\pi}{3} < \theta < 2\pi \end{cases} \]  \hspace{1cm} (13)

The functions \( f_b(\theta) \) and \( f_c(\theta) \) are similar to \( f_a(\theta) \) with a phase difference of 120\(^\circ\) and 240\(^\circ\) respectively.

The equations (15-33) represent the dynamic model of the PMBLDC motor.

The mechanical equation of motion in speed derivative form is given as

\[ P_\omega = \frac{(P/2)(T_e - P_L - B\omega)}{(J)} \]  \hspace{1cm} (18)

The derivative of the rotor position angle is given as

\[ P\theta = \omega \]  \hspace{1cm} (19)

Where \( P \) is no. poles, TL is load torque in Nm, \( J \) is moment of inertia in kg-m\(^2\) and B is friction coefficient in Nms/Rad. These equations (15-33) represent the dynamic model of the PMBLDC motor.

![Fig5 equivalent circuit of VSI fed PMBLDC drive](image)

3.2 DESIGN OF HALF BRIDGE CONVERTER BASED PMBLDCM DRIVE

The proposed PFC buck half-bridge converter is designed for a PMBLDCM drive with main considerations on PQ constraints at AC mains and allowable ripple in DC link voltage. The DC link voltage of the PFC converter is given as

\[ V_{dc} = 2 \left( \frac{N_2}{N_1} \right) V_{in} D \text{ and } N_2 = N_{21} = N_{22} \]  \hspace{1cm} (20)

Where \( N_1, N_21, N22 \) are number of turns in primary, secondary upper and lower windings of the high frequency (HF) isolation transformer, respectively.

\[ V_{in} = \frac{2\sqrt{2}V_s}{\pi} \]  \hspace{1cm} (21)

A ripple filter is designed to reduce the ripples introduced in the output voltage due to high switching frequency for constant of the buck half-bridge converter.

The inductance (\( L_0 \)) of the ripple filter restricts the inductor peak to peak ripple current (\( \Delta I_{Lo} \)) within specified value for the given switching frequency (fs), whereas, the capacitance (\( C_d \)) is calculated for a specified ripple in the output voltage (\( \Delta V_{Cd} \)).

The output filter inductor and capacitor are given as,

\[ L_0 = \left( 0.5 - D \right) V_{dc} / f_s \]  \hspace{1cm} (22)

\[ C_d = \left( 2 \omega_0 \Delta V_{Cd} \right) / L_0 \]  \hspace{1cm} (23)

The PFC converter is designed for a base DC link voltage of \( V_{dc} = 400 \) V at \( V_{in} = 198 \) V from \( V_s = 220 \) Vrms. The turn’s ratio of the high frequency transformer \( (N_2/N_1) \) is taken as 6:1 to maintain the desired DC link voltage at low input AC voltages typically at 170V. Other design data are \( f_s = 40 \) kHz, \( I_o = 4 \) A, \( \Delta V_{Cd} = 4 \) V (1% of \( V_{dc} \)), \( \Delta I_{Lo} = 0.8 \) A (20% of \( I_o \)). The design parameters are calculated as \( L_0=2.0 \) mH, \( C_d=1600 \) \( \mu \)F.

3.3 MODELLING OF PFC CONVERTER

The modeling of the PFC converter consists of the modeling of a speed controller, a reference current generator and a PWM controller as given below.

3.3.1 SPEED CONTROLLER

The speed controller, the prime component of this control scheme, is a proportional-integral (PI) controller which closely tracks the reference speed as an equivalent reference voltage. If at kth instant of time, \( V_{*dc}(k) \) is reference DC link voltage, \( V_{dc}(k) \) is sensed DC link voltage then the voltage error \( Ve(k) \) is calculated as

\[ Ve(k) = V_{*dc}(k) - V_{dc}(k) \]  \hspace{1cm} (24)

The PI controller gives desired control signal after processing this voltage error. The output of the controller \( I_c(k) \) at \( k^{th} \) instant is given as,

\[ I_c(k) = I_c(k-1) + k_p [V_e(k) - V_e(k-1)] + k_i V_e(k) \]  \hspace{1cm} (25)
Where $K_p$ and $K_i$ are the proportional and integral gains of the PI controller.

3.3.2 REFERENCE CURRENT GENERATOR

The reference input current of the PFC converter is denoted by $i_{d}^*$ and given as,

$$i_{d}^* = I_L(k)U_V$$

(26)

Where $u_V$ is the unit template of the voltage at input AC mains, calculated as,

$$u_V = \frac{V_a}{V_{sm}} ; V_a = |V_S| ; V_S = V_{sm}\sin\omega$$

(27)

Where $V_{sm}$ is the amplitude of the voltage and $\omega$ is frequency in rad/sec at AC mains.

3.3.3 PWM CONTROLLER

The reference input current of the buck half-bridge converter ($i_{d}^*$) is compared with its sensed current ($i_{dc}$) to generate the current error $\Delta i_{dc}=(i_{d}^* - i_{dc})$. This current error is amplified by gain $k_{dc}$ and compared with fixed frequency ($f_s$) saw-tooth carrier waveform $m(t)$ (as shown in Fig.2) in unipolar switching mode to get the switching signals for the MOSFETs of the PFC buck half-bridge converter as,

$$k_{dc}\Delta i_{dc} > M_a(t) \text{ then } S_A = 1$$

(28)

$$-k_{dc}\Delta i_{dc} > M_b(t) \text{ then } S_B = 1$$

(29)

Where $S_A, S_B$ are upper and lower switches of the half-bridge converter as shown in Fig. 2 and their values ‘1’ and ‘0’ represent ‘on’ and ‘off’ position of the respective MOSFET of the PFC converter.

4. PERFORMANCE EVALUATION OF PROPOSED PMBLDCM DRIVE

The performance of the proposed PFC drive is evaluated on the basis of various parameters such as total harmonic distortion (THDi), the crest factor (CF) of the current at input AC mains, displacement power factor (DPF), power factor (PF) and efficiency of the drive system ($\eta_{drive}$) at different speeds of the motor. Moreover, these parameters are also evaluated for variable input AC voltage at DC link voltage of 416 V which is equivalent to the rated speed (1500 rpm) of the PMBLDCM. The THD of AC mains current remains less than 5% along with nearly unity PF in wide range of speed as well as load as shown in Table-II. The performance of the proposed PMBLDCM drive in terms of various PQ parameters such as THDi, CF, DPF, and PF is summarized as

<table>
<thead>
<tr>
<th>Vdc (v)</th>
<th>THDi (%)</th>
<th>DPF</th>
<th>PF</th>
<th>CF</th>
<th>Efficiency of drive</th>
<th>Load (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>170</td>
<td>2.88</td>
<td>0.99</td>
<td>0.9995</td>
<td>1.41</td>
<td>84.9</td>
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<td>180</td>
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<td>0.9996</td>
<td>1.41</td>
<td>85.8</td>
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<tr>
<td>190</td>
<td>2.40</td>
<td>0.99</td>
<td>0.9996</td>
<td>1.41</td>
<td>86.3</td>
<td>33.3</td>
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<td>200</td>
<td>2.26</td>
<td>0.99</td>
<td>0.9997</td>
<td>1.41</td>
<td>87.2</td>
<td>40.0</td>
</tr>
<tr>
<td>210</td>
<td>2.07</td>
<td>0.99</td>
<td>0.9997</td>
<td>1.41</td>
<td>87.6</td>
<td>46.6</td>
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<td>220</td>
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<td>0.99</td>
<td>0.9997</td>
<td>1.41</td>
<td>88.1</td>
<td>53.3</td>
</tr>
<tr>
<td>230</td>
<td>2.07</td>
<td>0.99</td>
<td>0.9998</td>
<td>1.41</td>
<td>88.2</td>
<td>60.0</td>
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<tr>
<td>240</td>
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<td>0.9998</td>
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<td>250</td>
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<tr>
<td>270</td>
<td>2.01</td>
<td>1.00</td>
<td>0.9998</td>
<td>1.41</td>
<td>89.0</td>
<td>86.6</td>
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From the above table it is observed that the efficiency of drive system is improved for a wide range of speed.

5. OUTPUT WAVEFORMS FOR THE CORRESPONDING PROPOSED DRIVE SYSTEM

Fig 6 shows the performance of the proposed PMBLDCM drive fed from 220 V AC
mains during starting at rated torque and 900 rpm speed. A rate limiter of 800 V/s is introduced in the reference voltage to limit the starting current of the motor as well as the charging current of the DC link capacitor. The PI controller closely tracks the reference speed so that the motor attains reference speed smoothly within 0.35 sec while keeping the stator current within the desired limits i.e. double the rated value. The current (is) waveform at input AC mains is in phase with the supply voltage (vs) demonstrating nearly unity power factor during the starting.

Fig 6: PMBLDCM drive under starting condition

Fig 7: PMBLDCM drive under speed variation from 900 rpm to 1500 rpm.

Figs.6-7 show the performance of the drive during the speed control of the at 220VAC input. The reference speed is changed from 900 rpm to 1500 rpm for the rated load. It is observed that the speed control is fast and smooth in either direction i.e. acceleration or retardation with power factor maintained at nearly unity value. The speed control of the PMBLDCM driven compressor under steady state condition is carried out for rated speeds and the results are shown in Table-II to demonstrate the effectiveness of the proposed drive in wide speed range.

Fig 8: Performance of the PMBLDCM drive at 1500 rpm

Fig 9 shows (under steady state condition at 220 VAC input) voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the PMBLDC motor for phase „a” (Ia), and shaft power output (Po) at 1500 rpm speeds.

The performance of the proposed PMBLDCM drive in terms of various PQ parameters such as THDi, CF, DPF, PF is summarized in Table-II and shown in Figs. 9-10. Nearly unity power factor (PF) and reduced THD of AC mains current are observed in wide speed range of the PMBLDCM as shown in Figs. 9a-b.

Fig 9a: DC link voltage with speed
Fig 9b: Efficiency with load
Fig 9: Performance of the proposed drive under speed control at rated torque and 220VAC
6. CONCLUSION

A new speed control strategy of a PMBLDC drive is validated for constant load torque. The reference speed set by the dc link voltage, therefore speed control is directly proportional to the voltage control at DC link. The proposed additional PFC increases the efficiency of the drive. It also ensures to maintain nearly unity power factor. The power quality performance factors such as crest factor(CF), total harmonic distortion (THD) are maintained as per International standard IEC61000-3-2. The proposed drive has been found as a most promising drive for a variable speed 1-2kW power range. The bridge converter is selected for PFC amongst many DC-DC converter topologies due to its features like high voltage conversion ratio, continuous input current and low input current ripple.

APPENDIX

Rated Power: 1.5 kW, rated speed: 1500 rpm, rated current: 4.0 A, rated torque: 9.55 Nm, number of poles: 4, stator resistance (R): 2.8 Ω/ph., inductance (L+M): 5.21 mH/ph., back EMF constant (Kb): 0.615 Vsec/rad, inertia (J): 0.013 Kg-m2, Source impedance (Zs): 0.03 pu, switching frequency of PFC switch (fs) = 40 kHz, capacitors (C1= C2): 15nF, PI speed controller gains (Kp): 0.145, (Ki): 1.45.

REFERENCES