Classifying the Histology Image of Uterine Cervical Cancer

Vengatesan R
PG student
Department of Electrical and Electronics Engineering
Regional Office Anna University
Tirunelveli, India

Mrs. Vinolia Anandan
Assistant Professor
Department of Computer Applications
Regional Office Anna University
Tirunelveli, India

Abstract—This paper presents an image segmentation method for the manual identification of squamous epithelium from cervical cancer images. The present study was utilizing the various feature extraction techniques including texture feature, triangle feature and profile based correlation features. Generated features are used to classify the squamous epithelium into normal, Cervical Intraepithelial Neoplasia (CIN1), CIN2 and CIN3. The results are used to classify the images into: 1) normal, 2) pre-cancer. The final system will take as input a biopsy image of the cervix containing the epithelium layer and provide the classification using our approach, to assist the pathologist in cervical cancer diagnosis.

Keywords—Histology, Cervical Intraepithelial Neoplasia, Human Papillomavirus.

I. INTRODUCTION

Cervical cancer is the second highest cause of cancer death among women in the world. Every year 400,000 new cases of invasive cervical cancer in the world. The neoplasia is closely related to chronic infection by anogenital types of Human Papillomavirus (HPV)[2]. The most important risk factor of cervical cancer is infection by the HPV. HPV is a group of more than 150 related viruses, some of which cause a type of growth called papillomas. HPV can be spread from one person to another during skin to skin contact [3].

Cervical cancer starts in the cells lining the cervix the lower part of the uterus. This is sometimes called the uterine cervix. The cervix connects the body of the uterus to the vagina. The part of the cervix closest to the body of the uterus is called the endocervix. The part next to the vagina is the exocervix. The two main types of cells covering the cervix are squamous cells (on the exocervix) and glandular cells (on the endocervix). These two cell types meet at a place called the transformation zone. Most cervical cancer begins in the cells in the transformation zone. These cells do not suddenly change into cancer instead; the normal cells of the cervix first gradually develop pre-cancerous changes that turn into cancer. Doctors use several terms to describe these pre-cancer changes, including CIN, Squamous Intraepithelial Lesion (SIL), and dysplasia. This change can be detected by the pap test [4].

CIN increases in severity, the epithelium has been observed to show an increase in atypical immature cells from bottom to top of the epithelium for example as shown in Fig. 1, atypical immature cells are seen mostly in the bottom third of the epithelium for CIN 1 (Fig. 1b) while those for CIN2 lie in the bottom two thirds of the epithelium (Fig. 1c), In CIN 3, the atypical immature cells comprise the full thickness of the epithelium (Fig. 1d) [1].

II. LITERATURE REVIEW

Texture analysis of the nuclei structure is very important for classification of cervical cancer histology. In this paper a two tier classification strategy using Gabor filter banks for local classification and abnormality spread for global taxonomy was presented. In the algorithm developed in this work, a texture Classification method using Gabor filter banks is implemented to segment the image into five possible regions: of background, normal, abnormal, basal and stroma cells [4].
The boundaries are further fine-tuned at a higher (20X) resolution. The block-based segmentation method uses robust texture feature vectors in combination with Support Vector Machines (SVMs) to perform classification. Medical rules are finally applied. In testing, segmentation using 31 digital slides achieves 94.25% accuracy. For the diagnosis of CIN, changes in nuclei structure and morphology along lines perpendicular to the main axis of the squamous epithelium are quantified and classified. Using multi-category SVM, perpendicular lines are classified into Normal, CIN1, CIN2, and CIN3 [5].

III. DATA COLLECTION

The cervical biopsy images were collected from the cancerresearchuk.org web resource. The images are classified as abnormal and pre-cancer. The pre-cancer images are divided into: Cervical Intraepithelial Neoplasia (CIN) 1, CIN 2 and CIN 3.

IV. METHODOLOGY AND RESULTS

A. CIN grade classifications

The overall processes involved in the Cervical Intraepithelial Neoplasia grade image classification are outlined in the flowchart shown in figure 2 as follows.

Step 1: Manually segmented epithelium region.
Step 2: Vertical segmentation creations.
Step 3: Feature extractions.
Step 4: Classifications.

![Fig 1 Overall CIN grade classifications](image)

B. Manually segmented epithelium region

Use roiopoly to specify a polygonal region of interest (ROI) within an image. When active the pointer changes to + cross, Then move the pointer over the image in the figure. Using the mouse, by specifying the region by selecting vertices of the polygon then finished positioning and sizing the polygon, create the mask by double click. Roiopoly returns the mask as a binary image ‘BW’ the same size as image. In the mask image, roiopoly sets pixels inside the region to 1 and pixels outside the region 0 shown in fig 2.

![Fig 2 Specify the epithelium region by selecting vertices of the polygon](image)

Created a binary mask of the segmented epithelium region shown in fig 3.

![Fig 3 segmented epithelium region](image)

Bounding box specifies the minimum row and maximum row values for each dimensions shown in fig 4.

![Fig 4 Bounding box image](image)

Euclidean distance transform applied for the inverted binary mask. The Distance transform image measure highest intensity pixels shown in fig 5.

![Fig 5 Distance transform image](image)
C. Vertical segmentation creations

Segmented epithelium region divided into 10 equidistant segments shown in fig 6. Least squares regression implies that the ideal fitting of the regression line is achieved by minimizing the sum of squares of the distance between the straight line and all points.

D. Feature extraction

For each vertical segments image, three different types of features are computed, including: (1) texture features, (2) triangle features, and (3) profile based correlation features.

E. Texture features

Texture feature analysis refers to the characterization of region in an image by their texture content. Some of the most commonly used texture measures are derived from the Gray Level Co−occurrence Matrix (GLCM) function to extract feature information (e.g. contrast, correlation, energy, and homogeneity) [1].

F. Triangle feature

Create a Delaunay triangulation from a set of points. The points can be specified as an mpts by ndim matrix X, where ‘mpts’ is the number of points and ‘ndim’ is the dimension space where the points reside, ndim >= 2. Delaunay functions to extract feature information (e.g. average area of the triangle, standard deviation of this area, average distance between the edge of the triangle, and standard deviation of this distance) [1].

G. Profile based correlation features

Profile based correlation features have been computed for dermatology skin lesion discrimination by correlating the luminance histogram for skin lesion images with a set Weighted Density Distribution (WDD) basis functions [1].
Profile – based correlation features using the following four variations of the Profile Samples (PS).

\[
\begin{align*}
PS &= \{PS(1), PS(2), \ldots, PS(\text{H})\} \\
PS &= \{PS(1), PS(2), \ldots, PS(\text{H}/3)\} \\
PS &= \{PS(\text{H}/3 +1), PS(\text{H}/3 +2)\} \\
PS &= \{PS(2\text{H}/3 +1), PS(2\text{H}/3 +2)\}
\end{align*}
\]

As shown above, each 1/3rd of the profile (top to bottom) was analyzed separately along with the whole profile to extract profile based correlation features for each 1/3rd of the vertical segment image.

Table 3 profile based correlation features

<table>
<thead>
<tr>
<th>Property</th>
<th>Description</th>
<th>values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weighted density distribution</td>
<td>Correlation of profile of the segment and WDD function</td>
<td>0.0004</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0023</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0046</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0024</td>
</tr>
</tbody>
</table>

H. Classification

The Linear Discriminant Analysis method optimizes a linear transformation operator which depends on the ratio of the inter-class variance to the intra-class variance.

Table 4 Classification Grades

<table>
<thead>
<tr>
<th></th>
<th>Normal</th>
<th>CIN1</th>
<th>CIN2</th>
<th>CIN3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CIN1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CIN2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CIN3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

V. CONCLUSION

A framework for automated CIN grade classification of segmented epithelium regions was created which includes vertical segments using the manually segmented epithelium region, individual vertical segment feature extraction, and vertical segment classification. This method is utilized to classify the cervical cancer image into normal CIN1, CIN2 and CIN3. It aims to help the pathologist or technician to diagnose the cervical tissue slide.

VI. Acknowledgement

The authors wish to express sincere thanks to Dr. G. Sakhthinathan, Dean, Regional Office of Anna University, Tirunelveli for providing all necessary institutional support.

Reference

Grid connected high voltage gain DC-DC Boost Converter

Sunita Kumari, K. Mohanraj, Sanjit Singh.
Department of Electrical and Electronics Engineering, SRM University, Tamil Nadu, India

Abstract: Owing to the inexhaustible nature of solar power, more and more emphasis is on the use of solar energy, making PV arrays widely used. But there exists a mismatch between voltage level’s of parallel connected PV arrays and the grid voltage, making synchronization of PV with grid a bit complex. A three level DC-DC boost converter with a high voltage gain is presented in this paper. The converter is based on single phase, three level diode clamped inverter type topology. One of the advantages of the proposed converter is that high voltage gain is achieved without the use of transformer. Secondly, the proposed converter uses less number of components, also no transformer is required. It uses one inductor, two capacitors in series, and power switches and diodes, hence reducing cost. Pulse width modulation (PWM) control scheme is obtained according to the switching functions about the output pulse voltages of both half-bridges. Duty cycle is chosen close to 0.5, so as to get optimum result. Also, one more point is that the voltage across capacitor is balanced in both series and dynamic state. The proposed converter gives an efficiency of 92%, and the simulation results are presented to verify the feasibility of the proposed converter. Also, the output at different voltage gains is presented, and PWM scheme is validated and verified.

Keywords- Photovoltaic cell, Pulse Width Modulation, boost converter, diode clamped inverter.

1. INTRODUCTION

Both photovoltaic (PV) and wind power generations have become important parts of renewable energy sources, due to worldwide exhausted fossil fuel and world’s demand for clean energy [1],[2]. Photovoltaic (PV) source is one of the significant players in the world’s energy portfolio, and it will make one of the biggest contributions to electricity generation among all the renewable energy candidates by 2040, because it is a clean, emission-free, and renewable electrical generation source with high reliability.

Photovoltaic (PV) is a fast growing segment among renewable energy (RE) systems, whose is owed to depleting fossil fuel and climate-changing environmental pollution, PV power output capacity, however, is still low and the associated costs still high, so efforts continue to develop PV converters and its controller, aiming for higher power-extracting efficiency and cost effectiveness.

The PV grid-connected power system in the residential applications is recently becoming a fast growing segment in Europe, Japan, and the U.S. Unfortunately, the output voltage of the PV arrays is relatively low. In order to satisfy the high bus voltage requirements for the full-bridge, half-bridge, or multilevel grid inverters, the PV series-connected configuration is the conventional solution. However, the generated output power of the PV arrays is decreased greatly due to module mismatch and partial shading, especially in the urban areas. The grid-connected PV power system employing the cascaded H-bridge multilevel inverters or other multilevel configurations is introduced to optimize the PV output power.

2. DC-DC BOOST CONVERTER

In step up converter output voltage is greater than input voltage magnitude [3], so this topology can be used to connect low module voltages to high voltage load/battery. As duty cycle lies between [0, 1], a boost converter can’t reflect impedance greater than load impedance, and therefore does not achieve values near a module’s open-circuit Voltage [4], i.e., boost converter operates only if $R_{\text{load}} \leq R_{\text{mpp}}$

![Fig 1.Operational and non-operational region of I–V curve for Boost DC–DC converters](image-url)

Advantages of using a DC-DC Converter:
- High step-up voltage gain. Generally, about a ten fold step-up gain is required
- High efficiency
- No isolation is required
- Ripple reductions [5]
- Small filter components
- Cheaper implementation
- Better dynamic response
Cascaded boost converters are also used to extend the voltage gain and duty cycles [6], but one obvious disadvantage is that more separated inductors are demanded, and the power switch of the last power stage cannot avoid the output voltage stress. In recent years, many researchers have focused on step-up converters with coupled inductor, which has the transformer function to extend the voltage gain and duty cycles [7]–[9]. Some dc–dc converters provide high voltage gain, but with the penalty of either an extreme duty ratio or a large amount of circulating current.

DC–DC converters with coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors. Converters with active clamps recycle the leakage energy at the price of increasing topology complexity.

As to the parallel-connected PV configuration, one of the most important problems is that the low dc–bus voltage has to be boosted with high step-up gain. Therefore, high-step-up dc–dc converters are introduced to fulfill the voltage conversion between low-voltage parallel-connected PV arrays and the demanded high-voltage grid-connected side [10], as well as the maximum power point tracking (MPPT). When converters operate with high step-up gains, the power switches in conventional boost two-level converters would sustain high output voltage completely. While the classical boost three-level converters shown in Fig. 2(c) could reduce half of the voltage stress, but the extreme duty cycles of power switches limit its voltage gain and switching frequency because of the shorter turn–OFF time of the power switches in each switching period.

The three level (TL) inverter is also called NPC (neutral-point-clamped) inverter. The output voltage of the NPC inverter has lower harmonics as compared to that of traditional inverters. This allows the use of a smaller output filter. Since the phase leg provides three levels of voltages.

An additional advantage of the TL inverter is that the voltage stress [11] of the switches is reduced to half of the input voltage, which makes it suitable for high input voltage power Conversions. In addition, for some of the TL converters, the advantages also include a reduction in the size of the storage elements.

This technique has been applied to dc–dc converters by Pinheiro and Barbi to reduce the voltage stress of the switches. It should be emphasized that the application of the technique does not create a TL voltage state in the case of dc–dc converters. Nevertheless, since the phase leg of this dc–dc converter is similar to that of the TL inverter, i.e., having four switches, two dividing capacitors at the input, and two clamping diodes, this dc–dc converter was named TL converter. However, it will be shown in the following section that the so-called TL converter is essentially a half-bridge (HB) converter. To differentiate it from other TL derived converters, in this paper, we will refer to it as the HB TL converter.

3. ANALYSIS OF TOPOLOGY SYNTHESIS

3.1 Hybrid boost converter based on three phase diode clamped inverter

The conventional single-phase diode-clamped three-level inverter [12] is shown in Fig. 2(a), and there are four power switches Qa1 – Qa4 with corresponding antiparallel diodes Da1 – Da4. Based on this topology, two classical three-level dc–dc converters (buck and boost converters) are deduced, as shown in Fig. 2(b) and (c). In fact, there are still two other boost three-level converters shown in Fig. 3, which can also be deduced from the inverter in Fig. 2(a). However, these two boost three-level converters cannot operate separately, due to the unbalanced capacitor voltages across (C11, C12) or (C21, C22).

![Fig. 2. Single-phase diode-clamped three-level inverter and two classical three-level dc–dc converters](image1)

![Fig. 3. Two deduced three level DC-DC converters](image2)

In order to not only improve the dc–bus voltage and power level of PV generation systems, but also obtain narrower pulse voltages from the difference between wider ones through the idea based on the topology of a single-phase diode-clamped inverter with two three-level legs, a novel hybrid boost three-level converter can be synthesized by the two boost three-level Converters [13] I and II in Fig. 3. Naturally, \( V_{in1} \), \( V_{in2} \) and \( L_{d1}, L_{d2} \) are the input dc voltages and filtering inductors of Converters I and II, respectively.
Then, the input power level of the hybrid converter can be improved by means of two converters’ input sides in series, namely \((V_{in1} + V_{in2})\), and the output power level of the hybrid converter can also be increased by the parallel connected outputs of Converters I and II, namely \((i_1 + i_2)\) as shown in Fig. 3. Therefore, the synthesized process of the hybrid converter by the mode of inputs in series and outputs in parallel is depicted in Fig. 4.

The input node c is cutoff from node g1 in Converter I, which is denoted “Cut I.” In addition, the other input node d is also cutoff from node p2 in Converter II, which is shown as “Cut II.” Then, the two input nodes c and d can be connected in series, namely both of the input dc voltage supplies \(V_{in1}\) and \(V_{in2}\) are in series. While the output structures of Converters I and II are identical, nodes \(p_1\) and \(p_2\), as well as \(g_1\) and \(g_2\) can be connected in parallel, leading to the “paralleled output +” and “paralleled output –” for the hybrid converter as shown in Fig. 4.

A novel hybrid boost three-level dc–dc converter is proposed, taking the topology established without a transformer or coupled inductors into account. It is composed of only one inductor, two output capacitors in series, and other power semiconductor components, which are easy to be integrated. This proposed converter cannot only realize high step-up gain, but also avoid extreme duty cycles.

3.2 Operation principle of topology

According to Fig. 3.4, the output pulse voltages of two half bridges are \(V_{ag}\) and \(V_{bg}\), and then the output pulse voltage \(V_{ab}\) of the hybrid converter can be described as

\[
V_{ab} = V_{ag} - V_{bg} \tag{1}
\]

The output dc voltage \(V_{pg} = V_{o}\) can be obtained from \(V_{ab}\), filtering by capacitors \(C_{f1}\) and \(C_{f2}\).

The corresponding states of power components for instantaneous \(V_{ab}\) of the hybrid converter are listed in Table III, and it is also assumed that the voltages across capacitors \(C_{f1}\) and \(C_{f2}\) are equal, namely \(V_{Cf1} = V_{Cf2}\). When the power switches \(Q_1\) and \(Q_4\) are turned OFF, the capacitors \(C_{f1}\) and \(C_{f2}\) in series are charged together by both the dc voltage source \(V_{in}\) and the energy stored in \(L_1\) through diodes \(D_1 - D_4\). Then, the instantaneous \(V_{ab}\) of the hybrid converter is \(V_{o}\). While \(C_{f1}\) is charged by \(V_{in}\), as well as the energy stored in \(L_2\) through diodes \(D_2, D_3, D_5, D_6\), when only \(Q_1\) is turned ON. At the same time, \(C_{f2}\) is discharged for the load, and the instantaneous \(V_{ab}\) is \(V_{o}/2\), which is the voltage across \(C_{f1}\). In addition, the redundant state for the instantaneous \(V_{ab} = V_{o}/2\) is that \(C_{f2}\) is charged by \(V_{in}\) and the energy stored in \(L_4\) through diodes \(D_7, D_8\), and \(D_9\) when only \(Q_4\) is turned ON. Meanwhile, \(C_{f1}\) is discharged for the load, and \(V_{ab}\) is the voltage across \(C_{f2}\). When the power switches \(Q_1\) and \(Q_2\) are turned ON, the energy is stored in \(L_1\) through diodes \(D_4\) and \(D_5\), while \(C_{f1}\) and \(C_{f2}\) are discharged together for the load. Then, the instantaneous \(V_{ab}\) is zero. Moreover, the other two redundant states for \(V_{ab} = 0\) is that power switch pairs \((Q_2, Q_4)\), or \((Q_3, Q_5)\) are turned ON, respectively, the energy is stored in \(L_1\) by the corresponding diodes, while \(C_{f1}\) and \(C_{f2}\) are discharged together for the load.

4. PWM CONTROL OF DESCRIBED TOPOLOGY

According to Table I, the switching functions of \(V_{ag}\) and \(V_{bg}\) for both half-bridges can be described as follows:

\[
V_{ag} = (1 - S_1 \cdot S_2) \cdot (V_{Cf1} + V_{Cf2}) - (S_1 - S_2) \cdot V_{CT} \tag{2}
\]

\[
V_{bg} = S_3 \cdot V_{CT} + S_4 \cdot V_{Cf2} \tag{3}
\]
where $Sx$ (x = 1, 2, 3, 4) = “0” or “1” is the function of the switching state of the corresponding power switch. According to (1)–(3), the switching function of $V_{ab}$ for the hybrid converter can be written as:

$$V_{th} = [(1 - S_1) \cdot (1 + S_2) - S_3] \cdot V_{Cf1} + (1 - S_1 \cdot S_2 - S_4) \cdot V_{Cf2}$$

(4)

Then, the PWM control method can be depicted in Fig. 6, according to (2)–(4) and the consideration that switching actions are the least between two adjacent switching states $(S_1S_2S_3S_4)$ in one carrier period, as well as the required balancing principle for charging or discharging of $C_{f1}$ and $C_{f2}$. In Fig. 6, $m_1$ and $m_0$ are the modulation indexes for the double modulation waves, and carrier_1, carrier_2 are designed as π phase-shifted carriers due to the two half-bridges structure of the hybrid converter. In addition, the PWM control[14]-[16] law can be described as

Fig 6. Switching Pulses

According to Table I, there are such three switching states in each carrier cycle, namely “0000”, “1100” and “0011” that $C_{f1}$ and $C_{f2}$ are charged or discharged together in respective switching state. Then, the voltage balancing of $C_{f1}$ and $C_{f2}$ would not be affected by these three switching states. However, in the switching states “1000” and “0001,” $C_{f1}$ is discharged during the first half-cycle, while $C_{f2}$ is done in the second half-cycle. If the discharging time $(t_1+t_2)$ is not equal to $(t_3+t_4)$, the voltage balancing of $C_{f1}$ and $C_{f2}$ will be affected seriously. $t_{on1} - t_{on4}$ are the turn-on time of $Q_1 - Q_4$ respectively, while the carriers are about $t = T/4$ or $t = 3T/4$ symmetric in each half-carrier period, the discharging time of capacitors can be written as:

$$t_1 = t_2 = (t_{on1} - t_{on2})/2$$

$$t_3 = t_4 = (t_{on4} - t_{on3})/2$$

(6)

In addition, while the carriers are about $m = 0.5$ symmetric in each carrier cycle, the turn-on time $Q_1$ - $Q_4$ can be written as

$$t_{on1} = t_{on4}$$

$$t_{on2} = t_{on3}$$

(7)

<table>
<thead>
<tr>
<th>$V_{vo}$</th>
<th>$V_{vo}$</th>
<th>$V_{ab}$</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$I_L$</th>
<th>$C_{f1}$</th>
<th>$C_{f2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0000</td>
<td>0.0000</td>
<td>0.1111</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>ch</td>
<td>ch</td>
</tr>
<tr>
<td>0.0001</td>
<td>0.0010</td>
<td>0.1100</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>ch</td>
<td>disc</td>
</tr>
<tr>
<td>0.0100</td>
<td>0.0111</td>
<td>0.1001</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>disc</td>
<td>ch</td>
</tr>
<tr>
<td>0.0111</td>
<td>0.1101</td>
<td>0.0100</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>disc</td>
<td>disc</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$V_{vo}$</th>
<th>$V_{vo}$</th>
<th>$V_{ab}$</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$I_L$</th>
<th>$C_{f1}$</th>
<th>$C_{f2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0000</td>
<td>0.0000</td>
<td>0.1111</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>ch</td>
<td>ch</td>
</tr>
<tr>
<td>0.0001</td>
<td>0.0010</td>
<td>0.1100</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>ch</td>
<td>disc</td>
</tr>
<tr>
<td>0.0100</td>
<td>0.0111</td>
<td>0.1001</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>disc</td>
<td>ch</td>
</tr>
<tr>
<td>0.0111</td>
<td>0.1101</td>
<td>0.0100</td>
<td>0</td>
<td>0</td>
<td>0.00</td>
<td>disc</td>
<td>disc</td>
</tr>
</tbody>
</table>

TABLE I

Therefore, the discharging time $(t_1 + t_2)$ of $C_{f1}$, and $(t_3 + t_4)$ of $C_{f2}$ can be equal by means of (6) and (7), namely

$$t_1 + t_2 = t_3 + t_4$$

Fortunately, the load current could be considered constant in each carrier cycle (T is small enough)[17], and the alternating discharging time of $C_{f1}$ and $C_{f2}$ are identical, and then the voltages across $C_{f1}$ and $C_{f2}$ can be self-balanced.

4.1 Topology Operation With High Voltage Gain

As per the hybrid converter operation, energy $W_{st}$ is stored in $L_f$ when $V_{in} = 0$, otherwise, energy $W_{tr}$ is transferred. It is assumed that the inductor current $I_{on}$ is continuous, and $I_L$ is its average current. Then, $W_{st}$ and $W_{tr}$ can be described in one carrier period as follows:

$$W_{st} = V_{in} \cdot I_L \cdot t_{on2} \times 2$$

(8)

$$W_{tr} = (V_o - V_{in}) \cdot I_L \cdot (T/2 - t_{on1}) \times 2 + (V_o - V_{in}) \cdot I_L \cdot (t_1 + t_2) \times 2$$

(9)

As a result, the output dc voltage $V_o$ is obtained from (6) and (9) as follows:

$$V_o = V_{in} \left[ \frac{T}{T - (t_{on1} + t_{on2})} \right]$$

(10)

where $d_1$ and $d_2$ are the duty cycles of $Q_1$ and $Q_2$, respectively. Then, all the duty cycles of power switches can be described as follows with the modulation indexes $m_0$ and $m_b$, by means of (7).

$W_{st}$ and $W_{tr}$ are the required stored energy and transferred energy, respectively.
\[ d_1 = d_2 = 1 - m_b \]
\[ d_3 = d_4 = m_a \]  
\[ M = \frac{V_{o}}{V_{in}} = \frac{1}{1 - (d_1 + d_3)} = \frac{1}{m_b - m_a} \]  
\[ \text{where } d_1 \text{ and } d_2 \text{ are the duty cycles of } Q_1 \text{ and } Q_2, \text{ respectively. Then, the voltage gain } M \text{ of the hybrid converter is written as follows by (10) and (11)} \]

Moreover, the extreme duty cycles of the power switches can be avoided, if both \( m_b \) and \( m_a \) are around 0.5 with the limited conditions: \( m_a < 0.5 < m_b \) and \( m_b + m_a < 1 \).

As to the given voltage gain \( M \), there is an infinite number of solutions to \( m_b \) and \( m_a \). However, a tradeoff between the nonextreme duty cycles of power switches and the fluctuating amplitude of the inductor current must be well considered, and the better solution is described as

\[ m_b = 0.5 + \left( \frac{1}{4M} \right) \]
\[ m_a = 0.5 - \left( \frac{3}{4M} \right) \]

Combining (11) with (13), the relationship between the duty cycles of the power switches. It is indicated that the higher \( M \) is, the closer to 0.5 \( d_x \) (\( x=1, 2, 3, 4 \)) become. Therefore, the proposed hybrid converter is suitable for the high step-up dc–dc voltage source interface of PV generation systems.

### 4.2 Experimental Result:

<table>
<thead>
<tr>
<th>Parameters used</th>
<th>Value (units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>50V</td>
</tr>
<tr>
<td>Inductor ( L )</td>
<td>317µH</td>
</tr>
<tr>
<td>Switching freq ( f_c )</td>
<td>11.5kHz</td>
</tr>
<tr>
<td>Load resistance</td>
<td>300~2000Ω</td>
</tr>
</tbody>
</table>

### 4.3 Matlab simulation

Figure 7 shows the Matlab/Simulink model of the proposed circuit. Output parameters at gain value 25, and hence we reach to a satisfactory conclusion.

In the Matlab/Simulink model of the proposed circuit, we have assumed that \( V_{cf1} = V_{cf2} \). Figure 8, 9 and 10 represent the output performance characteristics of the proposed circuit with the help of which result is proved and obtained.

\[ \text{Fig. 7. Simulation of the proposed circuit} \]

\[ \text{Fig. 8. Output with gain 25} \]

The output three-level voltages \( V_{ag} \) and \( V_{bg} \) of both half bridges are shown. \( V_{ab} \) is the difference of \( V_{ag} \) and \( V_{bg} \) \( \{V_{ab} = (V_{ag} - V_{bg}) = V_o\} \). Here input voltage = 50V, output voltage = 1200V, hence, gain = 25

\[ \text{Fig. 9. Inductor Current Waveform} \]
Three-level hybrid boost dc–dc converter presented in this paper is based on the conventional single-phase diode clamped three-level inverter. It can operate with transformer less high voltage gain, as well as duty cycles of the power switches closer to 0.5 with the increasing voltage gain, instead of the extreme duty cycles.

Moreover, the capacitor voltages can be balanced both in dynamic and steady states by the proposed PWM control method. The proposed converter is suitable for PV generation systems connected to the grid with parallel-connected low-voltage PV arrays.

6. REFERENCES

**Conducted EMI Attenuation in Power Converters Using Chaotic Frequency Modulation Technique in Electric Vehicles**

Suganya M, Sugapriya P, VijayaKumari V  
B.E., Electrical and Electronics Engineering, Velammal College of Engineering and Technology, Madurai, India.

Mr. N. Selvam, M.E., Assistant Professor, Electrical and Electronics Engineering Velammal College of Engineering and Technology, Madurai, India.

**ABSTRACT**--In the growing trend of automobile industry, Electric Vehicles (EVs) have made a great impact in conserving the nature as well as energy. Yet, they are bound to be a prominent source of interference. This interference not only decreases the efficiency of the system but also affects the performance of the nearby systems. Therefore, it becomes necessary to take measures to reduce the Electromagnetic Interference (EMI) for better results. In EVs, the main source of EMI is found to be the power converters used due to the fast switching frequency from Pulse Width Modulation (PWM) technique which results in high change in current and high change in voltage. This paper emphasizes on the attenuation of EMI by using Chaotic Frequency Modulation technique as it greatly suppresses the interference emissions by using variable switching frequency.

**Keywords**-- EV; EMI; Chaotic modulation; PWM

**I. INTRODUCTION**

EMI, also referred to as Radio Frequency Interference (RFI) is the unwanted disturbance that occurs due to the oscillations of electric fields and magnetic fields. When we go for fast operation in power converters, high frequency arises which results in EMI [2]. EMI is of two categories which are Conducted EMI and Radiated EMI which is depicted in Fig.1. The path for conducted EMI is conductors and it has a frequency less than 30MHz while for Radiated EMI, the path of conduction is any air medium or the surrounding medium with a frequency greater than 30MHz. Conducted EMI is further classified into Common Mode and Differential Mode. It is essential that the common mode conducted EMI is reduced as it generates further radiated emissions. The sources of EMI could be both natural and man-made. The natural EMI occurs from stars and other electrostatic discharges while man-made EMI includes signals from navigation, electronic equipments, etc., EMI has harmful effects both on human and on the apparatus. In humans, it affects the health while in electronic equipments, the performance is degraded.

**II. EMC**

Electromagnetic Compatibility (EMC) refers to the ability of the electronic device and it concerns with the proper functioning of the apparatus in their corresponding EMI environment. It ensures that the standards and test procedures of the system are conducted accordingly to function without any losses or without generating any further EMI emissions [2]. EMC standards are specified by committees such as CISPR (Comité International Spécial des Perturbations Radioélectriques), FCC (Federal Communications Council), SAE (Society of Automobile Engineers). The various methods of electromagnetic interference coupling between an emitter and a receptor are as follows:

- Radiation coupling
- Conduction coupling
- Capacitive coupling
- Inductive coupling

Fig.1 EMI types
III. ELECTRIC VEHICLES

Any automobile that consists of an Electric Drive train and that runs on an Electric Motor is referred to as an Electric Vehicle (EV). The block diagram of an electric drive system is shown in Fig.2.

An Electric Vehicle receives the primary supply from 230V mains which is converted to DC by means of a converter and is then stored in Battery. This converter is the source of EMI due to its high switching frequency [5]. The battery used in olden days was Lead Acid battery but today, everybody prefers Lithium ion battery for better performance and reduction in weight. From the battery, the DC power is converted to AC by means of an Inverter after which the AC power is used to drive the Electric motor. In electric vehicles, Conducted EMI dominates Radiated EMI as conducted EMI is caused by bundled conductors.

IV. PULSE WIDTH MODULATION

In addition to the usage of PWM for encoding information, PWM technique is also used to control the power supplied to the devices by switching the devices accordingly [6]. In this technique, the phase angle between the supply voltage and current is maintained constant. The output voltage is controlled by varying the duty cycle. For the output voltage to be smooth without any ripples, the switching frequency has to be higher. As EMI centers on switching frequency, for PWM technique, even though the loss is less, it results in increased EMI. In order to overcome this, we go for Chaotic frequency modulation.

V. SPREAD SPECTRUM SIGNALING

Spread spectrum signaling is one of the Interleaving techniques [2]. The main aim of spread spectrum signaling is to reduce the EMI by reducing the switching frequency and the amplitude of harmonics which is illustrated in Fig.3. This is achieved by the generation of an additional set of sideband frequencies with lesser amplitude. This is where a signal with a particular bandwidth is spread over frequencies with wider bandwidth. Wider spectrum with lower amplitudes of the signal mainly depends upon several factors as Modulation profiles, Modulating frequency, Carrier frequency, modulation index and rate of percentage [1]. The rate of modulation is defined as the ratio of peak deviation of switching frequency to carrier frequency.

Fig.3 Spread Spectrum Signaling
VI. CHAOTIC FREQUENCY MODULATION

Chaotic theory deals with the behavior of dynamical systems which are highly sensitive to initial conditions. Chaotic signals are usually broadband signals which when modulated produce frequencies over wide range whose generation is illustrated in Fig.4. These systems are fully deterministic with no random elements involved but they are highly dependent on initial conditions. A small change in the initial condition produces a diverging output. Chaotic frequency modulation is one of the spread spectrum techniques where the signal frequency is spread over wide bandwidths \[1\]. As a result of this, the amplitude of the signal is lowered which results in suppressed EMI.

This shows that the resulting signal of chaotic frequency modulation is characterized by a continuous spectrum with lower amplitude.

VII. IMPLEMENTATION OF CHAOTIC CIRCUIT

As we have seen earlier, in an Electric Vehicle, the converter tends to be the source of EMI. So, the chaotic circuit is implemented here by means of a chaotic modulator as shown in Fig.5. The chaotic signals modulate signals with narrowband information to larger bandwidth and result in signals with lower Power Spectral Density (PSD) level in the signals which lead to reduction in EMI \[4\].

Fig.5 Chaotic modulator in power converter

Chaotic modulator is used to generate the analog patterns according to the input digital bits. In a chaotic modulator, the output patterns are generated based on the input bits with the help of chaotic patterns and the output is non-repeating. The chaotic signals generated are applied to the switching of the power electronic devices used. The TMS320F2812 is a 32-bit fixed-point Digital Signal Processor. A DSP is used because in order to generate chaotic signals, more computations are required which can be performed by a DSP. The higher the accuracy is required, the more computations have to be performed. Chaotic phenomenon can be easily implemented by means of the chua’s circuit as it behaves like a non-periodic oscillator which is illustrated in Fig.6.

The chua’s circuit which exhibits chaotic behavior can be implemented with 1 inductor, 2 capacitors, 2 resistors among which one is non-linear and the other is linear. The chaotic circuit simulated above consists of resistances \( R = 1.6k\Omega \), \( R_1 = R_2 = 2.2k\Omega \), \( R_3 = 3.3k\Omega \) and \( R_4 = 2.2k\Omega \), capacitances
C1 = 100 pf, C2 = 1nF. The inductor used is L = 180mH.

Fig. 5 Chaotic modulator in power converter

It uses the Current Feedback Operational Amplifier AD844 with a voltage bias of ±9 V. The circuit performance is affected by the load conditions. Here, in the above circuit, the smaller the load, the smaller the resistance R3 is required to maintain chaos in the circuit.

With the implementation of chaotic circuit, significant changes can be observed in the rectifier output. The rectifier output without the chaotic circuit as shown in Fig. 7 has more ripples when compared with that of the rectifier output with chaotic circuit as shown in Fig. 8.

Fig. 7 Rectifier output without chaotic circuit

Fig. 8 Rectifier output with chaotic circuit

The implementation of chaotic circuit is mainly used to reduce the Conducted EMI. The conducted noise without the usage of chaotic circuit is illustrated in Fig.9 where it can be seen that the frequency band is narrow and also with higher amplitude.

Fig. 9 Conducted EMI noise without chaotic circuit

The conducted EMI from the electric drive train with the implementation of chaotic circuit as shown in Fig.10 has lower amplitude signals with wider band of frequency.

Fig. 10 Conducted EMI noise with chaotic circuit
VIII. CONCLUSION

Thus, it can be seen that from the above simulations that Chaotic frequency modulation technique effectively suppresses EMI than using any Filters or any shielding techniques. Modulating the signals over wider bandwidth and lesser amplitude mitigates Conducted EMI due to which major loss occurs in Electric Vehicles.

From the simulation, it is clear that after the implementation of chaotic circuit, the conducted EMI is significantly reduced.

IX. REFERENCES


AC-AC Converter based on Switched Capacitor by using Microcontroller

S.Sakthivel, Student member of IEEE
M.E-Power Electronics and Drives,
Kings College of Engineering,
Punalkulam,
Pudukkottai.
email id:sakthi0021@gmail.com

Mr. S.R. Karthikeyan, M.E.,
Assistant Professor,
Department of EEE,
Kings College of Engineering,
Punalkulam.
email id : srkeekce@gmail.com

ABSTRACT -- Switched capacitor converters are mainly used in non-isolated dc-dc converters have been a very important research topics for many years. Recently switched capacitors are used in direct AC-AC conversion. This project proposes a new static AC-AC converter based on switched capacitor principle in order to replace the conventional auto-transformer in commercial and residential applications. A switched capacitor consists of only switches and capacitors. The main advantage of the proposed converter is the absence of magnetic elements which is present in the transformer. By replacing transformers in AC-AC conversion by switched capacitor converters we can improve their efficiency. In order to demonstrate the performance of converter the experimental results of prototype and design example are discussed here. The maximum and nominal efficiency shown by the prototype was 95% respectively.

Index terms -- AC-AC converter, step down converter, switched capacitor (SC).

I INTRODUCTION

Transformers are commonly used in applications which require the conversion of AC voltage from one voltage level to another. In general the auto transformer efficiency is poor and it produces audible noise. The global demand of copper utilized in transformer increasing nowadays exceeding the supply.

The SC converters are important research topic for many years in relation to non-isolated DC-DC conversion. By using SC principle applications like mobile chargers, electric vehicles, multilevel inverters, induction heating, speed control of AC drives, etc. As SC converters has advantages of using switching devices they can achieve size reduction, weight, cost and high power density.

The design of an SC converter requires an understanding of the technology trade-off is involved. A wide variety of capacitors are available from aluminum electrolytic through various types of solid dielectric to film and ceramic. Each technology has a relevant field of use depending on its loss characteristics. Capacitor technology choice is particularly important for high power converters, such as proposed for 220v to 110v conversion.

The switched capacitor principle was recently extended to AC-AC static conversion for the first time. In the article, a brief analysis and experimental results for a step down/step up converter with rated power of 600w, 220/110v, 60Hz, switching frequency of 50 kHz and a measured peak efficiency of 91%. The converter supplies a differential output voltage and it employs two SC’s and eight unidirectional switches.

II RELATED WORK

To understand the basic concepts of switched capacitor in field of power electronics [1]. To design and analyzing the switched capacitor circuit [2]. Performance parameters of switched capacitor can be designed [3]. Optimization of switched capacitor techniques can be obtained [5]. To obtain high power efficiency of DC-DC converters can be achieved [7]. A 600w direct AC-AC conversion by using switched capacitors can be obtained [3].

III PROPOSED SC AC-AC CONVERTER

The block diagram of the proposed system is shown in fig 2.1. It consists of ac supply, converter using switched capacitor principle, driver circuit, power supply, isolator, ADC (Analog to Digital converter) and ac drive. The digital signal to the microcontroller was provided by using ADC.
converter. The converter consists of MOSFET switches. The gating signal to these switches is given by the microcontroller.

The driver circuit employed here is for amplification i.e. converting the weak signal of the microcontroller. Isolator is employed for the purpose of protection of both low power and high power components. It isolates the AC source and power supply.

![Diagram of AC-AC converter using SC](image)

**Fig 3.1 Block diagram of AC-AC converter using SC**

The new proposed SC AC-AC converter topology is shown in figure 2.2. The topology consists of four switches (S1, S2, S3, and S4) and three capacitors represented as C1, C2 and C3. The main characteristics of the proposed converter is employing two fixed capacitor and one SC, it supplies an output voltage has a common reference with input voltage, and it uses four bi-directional switches. \( V_H \) and \( V_L \) represent high side voltage and low side voltage respectively.

![Diagram of Step down configuration](image)

**Fig 3.2 Step down configuration**

In this converter one half of the high side voltage is converted into low side voltage which represent that \( V_L = V_H / 2 \). Each ideal switches are connected to a resistance in order to minimize the losses. The gating signals of MOSFET’s and modeling of switch can be shown in fig 2.3 and fig 2.4 respectively.

![Diagram of Switch](image)

**Fig 3.3 Gating signals of step down converter**

**Fig 3.4 Modeling of a switch**

**IV PRINCIPLE OF OPERATION**

The principle of operation of the proposed SC AC-AC converter is discussed in two ways: low frequency
analysis and high frequency analysis. In high frequency analysis operating stages of converter is given by the same way low frequency analysis deals with frequency of input voltage.

During positive half cycle switches s1 and s3 are turned ON, capacitor C2 discharges and capacitor C3 charges during the first part of the stage (\(\Delta t_{1a}\)). When their currents reaches zero, C2 starts to charge and C3 starts to discharge until the end of (\(\Delta t_{1b}\)). Capacitor C1 charges throughout this stage and the power source \(V_H\) delivers energy to the circuit. Switches S1 and S3 are turned OFF at this stage.

Second stage starts when switches s2 and s4 are turned ON. Initially the power source receives energy from the circuit, capacitor C2 charges, and capacitor C3 charges until their current reaches zero (\(\Delta t_{2a}\)). After this, the power source delivers energy to the circuit, capacitor C2 charges and capacitor C3 discharges until the end of the stage (\(\Delta t_{2b}\)). Capacitor C1 discharges throughout this stage. Switches s2 and s4 are turned OFF at the end of the second stage.

During negative cycle operation of converter has similar operation with different current direction. At (\(\Delta t_{1A}\)) switches s1 and s3 are turned ON when capacitor C2 charges and C3 discharges during first stage of operation. When the current reaches zero C2 starts to discharge and C3 starts to charge until end of (\(\Delta t_{1B}\)). Capacitor C1 charges at both the stages, when capacitor C1 discharges switches s1 and s3 comes to OFF at this stage.

Second stage starts when switches s2 and s4 are turned ON. Initially the capacitor C2 charges and C3 discharges to the load during (\(\Delta t_{2A}\)). Capacitor C2 discharges to load and capacitor C3 charges until the end of (\(\Delta t_{2B}\)). At both the stages capacitor C1 charges when their currents reaches to zero the capacitor C1 discharges switches s2 and s4 comes to OFF state.

Fig 2.5 shows the proposed SC AC-AC converter for step up configuration. In this converter low side voltage \((V_L)\) can be converted into high side voltage \((V_H)\). Similarly the step up operation and waveform can be achieved by the above switching sequences.

V PROTOTYPE IMPLEMENTATION EXPERIMENTAL RESULTS

After the principle of operation a prototype was built to verify the operation of proposed converter in laboratory. The main components and their ratings are used in the prototype are presented in Table I. The pictorial representation of prototype was implemented in figure 4.1.

![Fig 5.1 Step down configuration using MATLAB](image)

The above diagram represents the MATLAB Simulink circuit diagram of step down configuration of AC-AC converter by using switched capacitor principle. Here four MOSFET switches are used. The simulated waveforms of this circuit diagram consist of gating signal of switches, comparison of input and output voltages and voltage across capacitors.

<table>
<thead>
<tr>
<th>Description</th>
<th>Qty</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak voltage ((V_i))</td>
<td>-----</td>
<td>100v</td>
</tr>
<tr>
<td>Output voltage ((V_o))</td>
<td>-----</td>
<td>50v</td>
</tr>
<tr>
<td>Frequency(f)</td>
<td>-----</td>
<td>50Hz</td>
</tr>
<tr>
<td>Switching frequency(f_s)</td>
<td>-----</td>
<td>100KHz</td>
</tr>
<tr>
<td>Capacitors C2,C3</td>
<td>03</td>
<td>100µF</td>
</tr>
<tr>
<td>C1</td>
<td></td>
<td>10 µF</td>
</tr>
<tr>
<td>MOSFET switches s1,s2,s3 and s4</td>
<td>04</td>
<td>FQA62N25C</td>
</tr>
</tbody>
</table>
The above waveform describes that gating signals of MOSFET switches in direct AC-AC conversion. When switches s1 and s3 are turned ON, switches s3 and s4 are turned OFF. When switches s3 and s4 are turned ON, switches s1 and s3 are turned OFF.

Fig 4.4 shows the waveforms of voltage across capacitors. The given capacitors are connected in parallel with the given AC source terminals. In general voltage across the parallel circuit remains same. The prototype was tested for the step down configuration and the basic waveforms were acquired.

VI. HARDWARE IMPLEMENTATION

The fig. 6.1 shows the design example of the step down converter. The design of the step down AC-AC converter consists of the MOSFET as a switch, isolator, and capacitors, the microcontroller is employed to deliver the gating signal to the MOSFET switches. The following table shows the hardware specifications of the converter. The fig
6.2 shows the hardware circuit with load. The load employed in the hardware design is the shaded pole induction motor.

![Fig. 6.2 Hardware design with load (Shaded pole Induction Motor)](image)

The MOSFET IRF450, its drain to source resistance ($R_{DS}=0.5\Omega$), at $V_{GS}=10V$, and $I_D=12A$). Its maximum drain source voltage is 500V under testing condition of $V_{GS}=0V$ and $I_D=1.0mA$.

Its input capacitance, output capacitance, and reverse transfer capacitance 2700, 600, and 240 pF respectively, under the testing condition of $V_{GS}=0 V$, and $V_{DS}=1.0 V$, the frequency is 1.0 MHz. The temperature coefficient of the breakdown voltage is 0.78 V/°C.

The Driver circuit employed in the proposed system is that ULN2003, the value of the output voltage is 50 V, the input voltage is 30 V, the continuous collector current is 500mA, the continuous base current is 25 mA, the junction temperature is 150°C.

The ADC employed in the proposed system is the ADC 0808. The ADC 0808 is the data acquisition system has the monolithic CMOS devices with the 8 block bit Analog to Digital converter. The supply voltage of the ADC converter is 5V. The voltage at the control pins ranges from the -0.3 V to 15V. The storage temperature of the ADC ranges from the -65°C to 150°C.

The power supply pin is the three terminal pins. The power supply employed in the proposed system is the LM 7805. The power supply pin is also known as the power regulator which regulates the power delivers to the low power devices such as the microcontrollers and ADC and isolators. The main advantages of the power regulator LM 7805 is that high power capability, output transistor safe area compensation. The input voltage, output current, and the junction temperature is 25 V, 1.5 A, 25°C respectively.

The isolator employed in the proposed system is that MCT2E. The MCT2E is the phototransistors, has the free ambient temperature of 25°C, the operating range of the 1.5 kV and 2.5kV rating. It is a plastic dual in line package. The input and the output voltage ranges from the 3.5 KV to 5.5 kV. The MCT2E has the equivalent circuit resistance of 2.5Ω.

The microcontroller employed in the proposed system is the ATME 895c1. This microcontroller was programmed by using the Kail software. The ATME 895c1 is the high performance, low power, and 8 bit CMOS device. The operating voltage of the microcontroller is 5V, flash programmable, and Erasable Read Only Memory (EPROM).

### TABLE 2

<table>
<thead>
<tr>
<th>S.No</th>
<th>Components</th>
<th>Qty</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>MOSFET(IRF 450)</td>
<td>4</td>
<td>500V</td>
</tr>
<tr>
<td>2.</td>
<td>ULN 2003</td>
<td>1</td>
<td>----</td>
</tr>
<tr>
<td>3.</td>
<td>MCT2E</td>
<td>1</td>
<td>----</td>
</tr>
<tr>
<td>4.</td>
<td>ADC0808</td>
<td>1</td>
<td>----</td>
</tr>
<tr>
<td>5.</td>
<td>ATMEL89C51</td>
<td>1</td>
<td>----</td>
</tr>
<tr>
<td>6.</td>
<td>CAPACITORS</td>
<td>4</td>
<td>400V/470µF</td>
</tr>
<tr>
<td>7.</td>
<td>STEP DOWN</td>
<td>1</td>
<td>12-0-12</td>
</tr>
<tr>
<td>8.</td>
<td>REGULATORS</td>
<td>2</td>
<td>----</td>
</tr>
</tbody>
</table>

### VI. CONCLUSION

A new static AC-AC converter based on switched capacitor is proposed in this paper. The proposed ac-ac converter employs only switches and capacitors. In the absence of magnetic elements less should be minimized. The main objective of the proposed system is to reduce the stress voltage caused by using transformers. The converter employs a single switched capacitors and has a common reference between input and output voltages. The main advantage of this proposed system is it does not require any complex control algorithms. Thus, the operation of step down AC-AC conversion process had achieved by using the
switcheed capacitor and the respective waveform has obtained.

REFERENCES


S.Sakthivel was born in Thanjavur, Tamilnadu in 1992. He received B.E. degree in Electrical and Electronics Engineering from Parisutham Institute of Technology and Science. He is currently doing his post graduate in Power electronics and drives in Kings college of engineering.


S.R.Karthikeyan was born in Thanjavur, Tamilnadu in 1983. He received B.Tech and M.E degree in Electrical and Electronics Engineering and Power Electronics & Drives from SASTRA University and JJ College of Engineering in 2005 and 2008 respectively. He is currently working as Assistant Professor in the department of EEE at Kings College of Engineering.