Hybrid Multilevel Inverter with Reduced Switches and Harmonics

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Abstract - *In this project mainly focused on the design and implementation of new topology in a 63 level Hybrid multilevel inverter by using only a 9 switches. The main merit of the new topology is to reduce the lower total harmonic distortion, lower electromagnetic interference generation and high output voltage. In this project, POD carrier pulse width modulation technique is proposed, which can minimize the total harmonic distortion and enhances the output voltages from proposed work of five level inverter. From the hardware and simulation we can justified that the new topology can be recommended to single phase inverter for better performance in comparison with conventional method. The simulation is done by Mat Lab 2010 version software.*

Index Terms – *Hybrid multilevel inverter; phase opposition and disposition; harmonics; power electronics devices.*

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three level converters such as diode clamped multi-level inverter, flying capacitor multi-level inverter and cascade cell multi-level inverter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a voltage waveform. The Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output. However, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two level converter that uses high switching frequency pulse width modulation. The objective of this is to provide a complete solution to the harmonic elimination problem for multilevel inverters switching at the fundamental frequencies. This includes not only the fundamental staircase scheme, but all possible switching schemes at the fundamental frequency. This allows choosing the particular solution that gives the smallest THD. It has been shown that the fundamental staircase scheme gives the lowest THD compared to the other possible switching schemes. However, it has also been shown that switching angle solutions for the staircase scheme exist only for a limited range of the modulation index. It is desirable to operate the multilevel converter at such value of those modulation indices lower frequency harmonics are eliminated and the higher frequency harmonics are a minimum.

The proposed scheme is used to control the voltage of each of the individual level capacitors in such a way that the staircase scheme of can be used for a much larger range of the modulation index for keeping low value of THD in output voltage.

II. BLOCK DIAGRAM OF PROPOSED SYSTEM

This system consists of multi tapping transformer, full bridge rectifier with filter and Hybrid multi-level inverter. Ac load (like induction motor) is connected to Hybrid multi-level inverter. Inverter is controlled by hybrid PWM is the combination of low frequency PWM and high frequency SPWM. The block diagram of proposed system is shown Figure 1.

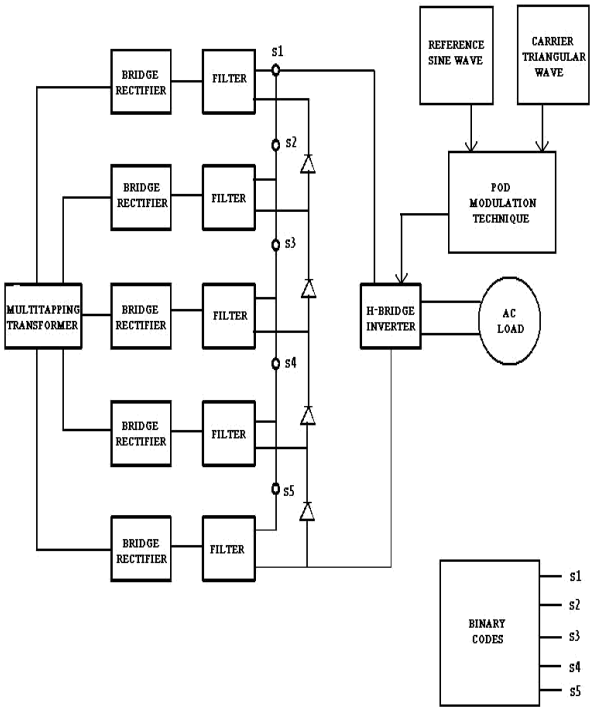

Fig.1 Block Diagram of proposed system

III. HYBRID MULTILEVEL INVERTER

Hybrid multilevel inverter gives multi-level operation by using hybrid source, hybrid configuration or hybrid device in such a way to produce output with reduced number of DC sources, high speed capability, low output switching frequency, low switching loss, high conversion efficiency, flexibility to enhance and various topologies for different applications.

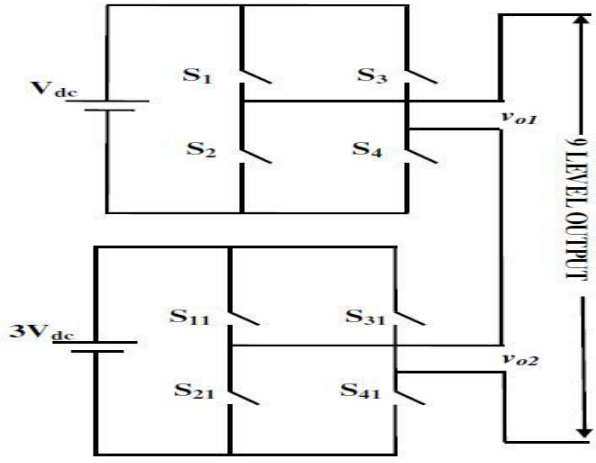

Fig.2 Hybrid Multilevel Inverter

A.Hybrid phase opposition Disposition

Multilevel inverter is an effective solution for increasing power and reducing harmonics of a waveforms. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Forth, lower acoustic noise and electromagnetic interference (EMI) is obtained.

B. Proposed hybrid PWM control method

The proposed hybrid PWM is the combination of low frequency PWM and high frequency SPWM. In each cell of cascaded inverter, the four power devices are operated

Low and High frequency PDPWM pulses at mi=0.8 and fc=1050 hz

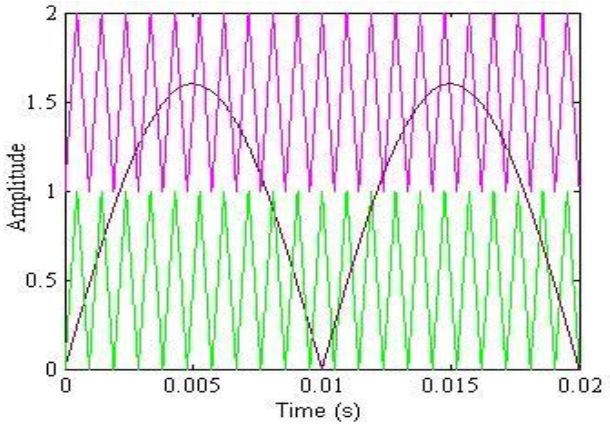

Fig.3 PWM Control waveform

At two different frequencies, two being commutated at low frequency, i.e., the fundamental frequency of the output, while the other two power devices are pulse width modulated at high frequency. This arrangement causes the problem of differential switching losses among the switches.

An optimized sequential signal added to the hybrid PWM pulses to overcome this problem. The low and high frequency PWM signal are shown in fig.3. An optimized hybrid PDPWM method

commutates the power switches at high frequency and low frequency sequentially. A common sequential signal and low frequency PWM signals are used for all cells in cascaded inverter. A high frequency SPWM for each cell is obtained by the comparison of the rectified modulation waveform with corresponding phase disposition carrier signal. The low frequency PWM signal should be synchronized with the modulation waveform. In the gate pulses are generated by a hybrid PWM controller. This controller is designed to mix the sequential signal, low frequency PWM and high frequency phase disposition sinusoidal PWM and to generate the appropriate gate pulses for cascaded inverter.

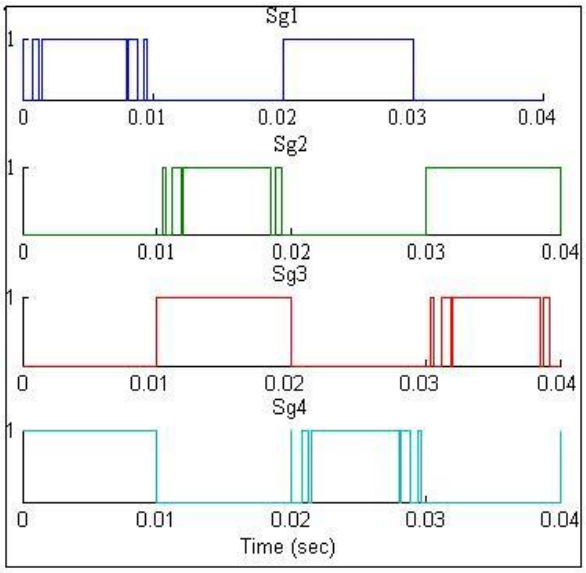

Fig.4 Control Pulses

IV. TOTAL HARMONIC DISTORTION (THD)

The total harmonic distortion or THD, of a signal is a measurement of the harmonic distortion present. It is defined as the ratio of the sum of the powers of all harmonic components to the power of the Fundamental frequency. Lesser THD, for example, allows the components in a loudspeaker, amplifier or microphone or other equipment to make a violin sound like a violin when played back, and not a cello or simply a distorted noise. In most cases, the transfer function of a system is linear and time-invariant. When a signal passes through a non-linear device, the additional content is considered as the harmonics of the original frequencies. THD is a measurement of the extent of that distortion. The measurement is most commonly the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental:

$$THD = \frac{\sum \text{Harmonics powers}}{\text{Fundamental frequency power}} = \frac{P_2+P_3+\cdots+P_n}{P_1}$$

\Other calculations for amplitudes, voltages, currents, and so forth are equivalent. For a voltage signal, for instance, the ratio of the squares of the RMS voltages is equivalent to the power ratio:

$$THD = \frac{\sqrt{V_2^2+V_3^2\ \ldots+V_n^2}}{V_1}$$

V. BRIDGE RECTIFIER

This post provides information about full wave bridge rectifier. We will also see its working principle and advantages and disadvantages.

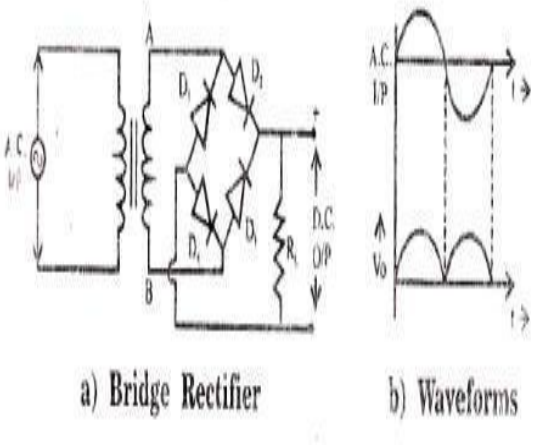

Fig.5 Full wave bridge rectifier circuit diagram

In full wave Bridge rectifier a transformer and four diodes are used. During the positive half cycle of secondary voltage, the diodes D2 and D4 are forward-biased, but diodes D1 and D3 do no conduct. The current is through D2, R, D4 and secondary winding.

During the negative half cycle, the diodes D1 and D3 are forward-biased, but diodes D2 and D4 do not conduct. The current is through D1, secondary winding, D3 and R.The load current is in the same direction in both half-cycles. Therefore a unidirectional (d.c.) voltage is obtained across load resistor. Average voltage = Vdc = 0.636 Vp = 2Vp/πWhere Vp = peak value of secondary voltage. Since each diode conducts for only half cycle, the

current rating (Io) of the diodes must be at least – half of the dc load current. i.e. 0.5 Idc.. Each diode must withstand a peak inverse voltage equal to the peak secondary voltage. PIV = Vp. Therefore the PIV rating of the diodes must be greater than Vp. As the output is a full-wave signal, the output frequency is double the input frequency. The maximum efficiency of bridge rectifier is 81.2%

A. Filter

Filters are used to narrow down the selection of data shown in the visualizations. For example, a filter could be adjusted so that data is only shown for a certain range of dates or for a certain number of food products. When you manipulate a filter, you can instantly see how the current setting affects the visible data in the visualizations related to that filter.

An analysis can be based on one or several data tables. Each data table is represented with a data table group in the filters panel. Each column in a data table is automatically represented by a filter.

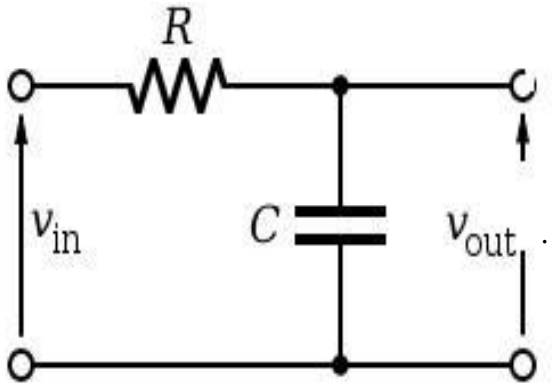

Fig.6 Filter circuit

B. N- Channel MOSFET

The N-Channel MOSFET has a N- channel region between source and drain It is a four terminal device such as gate, drain , source , body. This type of MOSFET the drain and source are heavily doped n+ region and the substrate or body is P- type. The current flows due to the negatively charged electrons. When we apply the positive gate voltage the holes present under the oxide layer pushed downward into the substrate with a repulsive force. The deflection region is populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and sources the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage a hole channel will be formed under the oxide layer.

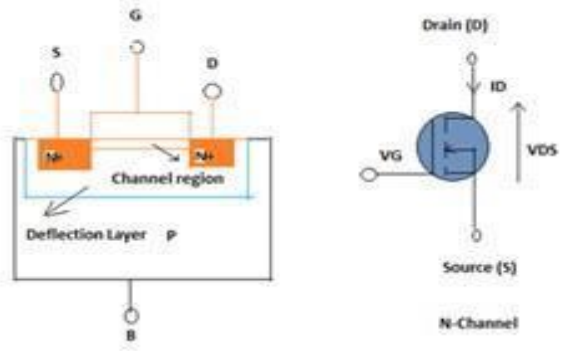

Fig.7 N- Channel MOSFET

V. SWITCHING SCHEME OF MULTILEVEL INVERTER

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, harmonic components up to m-1 can be removed from the voltage waveform. In general, the most significant low frequency harmonic components are chosen for elimination. Then, high frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics as constant, all switching angles must be less than π /2. However, if the switching angles do not satisfy the condition, this scheme is no longer valid. As a result, this modulation scheme basically provides a narrow range of modulation index, which is the main disadvantage

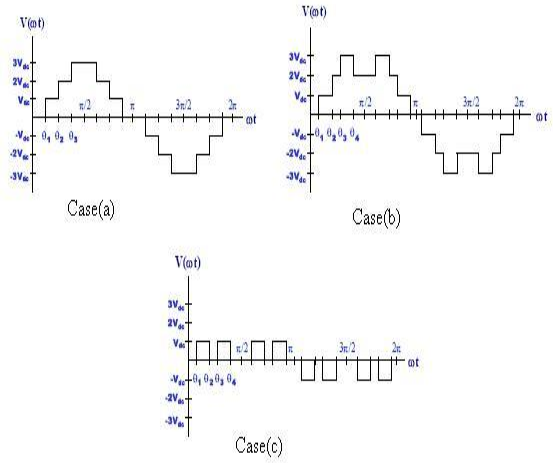

Fig.8 Switching pulses of Multilevel Inverter

TABLE.1 SWITCHING STATES

Switching Time(Sec)	Output Voltage (in volts)	Switching state								
		S1	S2	S3	S4	S5	S6	S7	S8	S9
0-1.25	0	0	0	0	0	0	0	0	0	0
1.25-2.5	50	0	1	1	0	0	0	1	1	0
2.5-3.75	100	1	1	0	0	0	1	1	0	0
3.75-5	150	1	1	0	0	1	1	0	0	0
5-6.25	150	1	1	0	0	1	1	0	0	0
6.25-7.5	50	1	1	0	0	0	1	1	0	0
7.5-8.75	100	0	1	1	0	0	0	1	1	0
8.75-10	50	0	0	0	0	0	0	0	0	0
10-11.25	0	0	0	0	0	0	0	0	0	0
11.25-12.5	-50	1	0	0	1	0	0	1	1	0
12.5-13.75	-100	1	1	0	0	1	0	0	1	0
13.75-15	-150	1	1	0	0	1	1	0	0	1
15-16.25	-150	1	1	0	0	1	1	0	0	1
16.25-17.5	-100	1	1	0	0	1	0	0	1	0
17.5-18.75	-50	1	0	0	1	0	0	1	1	0
18.75-20	0	0	0	0	0	0	0	0	0	0

VI. SIMULATION CIRCUITS OF MULTILEVEL INVERTER

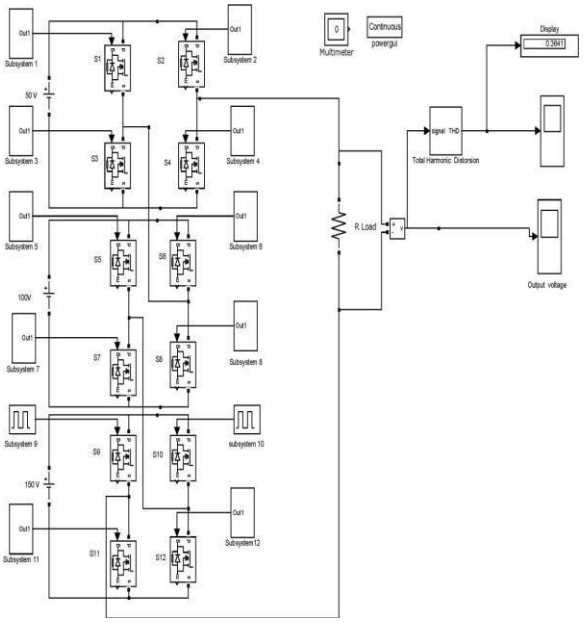

Fig.9 Simulation Circuit Diagram

In the proposed system from the single source the more number of isolated outputs can be achieved by ac source rectifier and filter. The uncontrolled rectifier used for rectification. The filter makes the pulse sating dc output in to pure dc output. To connect and or bypass the outputs of dc converter the MOSFET switches are used.by connecting or bypass the sources sequentially we can make multi stepped. By help of H-bridge circuit multi stepped DC is converter into multilevel AC. The multilevel AC output is connected with motor.

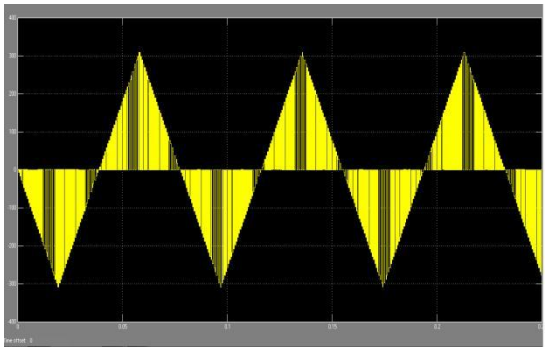

Fig.10 Simulation Output Waveform

VII. CONCLUSION

A strategy to minimize the total harmonic distortion(THD) when controlling a multilevel converter to act as a static VAR compensator has been presented. Set of solutions has been found for switching multilevel inverter's power electronic devices at fundamental frequency and eliminate the lower order harmonics. The voltage levels of the multilevel inverter can be controlled so that it operates in an optimum amplitude modulation index regime that minimizes its output voltage THD.

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