Seventeen Level Modular Multi Level Inverter

SK Khadarbasha[1], G V V Nagaraju[2]
[1]pursuing M.Tech (EEE), [2]working as Assistant Professor (EEE),
Nalanda Institute Of Engineering and Technology (NIET)Kantepudi(V), Sattenpalli(M), Guntur (D)-522438,Andhra Pradesh.

Abstract-

This paper concentrated on the modular multi level inverters (MMC) has enhanced features for the high power energy conversion based applications. From the last past years MMC has specified unique investigation completed to identify the technical aspects interconnected with proper control techniques for the MMCS. This paper concentrated on the MMC operation under basic criteria's also along with seventeen levels MMC proposed and analyzed with an effective Pulse Width Modulation. The modulation technique can maintain and produce the required reference voltage levels from the system. The implemented models are tested and verified within the MATLAB/SIMULINK. When we observe the results it produced minimized ripple contents at load side also reduced the THD values.

Keywords — *Capacitor voltage balancing, circulating current control, high-voltage direct current (HVDC) transmission, modular multilevel converter (MMC), modulation techniques, redundancy, variable-speed drive systems.*

I. INTRODUCTION

The modular multilevel converter (MMC) has become the most attractive multilevel converter topology for medium/high-power applications, specifically for voltage sourced converter high-voltage direct current (VSC–HVDC) transmission systems [1]–[14]. In examination with other multilevel converter topologies, the remarkable components of the MMC include: 1) its measured quality and versatility to meet any voltage level necessities, 2) its high productivity, which is of huge significance for high-control applications, 3) its prevalent consonant execution, particularly in high-voltage applications where countless sub-modules (SMs) with low-voltage evaluations are stacked up, in this way the span of detached channels can be decreased, and 4) nonappearance of dc-connection capacitors.

In the course of recent years, there has been a huge exertion towards tending to the specialized difficulties connected with the operation and control of the MMC and in addition widening its applications. The primary expectation of this audit paper is to give a superior comprehension of the MMC and its related specialized issues for different applications.

This paper gives an exhaustive audit on the latest advances and commitments on the operational issues, displaying, control, and balance methods of the MMC. This paper likewise highlights the rising uses of the MMC and layouts their related difficulties. Whatever is left of this paper is sorted out as takes after. Segment II presents the MMC circuit topology alongside different SM circuit arrangements that can be utilized as a part of the configuration of the converter.

This is trailed by an audit of most recent commitments on MMC tweak methods, outline limitations, and different operational issues, for example, capacitor voltage adjusting and circling current control introduced.

II. MMC TOPOLOGY

Fig. 1 shows a schematic chart of a three-stage MMC. The MMC, as appeared in Fig. 1, comprises of two arms for every stage leg where every arm contains N arrangement joined, ostensibly indistinguishable SMs, and an arrangement inductor Lo. While the SMs in every arm are controlled to produce the required air conditioning stage voltage, the arm inductor stifles the high-recurrence parts in the arm current.

The upper (lower) arm of three stage legs is spoken to by subscript "p" ("n"). The SMs of the MMC of Fig. 1 can be acknowledged by the accompanying circuits:

1) The half-scaffold circuit or chopper-cell [15], [16]: As appeared in Fig. 2(a), the yield voltage of a half-connect SM is either equivalent to its capacitor voltage vC (switched on/embedded state) or zero (exchanged off/avoided state), contingent upon the exchanging conditions of the complimentary switch sets, i.e., S1 and S2 [4].

2) The full-scaffold circuit or extension cell [15], [16]: As appeared in Fig. 2(b), the yield voltage of a full-connect SM is either equivalent to its capacitor voltage vC (exchanged on/embedded state) or zero (exchanged off/avoided state), contingent upon the exchanging conditions of the four changes S1 to S4. Since the quantity of semiconductor gadgets of a full-connect SM is twice of a half-connect SM, the force misfortunes and in addition the expense of a MMC in light of the full-connect SMs are essentially higher than that of a MMC taking into account the half-connect SMs [4].

3)The cinch twofold circuit: As appeared in Fig. 2(c), a cinch twofold SM comprises of two half-connect SMs, two extra diodes and one additional coordinated entryway bipolar transistor (IGBT) with its against parallel diode. Amid typical operation, the switch S5 is constantly exchanged ON and the clasp twofold SM acts equal to two arrangement joined half-connect SMs. Contrasted with the half-and full-connect MMCs with the same number of voltage levels, the clasp twofold MMC has higher semiconductor misfortunes than the half-connect MMC and lower than the full-connect MMC [4].

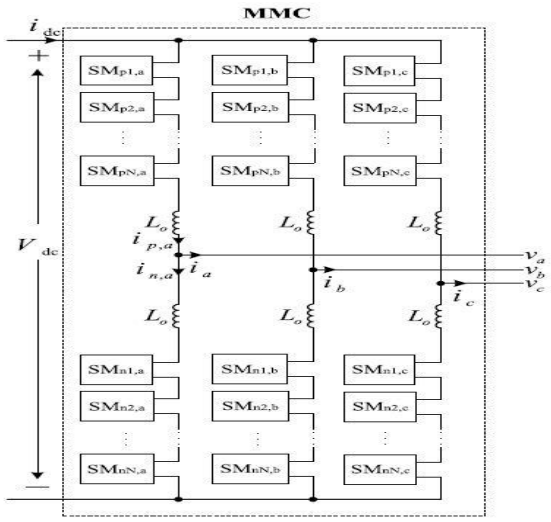

Fig. 1. Schematic Representation of the MMC.

4) The three-level converter circuit: As appeared in Fig. 2(d) and (e), a three-level SM is included either a three level nonpartisan point-clasped (NPC) or a three-level flying capacitor (FC) converter [17], [18].

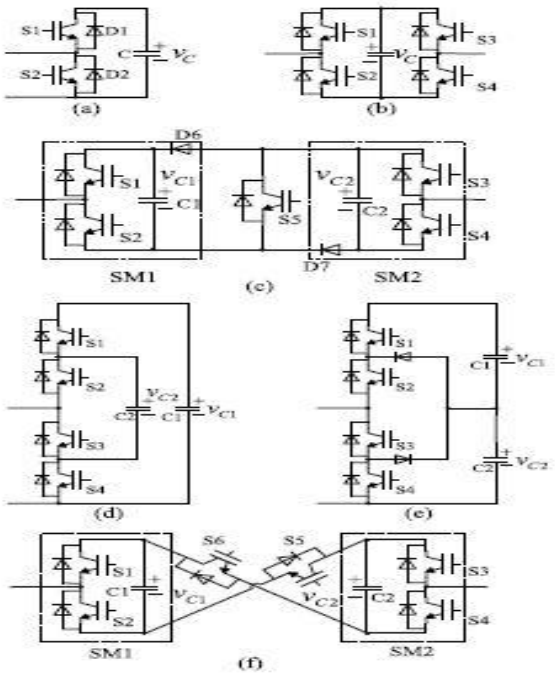

Fig. 2. Various SM topologies: (a) the half-bridge, (b) the full-bridge, (c) the clamp-double, (d) the three-level FC, (e) the three-level NPC, and (f) the five-level cross-connected SM.

The three-level FC MMC has the comparable semiconductor misfortunes with the half extension MMC. Then again, the three-level NPC MMC has higher semiconductor misfortunes than the half-connect MMC and brings down than the full-connect MMC. From an assembling viewpoint and control, this SM circuit is not exceptionally appealing.

5) The five-level cross-joined circuit: As appeared in Fig. 2(f), a five-level cross-joined SM likewise comprises of two half-connect SMs associated consecutive by two additional IGBTs with their against parallel diodes. Its semiconductor misfortunes are the same as the brace twofold SM [19].

A correlation of different SM circuits, as far as voltage levels, dc-side short out flaw taking care of ability, and force misfortunes, is given in Table I. The dc-side short out flaw is one of the significant difficulties connected with the MMC–HVDC

The SM circuit arrangements, the half-connect SM have been the most famous SM embraced for the MMC [1]–[12]. This is because of the vicinity of just two switches in the SM which brings about a lower number of parts and higher effectiveness for the MMC. Henceforth, the half-connect SM-based MMC is considered. It ought to be noticed that there are a couple of converter designs got from the MMC topology [15], [16]. This paper is just cantered around the supposed twofold star MMC design in [15], [16], which are shown in Fig. 1.

III.MODULATION, DESIGN, CONTROL, AND MODELINGOF THE MMC

A.Modulation Techniques

Various pulse-width modulation (PWM) techniques, based on using a single reference waveform, that have been developed/proposed for the MMC include:

1) Carrier-disposition PWM techniques (CD-PWM) [20], [21]:

These techniques require *N* identical triangular Carrier waveforms dislodged symmetrically as for the zero pivot.

The examination of the stage voltage reference waveform with the transporters delivers the craved exchanged yield stage voltage level.

Voltage moves relating to a triangular bearer are connected with the insertion/detour of a specific SM.

Based on the stage shift among the transporter waveforms, these systems are further characterized into:
a) Stage attitude (PD), b) stage restriction manner (POD), and c) interchange stage resistance aura (APOD), appeared in Fig. 3(a)–(c), individually. The disservices of utilizing these systems incorporate unequal conveyance of voltage swell over the SM capacitors that effect the consonant mutilation of the air conditioner side voltages and expansive extent of flowing currents.

To enhance the symphonies twisting of the air conditioner side voltages, a basic bearer pivot method [22], an altered transporter revolution strategy [23], or a sign turn procedure [20] is utilized to level the voltage appropriation over all the SM capacitors. Despite the proposed SM capacitor voltage adjusting methods, the yield voltages have a moderately high aggregate symphonies twisting (THD) [20]. To enhance the execution of these strategies, an altered PD PWM method with a SM capacitor voltage adjusting system is proposed in [8].

In this system, which depends on the PD bearer waveforms, voltage moves comparing to a triangular transporter are no more doled out to a specific SM. In this strategy, correlation of the reference waveform with the transporter waveforms creates a (N + 1)- level waveform that decides the quantity of SMs to be embedded in the upper and lower arms, separately. Contingent on the bearing of the arm current and the status of the SM capacitor voltages, the decided number of SMs out of the N SMs in the upper (lower) arm is embedded in order to minimize the distinction between the SM capacitor voltages. Mei et al. in [24] propose a PD PWM technique with specific circle inclination mapping system for adjusting the SM capacitors.

SM Circuit	Voltage Levels	DC-Fault Handling	Losses
Half-Bridge	0,Vc	No	Low
Full Bridge	0,+Vc	Yes	High
Clamp-Double	0,Vc1,Vc2,(Vc1+Vc2)	Yes	Moderate
Three Level Fc	0,Vc1,Vc2,(Vc1-Vc2)	No	Low
Three Level NPC	0,Vc2,(Vc1+Vc2)	No	Moderate
Five Level cross Connected	0,Vc1,Vc2,+(Vc1+Vc2)	Yes	Moderate

Table I Comparison of Various SM Circuits

This strategy executes bearer pivot utilizing the accompanying input: a) the most extreme/least SM capacitor voltages and b) the heading of arm current. The upsides of this procedure include: a) nonappearance of extra reference signs to control the SM capacitor voltages and b) simplicity of usage in a straightforward field executed entryway cluster (FPGA) even with an expansive number of SMs.

2) Sub harmonic methods [20]: In these procedures, there are 2N in distinguishable bearer for every stage leg, either saw tooth waveforms or triangular waveforms, with a stage movement of θ = 360◦/2N regarding one another, as appeared in Fig. 3(d) and (e). Expecting the same number of exchanging moves for both the PD PWM and sub harmonic procedures, the PD PWM strategy delivers better line to-line voltage THD [25], [26].

Furthermore, there are a few tweak procedures in view of utilizing different reference waveforms. These modulation strategies incorporate [27]:

1) Direct regulation: In this balance procedure, the upper and lower arm voltages of stage j are controlled by two corresponding sinusoidal reference waveforms, as given by.

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2}-v_{j,ref}}{V_{dc}} \quad (1a)$$

$$n_{n,j,ref} = N\frac{\frac{V_{dc}}{2}+v_{j,ref}}{V_{dc}} \quad (1b)$$

Where $v_{j,ref}$ speaks to the reference yield voltage and $n_{n,j,ref}$ and $n_{p,j,ref}$ are the reference waveforms for the quantity of embedded SMs in the upper and lower arms, separately. The reference waveforms in (1) are contrasted and the PD transporter waveforms, which fluctuate somewhere around 0 and N, to decide the required number of embedded SMs in the upper and lower arms. The real disadvantage of the immediate adjustment system is the vicinity of coursing streams, which expand the converter force misfortunes and rating estimations of the segments.

IV. MMC OPERATION UNDER SPECIAL CONDITIONS

A. Unbalanced Grid Conditions

The majority of the technical literature on modeling and control of the MMC primarily assume balanced system conditions [1]–[7], [9], [10], [12]. Control of the MMC under unbalanced grid conditions has been reported in [8], [9], [87]–[89].Under unbalanced grid conditions, the main control objectives are:

i) to keep the ac-side currents balanced by suppressing their negative-sequence components, ii) to regulate the net dc bus voltage, and iii) to control the circulating current and SM capacitor voltages. Saeedifard and Iravani [8] present a generalized PWM strategy to control the MMC under unbalanced grid conditions, in which the MMC dynamics can be visualized as two decoupled subsystems, the positive- and the negative-sequence subsystems; and each subsystem can be controlled independently.

The control strategy presented in [8], however, ignores the internal dynamics of the MMC and is only focused on the external dynamics. Furthermore, in the event of asymmetrical faults on the MMC side or in a transformer-less configuration, the zero sequence current components become present, which lead to the dc-bus voltage ripple.

Tu*et al.* [87] propose a dc-voltage ripple suppressing controller to remove the zero-sequence voltage components of the dc side under unbalanced grid conditions and to keep the net dc bus voltage constant. However, under unbalanced grid voltage, there is a double-line-frequency ripple in real power component.

In [88] and [89], the circulating currents are analyzed as three components: positive-, negative-, and zero-sequence circulating currents under unbalanced grid conditions. Moon *et al.* [88] propose a circulating currents control method with ac-side positive and negative-sequence current control to minimize the circulating currents and reduce the ac-side real power ripple under unbalanced conditions. In [89], based on the instantaneous power theory and by using a PR controller, a control strategy is proposed to eliminate the real power ripple and suppress the harmonics in the circulating currents.

Guan and Xu in [9] proposed a zero-sequence ac-side current controller, along with the positive- and negative-sequence ac-side current controllers, to operate the MMC–HVDC system with/without the interface transformer under unbalanced grid conditions. In [90], based on a notch filter and a proportional integral resonant controller, a control strategy is proposed to eliminate the dc power ripple by removing the harmonics in the zero-sequence circulating currents under unbalanced grid conditions.

B. Fault Tolerant Operation

As mentioned earlier, the structural modularity of the MMC adds to its redundancy and fault tolerance. In case of any component/SM failure, the failed SM needs to be detected and bypassed. When an open-circuit fault occurs, the output voltage and current of the MMC are distorted. Furthermore, the capacitor voltage of the failed SM may rise up, leading to further, vast destruction.

Given the large numbers of identical SMs and the symmetrical structure of the converter, locating a faulty SM is challenging if adding additional sensors to each SM and/or the converter is not desirable. The extra sensors add to the cost and complexity of the system. In [91], a sliding mode observer-based fault detection method has been proposed. The method, based upon the measured converter arm currents and the SM capacitor voltages, which are already available as the measurement inputs to the control system, detects and locates the faulty SM as well as Its failed switch.

V. PROPOSED SIMULINK SYSTEM

The implemented seventeen levels MMC simulink model is shown in below figure 3. This model consisted individual eight dc voltages and three universal bridges for each phase. The dc voltage sources are acts as an input system and the universal bridges IGBT's are acts as an inverter to convert dc system voltage into ac system voltages by utilizing Pulse Width Modulation Technique.

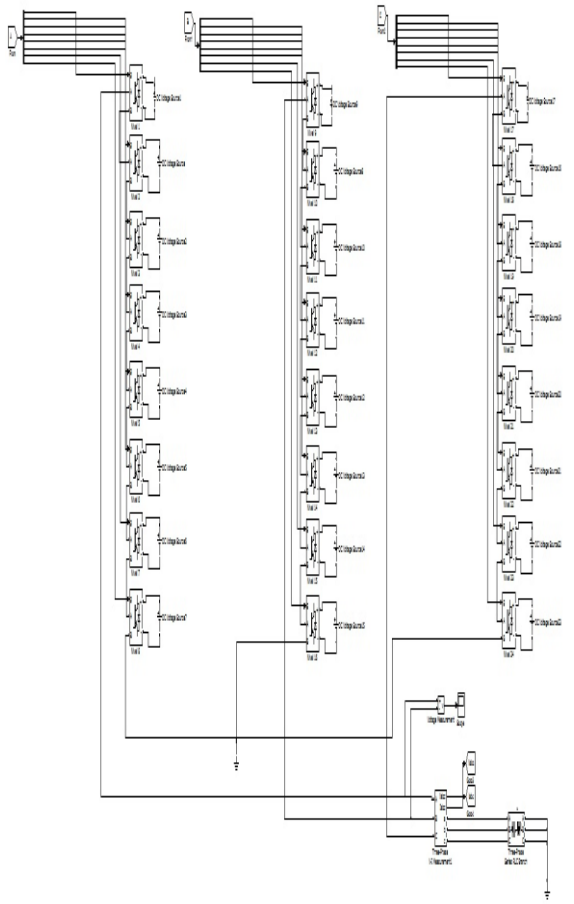

Fig 3: Proposed Seventeen Level Simulink Model

PWM technique process it utilized three phase voltage which is given to PLL block for to maintaining the phase voltages and phase sequences, from this module we can find the teeta variable and it is forwarded to mathematical operators. The sin and cos mathematical functions are provided for generate the phase angles from the teeta parameters.

These phase angles are connected to function block where the signal is converted to our general input formatted signal. Finally this is compared by the required reference values under constant values, the multi port switch which is passing through the input signals corresponding to the truncated value of the first input signal. Finally it can generate the firing pulses for the IGBT'S. The pulse width modulation technique is shown in fig 4 and fig 5.

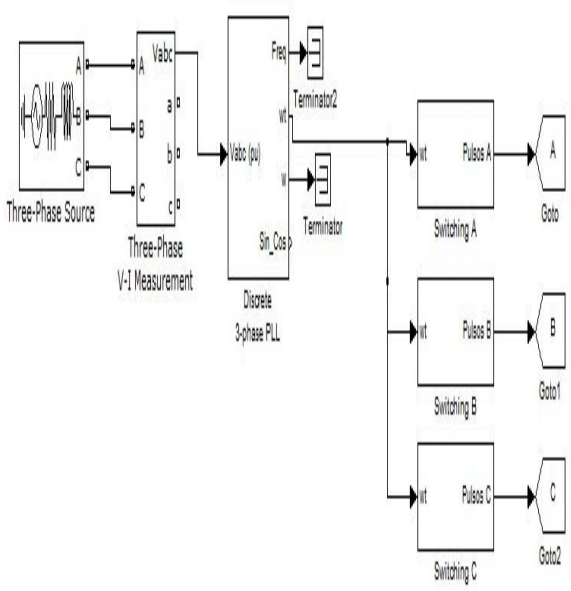

Fig 4: Pulse Width Modulation technique

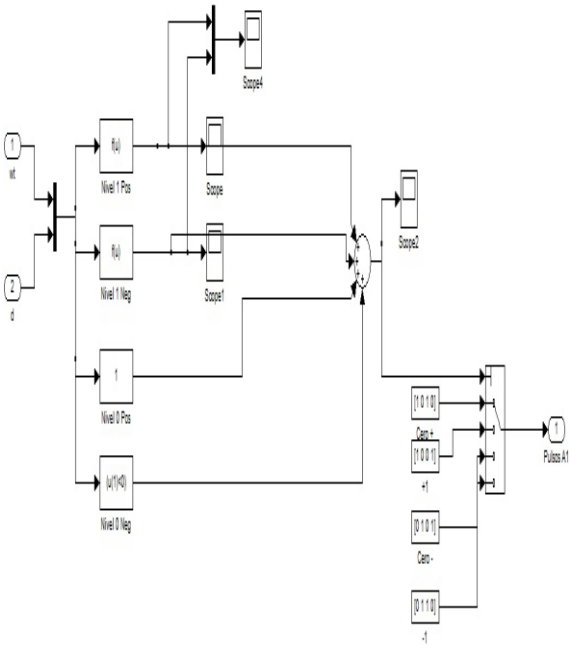

Fig 5: Pulse Width Modulation Technique Firing Pulse Generation Process

The generated firing pulses connected to the IGBTs these are triggered by these pulses and convert the dc voltages into required ac voltages. The three phase voltage measure is provided for to measure the three phase voltage currents. The generated voltage is transfer to the loads.

The generated results are shown in below figure. Fig 6 shows the individual phase voltages for the seventeen levels converter. Fig 7 shows the generated three phase voltage and current from the seventeen levels MMC. The generated output voltage is identified from the mathematical formula

is m=2(n+1); where m is denoted by generated output voltage levels representation & the n is denoted by the number of utilization of dc sources.

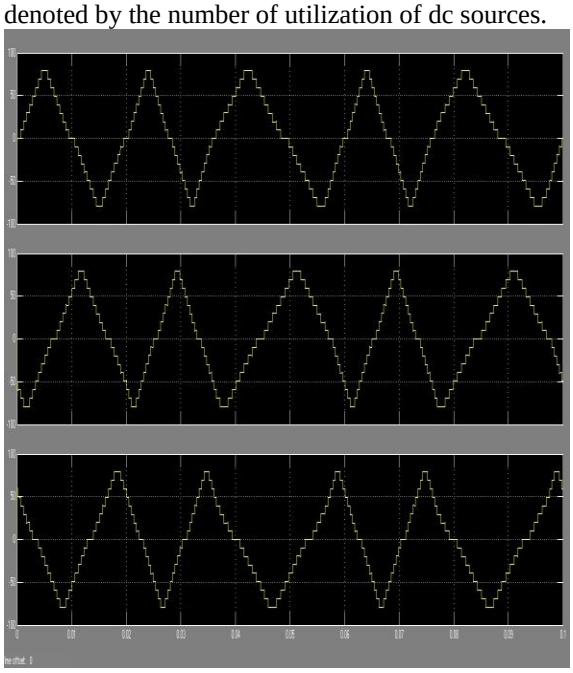

Fig 7: Individual Phase Output Voltages From The Seventeen Level MMC

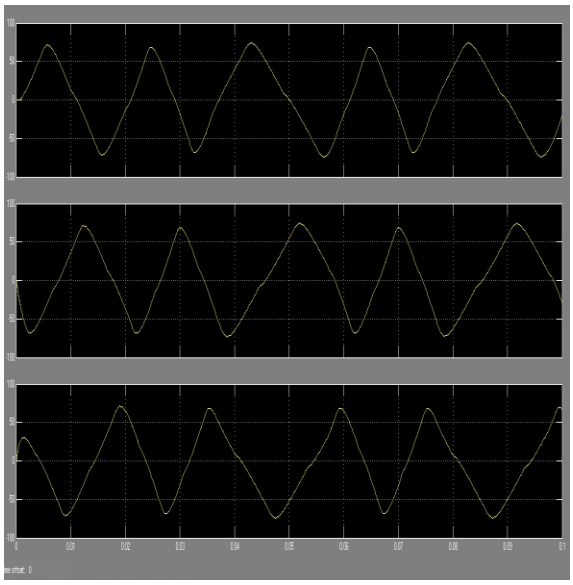

Fig 8: Individual Phase Output Currents From The Seventeen Levels MMC

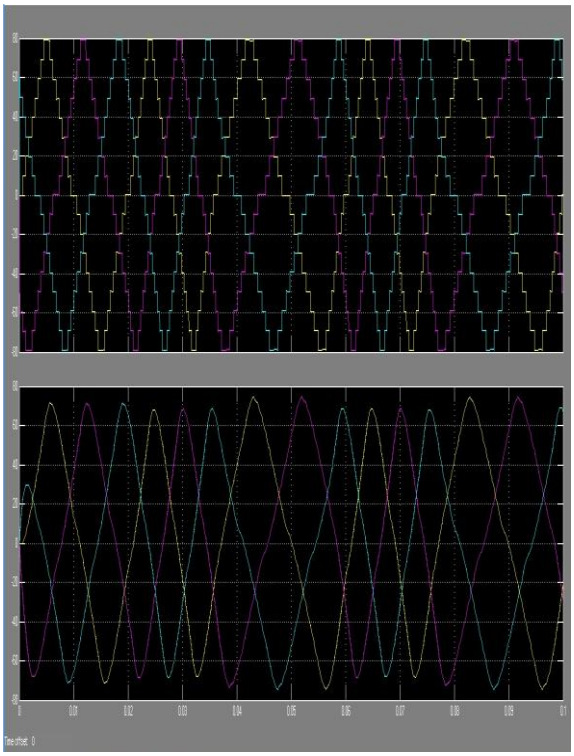

Fig 9: Output Voltage & Current from the Seventeen levels MMC model

The generated output results from the seventeen levels MMC given in above figures. When we observe these results the converter can produced less THD values. The seventeen level converters produces THD values as 0.0105.

IV. CONCLUSION

The striking elements of the MMC, i.e., its particularity and adaptability empower it to thoughtfully meet any voltage level necessities with unrivaled consonant execution lessened rating estimations of the converter segments and enhanced productivity. In the course of recent years, the MMC has turned into a subject of enthusiasm for different medium to high voltage/power frameworks and modern applications including HVDC transmission frameworks, FACTS, medium-voltage variable-velocity drives, and medium/high voltage dc–dc converters.

For force framework applications, e.g., HVDC frameworks and FACTS, the MMC has come to a sure level of development and appears to remain as the most encouraging innovation as various MMC–HVDC frameworks and STATCOMs has been effectively executed and introduced.

For medium-voltage variable-velocity drives, there is still a lot of space for further improvement to address the operational and control issues of the MMC, particularly under consistent torque low-speed operation.

One noteworthy issue that should be tended to will be to minimize the greatness of the capacitor voltage swell of the converter SMs at low frequencies without yielding the converter effectiveness, consequently making a sensible tradeoff between the converter size/volume/expense and proficiency.

The presentation of a group of particular multilevel dc–dc converters, began from the MMC topology, has opened up another parkway on innovative work of medium/high voltage dc–dc converters. To exploit these converters for different applications, propelled balance techniques that empower high-voltage transformation proportion, high productivity and diminished segment hassles are required.

With a lot of MMC-inferred converter topologies and applications, it is presumed that improvement of novel tweak and control procedures will be a noteworthy driving element to shape the eventual fate of MMC applications. The designed seventeen levels model tested and verified within the simulation with less THD under pulse width modulation technique.

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