An innovative technique on Low Power Leakage Reduction in CMOS circuits using Sleep transistors
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ABSTRACT

In CMOS technology, Static power dissipation is the most important concern despite of more power dissipation is caused by leakage power, the percentage of dissipation becomes increasing with respect to scaling in technology. In conjunction with technology scaling down and advanced working speeds of VLSI expertise, the leakage power is getting improved. In this paper, two newly renovated circuits are introduced for reducing the leakage power in the inverter circuit. The power dissipation during sleep mode of operation can be considerably concentrated related to usual power gating methods by these methods. The proposed system is practiced to the desired circuits and the consequences are compared with previous leakage minimization approaches. An important phenomenon called Inverter buffer chains are intended using a novel state maintenance low leakage practice and established to low power dissipation circuits. Entirely, the whole systems are demonstrated and simulated in cadence design tools for 90 nm CMOS process technology. The features such as state retention, power dissipation and leakage current are good when compared with former leakage power reduction approaches.

Keywords: Static power dissipation, leakage power, Inverter buffer chains, state retention.

1. INTRODUCTION

Nowadays, in the history of VLSI, a fundamental challenge and critical issue in electronics industry is control and management of power consumption. The advancement in VLSI technology allows integrating a complete system on chip (SoC) providing facility to develop a portable system. The power consumption is the major concerns in VLSI design, the excessive power dissipation in design depress their use in movable devices. The device planning is developed more stimulating work for VLSI circuit designer as the power ingestion turn out to be a major distress which prominent to reduces the battery life as because of decrease in feature size and resultantly implements in the chip density and operating frequency. The development in scaling technology raises transistor leakage power extravagantly, as power consumption or degeneracy improvement leads to humiliation in performance and reduces the design life time. In CMOS design the sources of power consumption mainly due to dynamic power dissipation and leakage power dissipation. The power consumption can be expressed in equation as below:

\[ P_{\text{TOTAL}} = P_{\text{STATIC}} + P_{\text{DYNAMIC}} \] (1)

Where

- \( P_{\text{TOTAL}} \) is the total power consumption,
- \( P_{\text{DYNAMIC}} \) is the dynamic power consumption due to switching of transistors;
- \( P_{\text{STATIC}} \) is the static power consumption.

From the above equation, it is confirmed that the dynamic power comprises of swapping power and short circuit power; this cannot be entirely removed because of calculating action. The static power consumption i.e. the leakage power dissipation has become an important share of total power consumption, it is the power dissipation due to leakage current which flows through a transistor when no transaction occurs and transistor is in steady state, depending on the gate length and breadth of oxide layer. The numerous methods appraised to decrease the leakage power in CMOS VLSI design. Through dropping channel length for uninterrupted technology groups, threshold voltage and gate oxide depth are also being mounted down. Leakage current subsequently increases exponentially with
reduction in threshold voltage. The leakage current is going to be a limiting factor for successive scaling down of transistors. Due to the smaller feature sizes in nanometer technologies, shorter channel lengths cause sub threshold current to increase when the transistor is in the off state. The lower sub threshold voltage contributes increase to increased sub threshold current as well, because transistors cannot be turned off absolutely. Since with every consecutive technology the number of transistors per given area is on a rise, the leakage power in an integrated circuit for continual generations is growing, because transistors leak even when they are not triggered and substantial power dissipation takes place even during inactive state of circuits.

The parameter of the system such as subthreshold voltage is becoming downwards to retain pace with decreased supply voltage for top down technologies so as to have worthy performance. The lower subthreshold voltage in the recent technologies gives rise to improved leakage current because transistors cannot be swapped off absolutely. Subthreshold current is the drain to sourceleakage current when the transistor is off. Leakage current performs as a controlling factor for additional scaling down oftransistors as per the International Roadmap for Semiconductor Technology. Thus it is important to reduce leakage (static) power consumption for the duration of the idle or standby states of the circuits.

For a CMOS circuit, the total power dissipation contains dynamic and static modules during the active mode of operation. In the reserve mode, the power dissipation is due to the standby leakage current. The dynamic power (P_D) and leakage power (P_LEAK) are stated as

\[ P_D = \alpha f C V^2 \]  \hspace{1cm} (2)

\[ P_{LEAK} = I_{LEAK} V \]  \hspace{1cm} (3)

where

- \( \alpha \) is the switching activity,
- \( f \) is the operation frequency,
- \( C \) is the load capacitance,
- \( V \) is the supply voltage and
- \( I_{LEAK} \) is the cumulative leakage current due to all the components of the leakage current.

In this system, the leakage current is the sub threshold or weak inversion current that drifts from drain of a transistor to its source when the transistor is off. Hence, the subthreshold leakage current can be condensed by accumulative threshold voltage VTO, increasing VSB and reduction of VGS, VDS and dropping the temperature. In profound submicron CMOS circuits, the lessening in leakage current has to be attained using both process- and circuit-level methods. At the progression level, leakage reduction can be accomplished by monitoring the dimensions and doping summary in transistors. At the circuit level, threshold voltage and leakage current of transistors can be effectively controlled by controlling the voltages of different device terminals.

2. RELATED WORK

Kaushik Roy et. al proposed Leakage Current Mechanisms and Leakage Reduction Techniques in Deep Sub micrometer CMOS Circuits. In this paper, they demonstrated High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. This paper reviews various transistor intrinsic leakage mechanisms, including weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling. Channel engineering techniques including retrograde well and halo doping are explained as means to manage short-channel effects for continuous scaling of CMOS devices. Finally, the paper explores different circuit techniques to reduce the leakage power consumption.

L. Wei et.al proposed Design and optimization of dual threshold circuits for low voltage low power applications. In this paper, they explained Reduction in leakage power has become an important concern in low-voltage, low-power, and high-performance applications. In this paper, we use the dual-threshold technique to reduce leakage power by assigning a high-threshold voltage to
some transistors in noncritical paths, and using low-threshold transistors in critical path(s). In order to achieve the best leakage power saving under target performance constraints, an algorithm is presented for selecting and assigning an optimal high-threshold voltage. A general leakage current model which has been verified by HSPICE simulations is used to estimate leakage power. Results show that the dual-threshold technique is good for leakage power reduction during both standby and active modes. For some ISCAS benchmark circuits, the leakage power can be reduced by more than 80%. The total active power saving can be around 50% and 20% at low- and high-switching activities, respectively.

S. Mutoh et.al proposed 1-V power supply high-speed digital circuit technology with multi threshold voltage CMOS. In this paper, they explained 1-V power supply high-speed low-power digital circuit technology with 0.5-/spl mu/m multi threshold-voltage CMOS (MTCMOS) is proposed. This technology features both low-threshold voltage and high-threshold voltage MOSFET's in a single LSI. The low-threshold voltage MOSFET's enhance speed performance at a low supply voltage of 1 V or less, while the high-threshold voltage MOSFET's suppress the stand-by leakage current during the sleep period. This technology has brought about logic gate characteristics of 1.7-ns propagation delay time and 0.3-/spl mu/m MHz/gate power dissipation with a standard load. In addition, an MTCMOS standard cell library has been developed so that conventional CAD tools can be used to lay out low-voltage LSIs. To demonstrate MTCMOS's effectiveness, a PLL LSI based on standard cells was designed as a carrying vehicle. 18-MHz operation at 1 V was achieved using a 0.5-/spl mu/m CMOS process.

ManashChanda et.al proposed Analysis of NAND/NOR gates using sub threshold adiabatic logic (SAL) for ultra-low power applications. In this paper, in depth analysis of the NAND/NOR gates in the weak inversion regime using sub-threshold adiabatic logic (SAL) has been analyzed. As either pull up or pull down network in SAL, silicon area can be reduced significantly. The analytical expression of the power dissipation, leakage energy dissipation, and maximum and minimum output voltages is detailed here. Also the analytical expression of the optimum supply voltage and the frequency are given for the analysis. Extensive CADENCE simulations have been done to verify the analytical expressions. Simulated results are well matched with the analytical value which validates the acceptability of the proposed structure in the sub-threshold regime for the ultra-low power application.

Flavio Carbognani et al proposed Two-phase clocking combined with sleep transistors reduces active leakage in low-frequency portable applications. In this paper, the aggressive down-scaling in semiconductor devices implies the transistor voltage threshold reduction, which is associated with an exponential increase in sub-threshold leakage currents. For this reason, static power consumption is becoming the major issue of the newer technologies. A novel low-leakage technique (2Phi+sleep), which combines levelsensitive two-phase clocking (2Phi) with sleep transistors (sleep), is proposed and compared to the state of the art. The results of transistor-level simulations indicate that the proposed technique reduces active leakage (~22% in the evaluated design in a 90 nm process), while preserving the same capabilities of counteracting stand-by leakage as conventional sleep transistors.

3. LOW LEAKAGE POWER REDUCTION TECHNIQUES FOR POWER DISSIPATED CIRCUITS

The main source of an operation is the power consumption in the desired device. Devices which are functioned on battery are either Sleep or Active mode. Leakage power can be divided in to two groups based on these two modes such as Leakage Control in Sleep Mode and Leakage Control in Active Mode. In sleep mode, the techniques like Power gating and super cutoff CMOS are used for leakage reduction in standby mode. In these techniques, circuit is cutoff from the supply rails, when it is in idle state. In Leakage Control in Active Mode, the techniques like forced stacking and sleepy stack can be used during the run time or active mode for leakage current reduction.

3.1 SLEEPY INVERTER APPROACH

The sleepy inverter delivers a worthy leakage power reduction to the circuit.
Nevertheless, when it comes in to sleepmode it drops the state information. Hence this valuable Sleep transistor method can be developed to the circuits which have pull down principle of the inverter.

A method which has been used to improve the power dissipation by the leakage reduction technique is known as sleepy keeper technique. Sleepy Keeper approach announces extra keeper transistors to the sleep transistor technique to sustain the state of the circuit. It has been determined this circuit procedure has occasioned in large dynamic power dissipation. Multiple powers gating technique of maintains the state but has large related power consumption. Sleepy keeper method uses the traditional sleep transistors with two additional transistors to protect state during sleep mode. Dual threshold voltages can also be smeared in the sleepy keeper approach to reduce sub threshold leakage current.

4. NOVEL LOW POWER LEAKAGE TECHNIQUES

The novel technique for low leakage operation of an inverter is mainly concentrated on the power leakage of the gates of the circuit. This innovative sleepy inverter however offers good leakage power reduction; the voltage levels at the output are not at good logic 1 and logic 0 values. Hence, this larger reduction in leakage power can be employed in inverter chains which are used in peripheral circuits of SRAM memory systems.

There are two novel low leak circuit methods for logic gates are suggested as follows as:

- Firstly, an ultra-low seepage power reduction method with lowermost leakage power with lower output voltage strike during active mode of process.
- Secondly, state retention low leakage technique LPSR with four modes of operation, viz. Active mode, Deep Sleep mode, State Retention with good 1 and State Retention with good 0.

4.1 ULTRA-LOW LEAKAGE POWER REDUCTION TECHNIQUE

The Ultra-Low leakage logic gate makes use of PMOS transistor as the pull down sleep transistor and NMOS transistor as the pull up sleep transistor.
Fig. 3: Novel Sleepy Inverter technique

- **Active mode**: In active mode of process the sleep signal is detained at logic 0 value and sleep-bar signal is held at logic value 1 so that both sleep transistors are on. Consequently the current though the circuit decreases and power dissipation originates down. The gate has accurate functionality but higher logic low and concentrated logic high output levels. The power dissipation thus reduces.

- **Sleep mode**: In sleep or standby mode of process the sleep signals are paired of active mode of operation. Now Signal is completed logic 1 and signal is made logic 0. Sleep Transistors are off, actual power and ground path is destroyed, the off resistance increases and leakage current is lowered. The current flowing through the circuit comes down significantly.

4.2 LOW POWER STATE RETENTION TECHNIQUE

The low power state retention technique is demonstrated above. The ultra-low leakage gate can be better to accelerate good logic levels for the period of active mode of process by using a conservative sleep transistor both across pull down and pull up paths of logic gate. The unique low leak sleepy inverter still affords excellent low leakage power operation, has ruined output voltage levels during active mode of operation.

Fig. 4: State Retention Inverter

The inverter output is also not at good logic levels. During sleep (standby) mode of operation, the last output state is also not retained. To report these disputes, a state retention transistor is associated in similar to the sleepy transistors in the circuit of low leak sleepy inverter. Through sleep mode of operation sleep signals are held at logic 1 and 0 values correspondingly. Both the pairs of sleep transistors are off and later reduced leakage current and lower power dissipation.

5. SIMULATION AND RESULTS

Simulations have been accomplished using virtuoso (cadence) in 90 nanometer (nm) CMOS technology with supply voltage 1.2V to estimate power consumption. The static power consumption and dynamic power consumption measured for different design techniques. Simulation of inverter with sleepy transistor technique and the input and output waveform of this simulation results are shown in fig 5 and 6. Simulation of inverter with sleepy keeper technique and its input and output waveform are shown in fig 7 and 8.
Fig. 5: Inverter with Sleep Transistor Technique

Fig. 6: Input and Output waveform of Inverter with Sleep Transistor Technique.
Fig. 7: Inverter with sleepy keeper technique

Fig. 8: Input and output waveform of inverter with sleepy keeper technique
CONCLUSION

The low leakage power dissipation is the most important concern for many proposals in nanometer technologies. As the technology scaling goes below 90nm, the backup leakage power dissipation has turn out to be a precarious matter. Due to this indomitable issue, the leakage power is of great worry for designs in the field and is charming a major provider to the total power consumption; leakage power has turn into more prevailing when compared with Dynamic power. The state retention inverter has brought about in good leakage power drop as well as the former output state can be reserved. The gate leakage has become leading sources of leakage and is estimated to increase with the technology mounting. The results for leakage power dissipation or reduction of leakage power dissipation have to be required both at the process technology and circuit levels. The leakage power during sleep is also minor and state retention can also be accomplished at good logic levels. The Total power dissipation is smallest. Subsequently single threshold transistors are used in all the schemes to accomplish low power the innovative methods provide new choice to the designers of low power logic gates.

REFERENCES


