Design of A Low Power 16- Bit CSLA Using Binary To Excess-1 Converter

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Abstract: *For math functions , the fastest adders used is Carry Select Adder (CSLA) in many data processors. CSLA is an Application Specific Integrated Circuit (ASIC) developed by modifying the CSLA Regular Square Root Structure (SQRT). The main goal is a poster design that has less space and strength compared to the regular CSLA SQRT to assess the proposed design performance in terms of area and power with logical voltage and custom design. However, CSLA is not effective in the region because it uses multiple pairs of corrugation load additives (RCA) to generate a partial amount and a conversion taking into account the input entry then the final sum and the conversion specified by the multiplexers. The basic idea of this synthesis is to use BEC as an alternative of a RCA with a regular CSLA to achieve lower power and region consumption. Despite the delay, CSLA is more beneficial in that it requires low power and area consumption. The proposed design was developed using Verilog-HDL and compiled into XILINX ISE 14.7 Software Tool.*

Keywords: *Binary to Excess-1 Converters (BEC), Carry Select Adder (CSLA), squareroot (SQRT) CSLA architecture, Low power, Ripple Carry Adder(RCA).*

I. INTRODUCTION

Most IC engineering students are exposed to ICs at a very basic level, including SSI (small-scale integration) circuits such as logic gates or MSI (medium-sized integration) circuits such as multiplexers, valence codes, etc. But there is a world Much larger involves miniaturization at levels so large that micrometer and microseconds are literally huge! This is the world of VLSI: large-scale integration. VLSI refers to "broadband integration". In recent years, CMOS circuit power consumption has become an important design consideration for a VLSI system. On VLSI systems, power consumption includes dynamic power and static power consumption. Most of the power consumption of any VLSI system consists of dynamic power consumption. In addition, the trends of the MOSFET scale are driving development toward nanoscale operations as motivated by Moore's Law. With these developments, leakage currents are also increasing, and the constant energy component of the energy dissipation plays a vital role in the total energy consumption. Static energy dissipates primarily due to source and drain leakage currents, and the loose terminal control of the CMOS provides improved performance in terms of energy dissipation and delay. The aim of this thesis is to design a high-speed adherent with low energy and a smaller area as a primary consideration for optimizing circuit level design to reduce energy consumption in CMOS circuits. Complete assembler design with low energy consumption and low delay. It is an Adder Selection Adder (SQRT CSLA) and the Add Selection Adder was developed.

II. 16 BIT REGULAR CSLA

Two ripple carry adders and a multiplexer and multiplexer combination results a carry-select adder.For addition of two n-bit numbers with the two ripple carry adders where Cin=0 and Cin=1.The delay o$\sqrt{n}$ is calculated from uniform sizing, anywhere the best number of FA elements per block is identical to the square root of the number of bits being added, because that will yield an equivalent number of multiplexer delays. The block diagram of a 16-bit regular SQRT CSLA as shown in Fig.1.The final carry out is calculated is used to select the actual calculated values of the output carry and sum with the help of MUX.

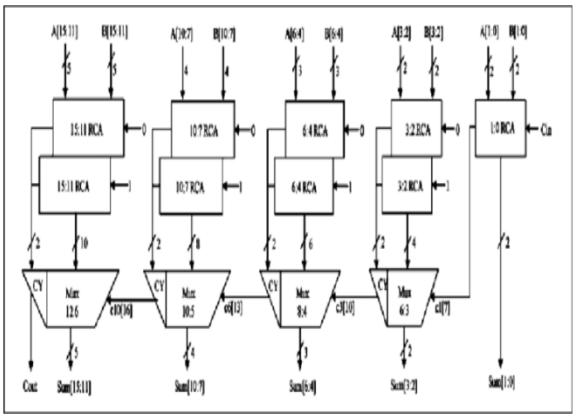

Figure 1:16 bit CSLA

The problem in CSLA design is the number of full adders are increased then the circuit complexity is also increases. The number of full adder cells is more there by power consumption of the design also increases. Number of full adder cells doubles the area of the design also increased. A parallel RCA with carry input equal to 1 is overcome by BEC.

III. BINARY TO EXCESS CODE

For high speed processors and systems, is achieved by high speed addition and multiplications, where as the limitation of any adder is that it generates carry. To improve the speed of addition , we proposed a BEC using n-bit to. To attain the low power and area using carry select adder. The advantage of BEC consists of less gates than n-bit RCA. The 4 bit BEC as shown in figure 2 and the truth table is as shown in table 1.

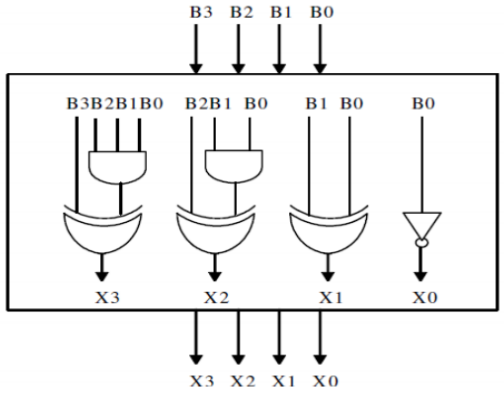

Figure 2: 4 bit BEC

The expressions of 4 bit BEC are

X0=~(B0)

X1=B0 Xor B1

X2=B2 Xor (B0 & B1)

X3= B3 Xor (B0 & B1 & B2)

Table 1: Truth table of BEC

B [3:0]	X [3:0]
0000	0001
0001	0010
.	.
.	.
.	.
1110	1111
1111	0000

IV. 16 BIT CSLA USING BEC

The fundamental idea to use Binary to Excess-1 converter (BEC) replaces RCA , Cin=1 in traditional CSLA in order to reduce the area and power. SQRT CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and power. Regular SQRT CSLA also uses dual RCAs. In order to reduce the delay, area and power, the design is modified by using BEC instead of RCA with Cin=1. The circuit of basic 16 bit CSLA as shown in figure 3.

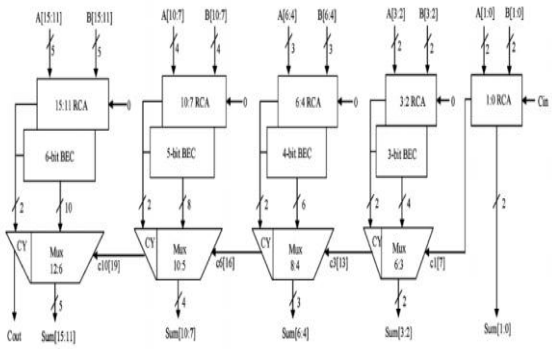

Figure 3:16 Bit CSLA using BEC

V. SIMULATION RESULTS

The implemented Design of 16-bit CSLA Using BEC has been simulated using Xilinx 14.7 software and the results are compared with regular Carry Select Adder using RCA. The modified CSLA structure decreases the power consumption & Area. The area can be reduced by using BEC structure instead of RCA.

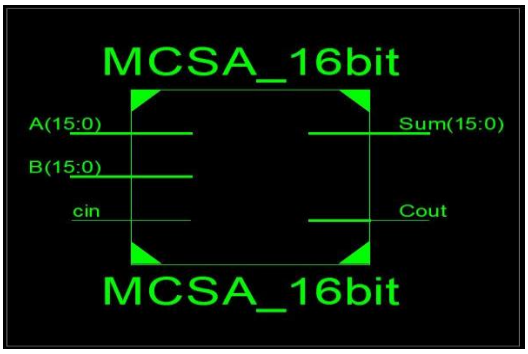

Figure 4: 16- bit CSLA Using CSLA

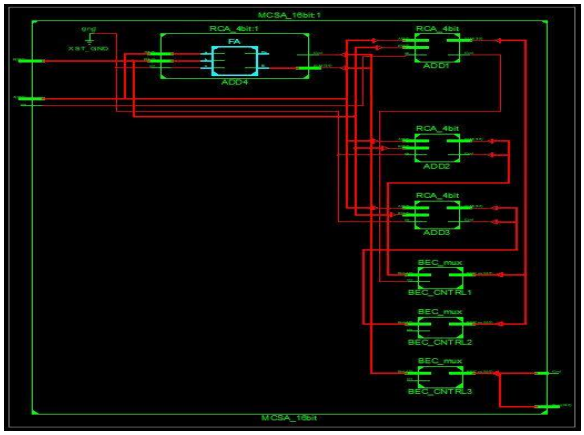

Figure 5: RTL Schematic of 16 BIT CSLA Using BEC

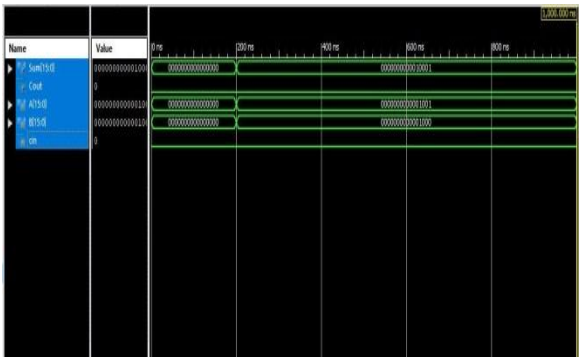

Figure 6: Simulation waveform for 16 -bit CSLA

Table 2: comparison in terms of power

Parameter	Regular 16 bit CSLA	Modified 16 bit CSLA
Power(watts)	1.9u[2]	0.081n

The power analysis of the 16-bit Lower Power Modified CSLA system as compared with a Regular (original) 16-bit CSLA taking a reference from [2] Low power & Area efficient Carry Select Adder using CMOS Technology is bit faster.

VI. CONCLUSIONS

In this paper, the 16 bit SQRT CSLA is developed and simulated using Xilinx and X-Power analyzer , the amount of power and the area is reduced by nearly 50% . Whereas modified CSLA reduces the area and power when compared to standard CSLA with enhance in delay by the use of Binary to Excess-1 converter.

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