PERFORMANCE COMPARISON BETWEEN ULTRA LOW POWER ALU WITH CMOS AND GDI TECHNIQUES

Vanajeswari Imandi[#1], Nagalakshmi Harisha A[*2]

[#] *PG scholar, Department of Electronics and Communication Engineering*
Ramachandra College of Engineering, Eluru, Andhra Pradesh, India

**Assistant Professor, Department of Electronics and Communication Engineering*
Ramachandra College of Engineering, Eluru, Andhra Pradesh, India

Abstract

The ALU is one of the most fundamental operational units in any processor. The ALU can be characterized as the combinational unit, which is utilized to play out its intelligence and number juggling units. This paper presents a low power rapid Arithmetic Logic Unit (ALU) in 14 nm technology utilizing Multi-limit voltage semiconductor logic and Gate Diffusion Input procedure. Its presentation is contrasted and regular CMOS method. The reproduced outcomes uncovered better execution attributes of different number juggling and logic elements of a 1-piece ALU utilizing VTV and GDI procedures contrasted with customary CMOS strategy. This procedure permits diminishing power scattering and deferral while keeping up the low intricacy of logic design.

Keywords — *VTV technique, GDI, ALU, Digital Design.*

I. INTRODUCTION

Gate Diffusion Input is another procedure for lessening structure limitations like power and area. As of late, low power, less area, and fast are the primary design combinational for designing the circuits in any industry. The power utilization is the fundamental design objective in any electronic gadgets, for example, mobiles, workstations, TV applications, which limits in both high and low framework execution power utilization, which is one of the cutoff points in both high and low framework execution. In this manner, this spurs us for the design of circuits with low vitality utilization.

ALU is one of the primary parts of a microchip. CPU fills in as a cerebrum to any framework, and ALU functions as a mind to CPU. Number-crunching activities are essential capacities and fundamental for designing any low power, fast applications, for example, computerized signal handling, picture preparing, microchip. In this paper, the Addition, Subtraction, AND, OR, XOR, and XNOR logic circuits are executed utilizing the GDI method.

II. GATE DIFFUSION INPUT TECHNIQUE

A solitary PMOS and NMOS semiconductor are utilized to plan an essential GDI cell; the GDI structure is like CMOS. The distinction between the CMOS and GDI based plan is that the wellspring of the PMOS in a GDI cell isn't associated with VDD, and the wellspring of the NMOS isn't associated with GND. This component gives the GDI cell two additional information pins for the use, which makes the GDI plan more adaptable than the CMOS structure. Majority of both NMOS and PMOS are associated with N and P separately

GDI cell comprises of three sources of information
- •G (basic door contribution of NMOS and PMOS)
- •P (contribution to the source/channel of PMOS)
- •N (contribution to the source/channel of NMOS).

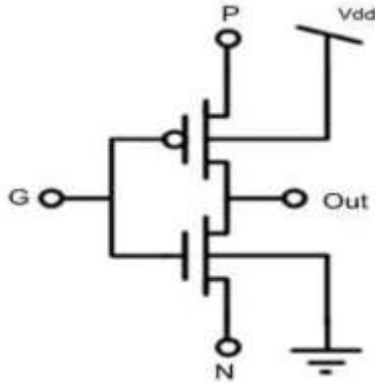

Figure 1: Basic GDI cell with inputs G, P and N

III. EXISTING METHOD

The current fulladder configuration is actualized by utilizing 14 semiconductors, as appeared in Fig. 2. It comprises, for the most part, five logic blocks one XOR/XNOR, two multiplexers, one Swing Restored Transmission Gate (SRTG), and the other one is Swing Restored Pass Transistor (SRPT) square. The XOR/XNOR square is structured utilizing the GDI method since the way of the inverters utilized in the XOR/XNOR blocks has no voltage drop. They are consolidated with standard VT gadgets. The convey input (Cin) is created by the GDI MUX-1, which multiplexes the yield of the XOR and the XNOR to

get the whole capacity. The GDI MUX-2 multiplexes the data sources Cin and B with a control line from the yield of XNOR logic (A XNOR B) to get convey output(Cout).

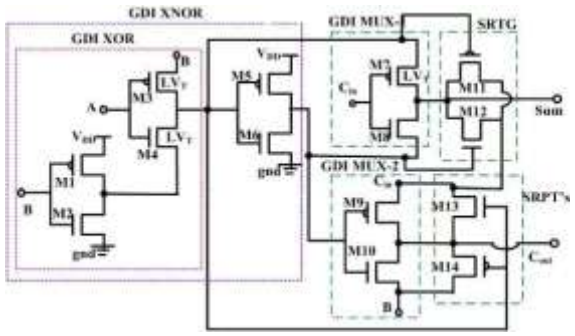

Figure 2: Existing 14T VTV-GDI hybrid full adder design

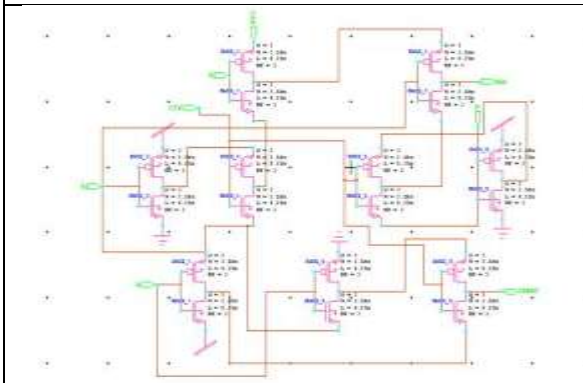

Figure 3. Existing 14T MVT-GDI hybrid full adder design Schematic

However, the existing structure is similar to many previous XOR/XNOR logic-based designs; the full swing is ensured using an SRTG at the output of the sum and SRPT's at the carry output (Cout). The swing restoration transistors (M11, M12, M13, M14) are 'ON' when there is a VT drop at the output of the sum generation GDI MUX1 and Cout generation GDI MUX-2 to provide full swing logic.

IV. PROPOSED METHOD

In the proposed method, we can see that the operating circuits at ultra-low voltage, the transistors are in the sub-threshold weak-inversion region. The power and area are the major problems in ALU implementation. Hence low power logic design style that is GDI is used. The reduction of the transistor logic functions has greatly reduced the power and delay. The sizing of the transistors also helped in reducing the power and delay.

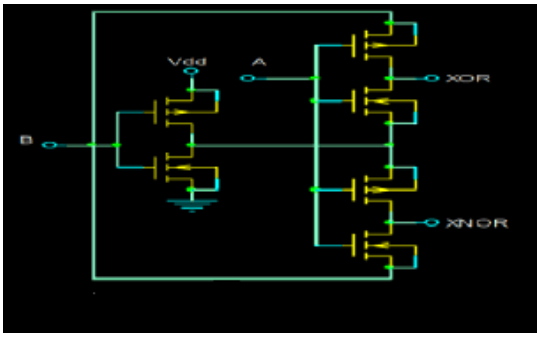

Figure 4. XOR and XNOR based GDI

XOR gate, also pronounced X-OR gate, results in a 0 if both the inputs are 0 or if both are 1. Otherwise, the result is 1. This figure shows the logic of the XOR gate similarly in XNOR gate based GDI; when AB = 01, the NMOS transistor is switched OFF, and the PMOS transistor is switched ON. When AB = 00, the PMOS transistor is switched ON, and the NMOS transistor is switched OFF.

Full adder based GDI

The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, where

Sum = (A XOR B) XOR Cin

Cout = A AND B + Cin (A XOR B)

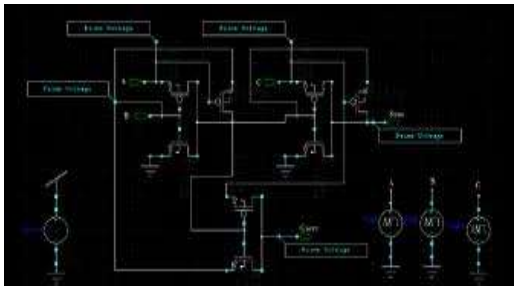

Figure 5. 1-bit 8T Full Adder based GDI.

Figure 5 shows the circuit of eight transistor 1-bit full adder cell. The Sum output is basically obtained by a cascaded exclusive OR gate of the three inputs. The cout module is implemented using a 2T multiplexer. It is quite evident from Figure 1 that two-stage delays are required to obtain the sum output, and at most two-stage delays are required to obtain the carry output. The voltage drop due to the threshold loss in transistors M3 and M6 in Figure 3 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of |VT p| provided by the PMOS pass transistor M3 when a=0 and b=0 is used to turn on the NMOS pass transistor M8and, therefore, we get an output voltage equal to |VTp |-VTn, where VTp is the threshold voltage of the PMOS transistor and VTn is the threshold voltage of the NMOS transistor

Full Subtractorsubtractor based GDI

A full subtractor is one of the modules used to design the ALU of a processor. The subtraction of two binary numbers is done by taking the complement of the subtrahend and adding it to the minuend. The full-subtractor is a combinational circuit that is used to perform subtraction of three bits. It has three inputs, A (minuend) and B (subtrahend) and Bin (borrow -in), and two outputs, D (difference) and Bout (borrow-out). Full Subtractorsubtractor using GDI is as figure 6.

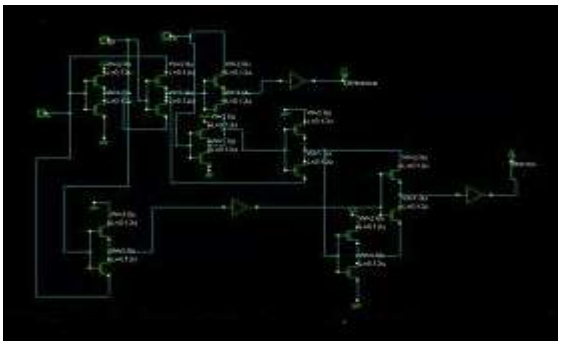

Figure 6: 8T Full Subtractor based GDI

V. EXPERIMENTAL RESULTS

The simulation results are observed using the tanner EDA 16.0 version tool has used for the simulation with 180nm technology with TSMC 80 process for each set of parameters.

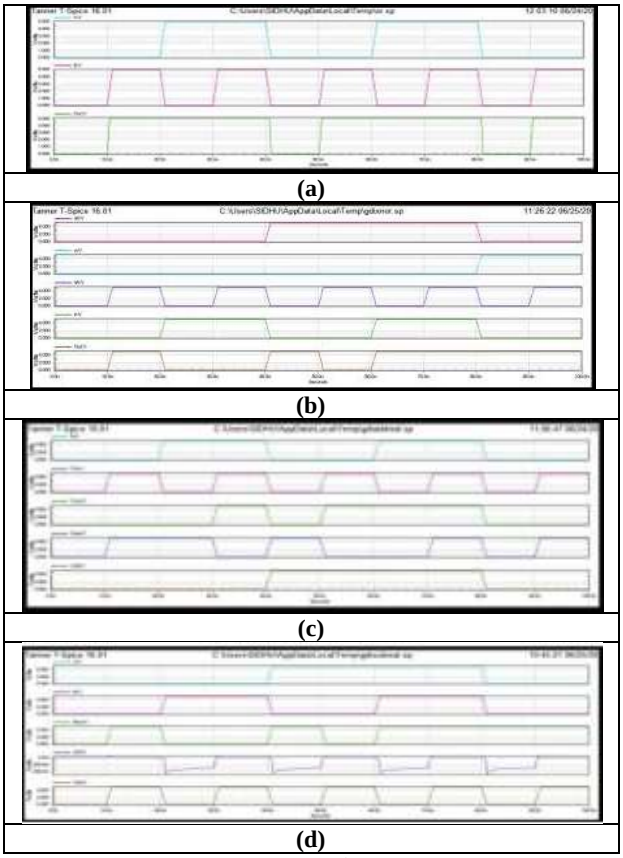

Figure 7: Simulated Output waveforms (a) XOR (b) XNOR (c)Full adder (d)Full Subtractorsubtractor

TABLE I
Number of transistors and consumed power between CMOS and GDI techniques

ALU Functional Programs	CMOS		GDI	
	No. of transistors	Power (µW)	No.of transistors	Power (µW)
OR	6	6.914	2	5.50
AND	6	5.68	2	1.11
XOR	8	19.89	2	1.24
XNOR	8	18.76	2	2.13
Full adder	14	20.48	8	2.16
Full Subtractor	14	21.03	8	6.60

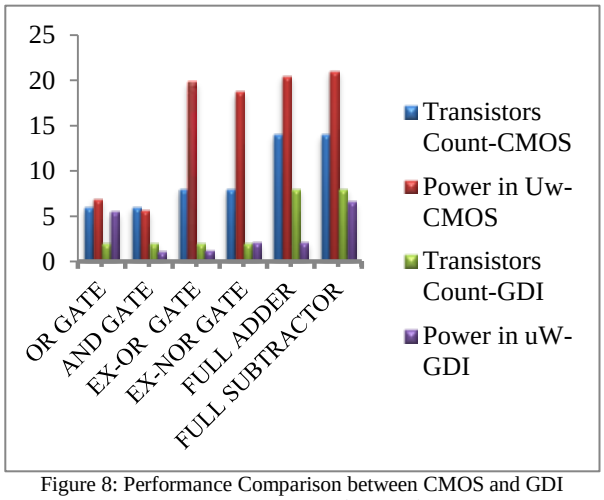

Figure 8: Performance Comparison between CMOS and GDI techniques in the implementation of ALU of Processor

VI. CONCLUSION

This paper basically focused on the structure of low time deferral and superior of ALU utilizing GDI and CMOS logic styles. It additionally introduced an area efficiently with low power architecture. As GDI requires less number of transistors when contrasted with CMOS and other circuit styles. Accordingly, this technique has ended up being effective regarding ALU.

REFERENCES

[1] S. D. Brown, R. J. Francis, J. Rose, and Z. G. Vranesic, "*Field Programmable Gate Arrays*". Boston,MA,USA:Kluwer,1992.

[2] S. Seo et al., "Reproducible resistance switching in polycrystalline NiO films," Appl. Phys. Lett.,vol.85,no.23,pp.5655–5657,2004.

[3] L. Torres, R. M. Brum, L. V. Cargnini, and G. Sassatelli, "Trends on the application of emerging nonvolatile memory to processors and programmable devices," in Proc. IEEE Int. Symp. Circuits Syst.(ISCAS), May 2013, pp.101–104.

[4] M. Wang et al., "*A novel Cux SiyO resistive memory in logic technology with excellent data retention and*

resistance distribution for embedded applications," in Proc. Symp. VLSI Technol. (VLSIT),Jun.2010,pp.89–90.

[5] X. Xue et al., "Nonvolatile SRAM cell based on Cux O," in Proc. 9th Int. Conf. Solid-State Integr.-Circuit Technol. (ICSICT), Oct. 2008, pp. 869–871.

[6] N. Bruchon, L. Torres, G. Sassatelli, and G. Cambon, "Technological hybridization for efficient runtime reconfigurable FPGAs," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), Mar. 2007, pp. 29–34.

[7] Alioto, M., Cataldo, G.D., Palumbo, G.: 'Mixed full adder topologies for high-performance low-power arithmetic circuits,' Microelectron. J., 2007, 38, (1), pp. 130–139.

[8] Bui, H.T., Wang, A., Jiang, Y.: 'Design and analysis of low-power 10- transistor full adders using novel XOR-XNOR gates', IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., 2002, 49, (1), pp. 25–30.

[9] M.Aruna Devi and A.Jagadeeswaran, "Design of Low Power Sense Amplifier Flip Flop using GDI and FinFET Techniques" SSRG International Journal of Electronics and Communication Engineering 5.5 (2018): 4-10.

[10] Kalicherla Himabindu, Mr. K.Hariharan, "Design of territory and power powerful complete adder in 180nm", the worldwide convention on Networks and Advances in Computational technologies, 20,2017.

[11] H. T. Bui, A. Okay. Al-Sheraidah, and Y.Wang, ―New 4-transistor XOR and XNOR designs‖ Tech. Rep., Florida Atlantic Univ., Boca Raton, 1999.

[12] Sreehari Veeramachaneni and Hyderabad, ―New stepped forward 1-bit snake cells‖, CCECE/CCGEI, Niagara Falls. Canada can also five-7 2008, pp. 735-738..

[13] Morgenshtein A, Yuzhaninov V, Kovshilovsky A. Fish, Full-swing gate diffusion input logic-case-study of low-power CLA adder design, Integr. VLSI, J., 2014, 47: 62–70.