Probability-Driven Timing Error Based Multibit Flip-Flop with Clock Gating

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Abstract—*Data-driven clock gated (DDCG) and multibitflip-flops (MBFFs) are two low-power design techniques that areusually treated separately. Combining these techniques into a singlegrouping algorithm and design flow enables further power savings.We study MBFF multiplicity and its synergy with FF data-to-clocktoggling probabilities. A probabilistic model is implemented to maximizethe expected energy savings by grouping FFs in increasing order oftheir data-to-clock toggling probabilities. We present a front-end designflow, guided by physical layout considerations for a 65-nm 32-bit MIPSand a 28-nm industrial network processor. It is shown to achieve thepower savings of 23% and 17%, respectively, compared with designswith ordinary FFs. About half of the savings was due to integrating the DDCG into the MBFFs.*

INTRODUCTION

CMOS technology scale down, increase in process variation, the complexness of integrated circuits,many performance degradation mechanisms and reduction in the power supply affect the reliability and set error values[11],[12].

Circuits' noise margins and reliability are affected by the device size scaling, increase in operating frequency and the power supply reduction, Thereby probability of transient fault generation increases. Many times it is hard to achieve error rate specification levels. Timing error generation are mainly due to various mechanisms like crosstalk, power supply disturbance or ground bounce. The increased path delay deviations, due to process variations, and the manufacturing defects that affect circuit speed may also result in timing errors that are not easily detectable in high frequency and high device count ICs. The already complex testing process can not sufficiently use the huge number of paths in modern circuit designs, and thus it cannot effectively find out all timing related defective ICs. A considerable part of defective ICs may escape the fabrication tests. In addition and for similarreasons, timing verification turns to be a tough task escalating the likelihood of timing failures in a design.Furthermore, modern systems running at multiple frequency and voltage levels could suffer from an enhanced timing error rate due to various environmental andmethod related as well as data dependent variabilities that may have an effect on circuit performance. Besides, *dynamic voltage scaling* (*DVS*) techniques for low power operation which reduces power supply voltage with marginal performance degradation have been proposed in the literature. These exploit timing error detection and correction mechanisms to overcome increased timing error rates. In addition, transistor aging problems considerably impact the performance of nanometer circuits resulting in the appearance of timing errors during their normal lifetime[13],[14]. Such an example is the *Negative Bias TemperatureInstability* (*NBTI*) induced aging of PMOS transistors that degrades their thresholdvoltage in time enhancing path delays [15]. From the on top, it's evident that concurrent on-line testing techniques for timing error detection and correction have become necessary so as to attain acceptable levels of error robustness and meet reliability necessities [16].

In a combinational logic, timing failures are responsible for delayed responses. A delayed response. After the edge triggering of the clock signal that drive the memory elements at the outputs of the combinational block, can result to the generation of timing errors on the information stored within the memory elements. A number of error detection techniques have been proposed in the literature[2],[3],[4],[5],[9],[18][19]. These techniques detect the delayed circuit response and provide error tolerance using time redundancy approach. A well known error detection scheme is based on the use of a comparator which is realized by a simple XOR gate. The monitoring circuitry consists of mux, an XOR gate and a NOT gate for every memory element (flip-flop) in the design. At recent times, transition detectors [8] are used to avail timing error tolerance.

This work presents a reliability aware design technique that provides low power and cost efficient timing error tolerance in nanometer technology small cores designs that are the building blocks for many

core system-on-a-chip (SoC) applications. Two error detection techniques to latch based designs are worked out in [10]. A bit flipping flip-flop topology is introduced in this work along with a proper error handling mechanism that provides timing error detection and correction in flip-flop based cores. A pririor version of this process has been presented in [6].

I. RELATED WORKS

Timing error detection and correction techniques may be divided into two general categories, they are targeting flip-flop based designs and targeting latch based designs.

A. Razor technique

A pipeline architecture named razor [1] contains error detection and correction capabilities. It consists of main system flip flop plus an assistant shadow latch, a mux and an XOR gate. The xor gate performs as a comparator and compares the outputs of the main flip flop and the shadow latch. The xor output will rise to high indicating the detection of an error and to low indicating the absence of error. The main advantage in this paper is efficient error detection and correction of errors with energy reduction. Disadvantage is that razor technique suffers from increased silicon area, for every main flip flop an extra latch, a mux and xor gate are required. In addition an extra clock signal is used.

B. Timber technique

This paper presents TIMBER [20], a technique for online timing error resilience that finds timing errors by borrowing time from successive pipeline stages. TIMBER-based error masking will recover timing margins while, not instruction replay or roll-back support is used. Two sequential circuit elements—TIMBER flip-flop and TIMBER latch—that implement error masking based on time borrowing are described.

It utilizes an additional latch per main system flip flop.The main advantage of this paper is that it recovers the time margins and improves the performance and power consumption of the circuit design and the drawback is, it requires three extra clock signals plus two control signals for its operation.

C. Time dilation technique

Inthispaper,theTimeDilation [7]design techniqueisproposedthatprovides errordetectionandcorrection technique and alsosupportsoff-line manufacturingscantesting.By using anewscanFlip-Flop,theTimeDilationtechniqueiscapabletodetectand correctmanyerrorsat theminimumofoneclockcycledelay. Thearea overheadandthepowerconsumptionarereduced,sinc enoadditionalmemoryelementsarerequired.

The stage registers are constructed by using the time dilation flip flop , that consists of scan flip flop, a mux and an XOR gate. Atthesametime,this technique introducesonlynegligibleperformancedegradationsi nce noextracircuitryisinsertedinthecriticalpaths ofadesign. The main advantage is that it reduces the silicon area overhead and the disadvantage is that number of buffers is increased and consequently silicon area penalty and error tolerance is reduced.

D. Razor II technique

In this paper, we present a design RazorII [9] which implements a flip-flop withdetection and architectural correction. Error detection is based on flagging spurious transitions in the state-holding latch node. The RazorII based DVS allows removal of safety margins and operation at the first failure of the processor, which exploits a transition detector for error detection while error correction is performed through architectural replay. The main advantage is, it Provides energy efficiency and error tolerance. Disadvantage is its Conflicting power and less performance.

E. Timing error tolerance in soc applications

Timing error is an increasing reliability concern in nanometer technology, high complexness and multi voltage/ frequency integrated circuits, which is given in the literature [17]. A local error detection and correction system is presented in this paper. It is based on a new bit flipping flip flop. Whenever a timing error is detected, by complementing the output of the flip-flop it is corrected. The proposed solution is characterized by very low silicon area and power requirements compared to previous design. Apart from the original flip flop (Main Flip-Flop), the system consists of two XOR gates and a Latch. The first XOR gate compares the input and output of the Main Flip-Flop and provides the result to the Latch.

The Latch sends the second XOR gate at the output of the Main Flip-Flop. Depending on the comparison result within a particular time interval, either the output of the Main Flip-Flop or its complement is propagated to the final output of the EDC Flip Flop.

F. Summary

The above shown papers fail to detect and correct the timing errors more efficiently, also the power consumption, silicon area overhead of the existing systems is more compared to the proposed method in addition speed of the circuit operation is slow.

II. PROPOSED SYSTEM

A new soft and timing error detection circuit delivers fast response times with the use of a MUX and inverter. The proposed flip-flop detects late-arriving data by comparing the input and output of the flip-flop using XOR gate as a comparator. MUX uses the XOR output as a selection line and choose either flip flop normal correct output or inverted output. The proposed circuit is shown in the figure 1.

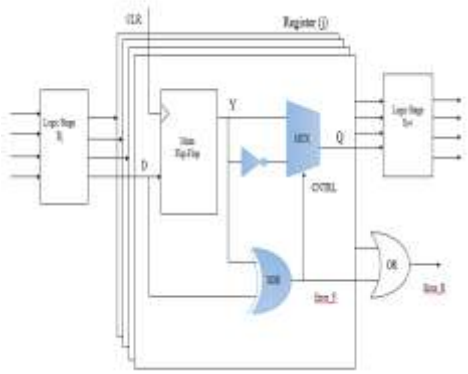

Fig 1.Proposed circuit

That is when the xor gate output is "0" then the comparison output is "low" indicating timing error free condition and so the output of the flip flop is given directly to the next stage of combinational circuit through the 2*1 MUX. But when the XOR gate output is "1" then the comparison output is high indicating timing error, hence in this condition the output of the flip flop is inverted using NOT gate and gives the corrected output to the next combinational stage. A main characteristic and an advantage of the proposed circuit is that no extra circuitry is inserted in the critical path from the *D* input to the *Q* output of the Flip-Flop or in the distribution path of the clock signal *CLK*. The additional MUX is inserted in the path which is not critical. The main advantage of the proposed method is that the speed is increased, area is reduced, and the power consumption is decreased. In addition the error tolerance is better when compared to the previous schemes and it is implemented using Xilinx 12.1.

III. OUTPUT OF THE PROPOSED METHOD

At first *clk,d,reset and f* are the inputs where *y,cntrl* are the intermediate output, *correct* is the final output of the flipflop which is given to the next combinational logic stage.Initially clock is given as positive edge triggering,d is the input of the flip flop where it can be given either zero or one here "0" is given first,reset is given "1" for resetting and then "0" ,fault is initially given as "0" that is fault free condition then checked for faulty condition that is "1"the figure 2 shown below is error detection and the next figure 3 shows the correction of error in the proposed system.When control is "0" there is no detection of error so the output of the flipflop "y"is given to the next combinational stage through MUX and when the control is "1" fault is detected and so the output of the flip flop is inverted through the NOT gate and then given to the the next combinational stage through MUX. Below graph shows the clearly that the error detection and correction is more efficient than the existing methods.Table 1 shows the comparative values of power,area and speed between existing and proposed techniques.

Fig 2.Error detection of the proposed method

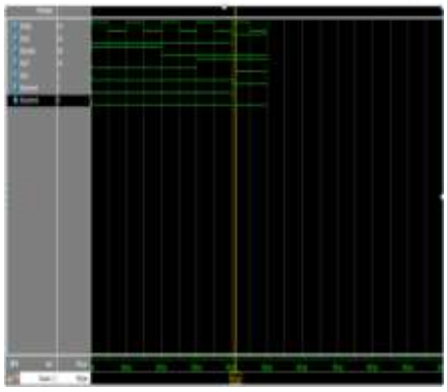

Fig 3.Error correction of the proposed method

TABLE I. COMPARISION TABLE

S.NO.	Parameter	Existing	Proposed
1.	Power	0.027 watt	0.011 watt
2.	Area	17	12
3.	Delay	7.889 ns	7.760 ns

A. Performance analysis

The graphs given below shows that there is a considerable reduction in time and area based on the implementation results which have been done by using Xilinx ISE 12.1, Spartan 6 family. The proposed technique significantly reduces power consumption when compared to the existing system. The power comparison of the existing and proposed is shown in the figure 4 and the comparison chart for area and delay is shown in the figure 5 and figure 6 respectively.

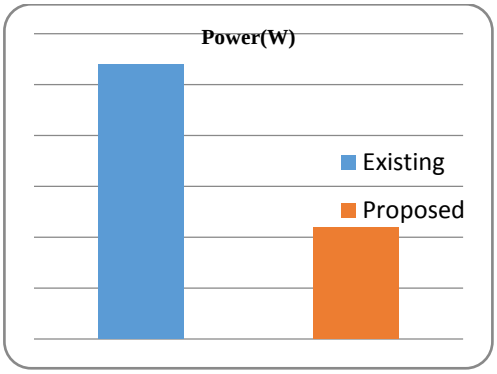

Fig 4.Comparison chart for power

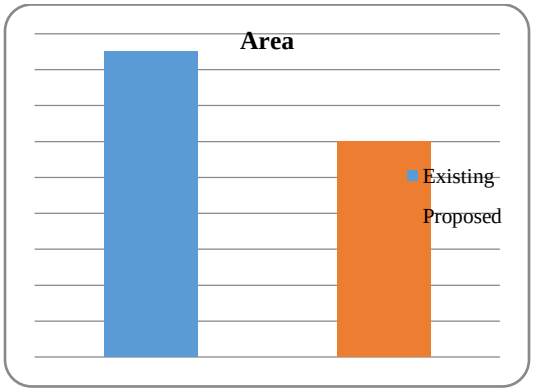

Fig 5.Comparison chart for area

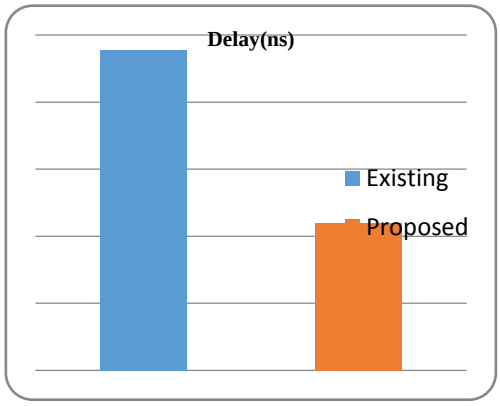

Fig 6.Comparison chart for delay

The comparison of device utilization summary between existing and proposed system is shown in the figure 7.

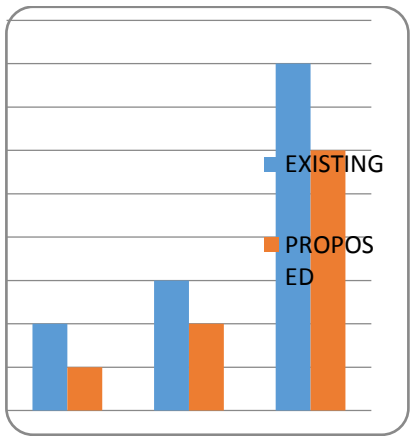

Fig 7.Bar chart for device utilization summary

IV. CONCLUSION

Timing errors are a real concern in modern nanometer CMOS technologies. A promising way to cope with them is the development of error detection and correction techniques. A timing error tolerance technique is presented in this work for enhanced reliability in flip-flop based nanometer technology cores. It exploits a new bit flipping flip-flop, which provides the ability to detect and correct timing errors in a circuit, with a time penalty of a single clock cycle. The proposed approach is characterized by low silicon area requirements and reduced design complexity that also result in reduced power consumption with respect to earlier design schemes.

V. FUTURE WORK

The router is characterized by its design having four directions (North, South, East, West) suitable for a 2-D mesh NOC. The PEs and IPs are connected to any facet of the router. Thus there's no specific connection port for a PE or IP. The proposed detection mechanism can even be applied to NoCs 5 port routers with a port dedicated to an IP. Our proposed efficient error detection and correction technique is employed in router to reduce the timing errors.

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