Fast Multiplier Design Using MBA with Hybrid Adder

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Abstract

This paper suggests a new multiplier which gives improved performance in terms of carry computation. Proposed multiplier starts with an idea of combining the CSLA and KSA adders in the finishing addition of PP generation. The anticipated multiplier is a Modified Booth-multiplier using Hybrid adder to achieve high speed by reducing the delay. MBM is an efficient multiplier which diminshes the PP's stages using the bit pairing encoding process to increase the speed of computation. Hybrid adder uses a KSA in CSLA structure to lowering the delay in the operation. A comparative analysis is done using xilinx 13.2 design suite in-terms of area and delay .

Keywords: CSLA, KSA, Hybrid Adder, MBM.

I.INTRODUCTION

In most of the systems the basic arithmetic operation that are performed are accumulation, subtraction, multiplication, division. From the above discussion the multiplication opearation is slows any system performance(1). The speed at which a multiplexer operation can be carried out by the performance of many computational problems. To design a multiplier with required speed, huge hardware resources are utilized, Here is a need to design a multiplier that has high speed and area efficient. Most of the research work was done on improving operating speed area and power consumption to design an efficient multiplier architecture(2),(3).Here we mainly focusing on the constrainsts, speed and area of multiplier architecture. In most of the microprocessor digital signal processing systems and communication systems, the multiplier plays a major role. A multiplier has its application include digital filtering digital communication and spectral analysis.

The entire procedure of multiplication is divided into three parts, PP generator and a Wallace structure to compact the PP and final addition(4). BE is used to generate minimum number of PP stages.

In Modified Booth, half of the PP stages are reduced compared to Booth Multiplier. For parallel addition of PP a WT structure is used. In final addition the hybrid adders are used to reduce the carry propogation.

Nowadays, we are mainly focusing on reducing the stages in PP by encoding the addition using parallel prefix adders..To achieve high speed as per the constraint a special adder which gives better performance is designed, which referred as Hybrid adder. By using high speed hybrid adder design a fresh MBM is discussed and also the conventional MBM design with carry look-ahead adder is compared with proposed multiplier.
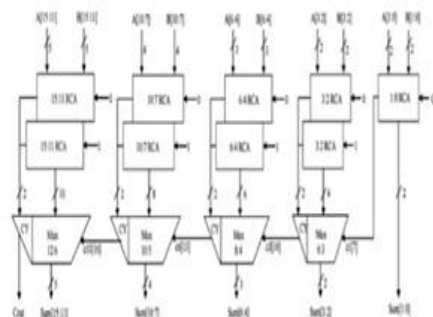
II.RELATED WORK

A. CSLA

Fig1: block diagram of CSLA

The carry select adder commonly consists of dual CPA and mux, adding two n-bit binary numbers with the carry select adder, with two CPA adders to make the computation twice one time with an assumption of carry in being zero and other assuming as one, after the two results, once the accurate carry in is known the mux selects the correct sum and Cout.

B.High Speed Adders

Parallel prefix adder is primarily fast compared with CPA. Parallel prefix adder is the family of the adder taken from the normally known carry look-ahead adder. The two familiar parallel prefix adders are Brent-Kung and Kogge-Stone adders, which reduces carry computation process.
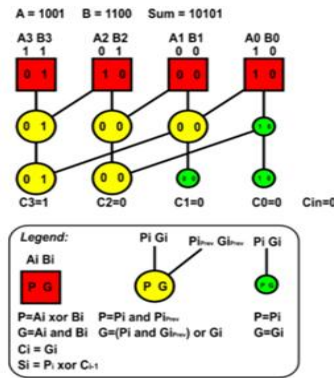
C.Kogge-Stone Adder

Fig2: 4-bit KS adder

The input A and B are given for each block for every input a bit is assigned the above fig shows the 4-bit kogge-stone adder. To perform the operation the first red box has two inputs that are designated as Ao and Bo which performs XOR for propogate and AND for generate and then next A1,B1 perform as well and similarly for A2,B2 and A3,B3.

The yellow circle performs $P=P_i$ AND P_{iprev} for propogate and $G= (P_i$ AND $G_{IPREV})OR$ G_I for generate(5). The green circle acts as a buffer.

III.PROPOSED MULTIPLIER USING HYBRID ADDER

By using MBA we can perform a fast multiplication. The logarithm of the word length operands and this MBM computational time are relative to each other. By utilizing radix-4 algorithm it expands the fastness of the multiplier and diminishes chip-area of the multiplier circuit. Rather than multiplying with zero or one after changing and including of each column of booth multiplier in this algorithm second column is considered and multiplied by 0 or 1 or +2 or -1 or -2. By utilizing Booth algorithm half of the fractional produts can be diminished. The method of encoding multiplicand is performed by radix-4 BE based on multiplier bits. For contrasting three bits at once overlap is utilized. Grouping is begun from LSB,

in this just two bits of booth multiplier are utilized by initial block and 0 is expected as a third bit appeared in figure
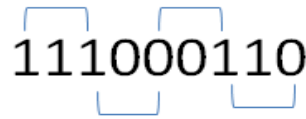

Fig3: Bit pair recoding

The figure shows the point of radix-4 BE that consists of 8 unlike types of states.

TABLE1: Booth recoding for radix-4

Multiplier Bits Block			Recoded 1-bit pair		2 bit booth	
i+1	i	i-1	i+1	i	Multiplier Value	Partial Product
0	0	0	0	0	0	Mx0
0	0	1	0	1	1	Mx1
0	1	0	1	-1	1	Mx1
0	1	0	1	0	2	Mx2
1	0	0	-1	0	-2	Mx-2
1	0	1	-1	1	-1	Mx-1
1	1	0	0	-1	-1	Mx-1
1	1	0	0	0	0	Mx0

The process given below represents radix-4 BA:

1. If necessary enlarge the sign bit 1 position to ensure n is not odd.
2. Put 0 to the right of LSB of BM.
3. According to bit-pair encoding each PP will be 0, +X,-X,+2X or -2X.

A.Hybrid Adder

By merging CSLA and KSA(6) adder designs, a quicker addition method can be introduced called Hybrid adder. CSLA is simple but fast it has binary adder circuit and MUX (7)(8)(9). To save delay in carry select, mandatory to calculate all the bits and choose the correct bit to get the correct result.

The S and Cy bits simultaneously can be calculated by the two adders ones the carry bit is known the correct S and Cy bits can be selected by mux. Instead of RCA, KSA is utilized which is parallel prefix of CLA(10).

This KSA can generate the carry bit faster. In both the adders the delay is reduced at large extent. To design faster circuit, the properties of both the adder circuit is used. Multiplexer selects the correct S bit.
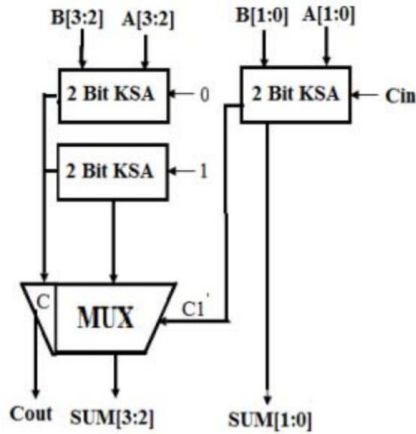
Fig4: 4-bit Hybrid adder

From the fig, first column operation is perfored using KSA addition method. And the remaining operands addition are performed using KSA in CSLA structure. All other paired block can calculated twice by same method(11). In order to take correct sum as number of input bits increases for this several multiplexers are needed.

IV. PROPOSED MULTIPLIER

It has 4 parts : 2's complement, BE, Booth decoder, and Final addition.

A.2'scomplement

When signed operation is performed the 2's complement operation is used to differentiate between the positive and negative multiplicand to be added.
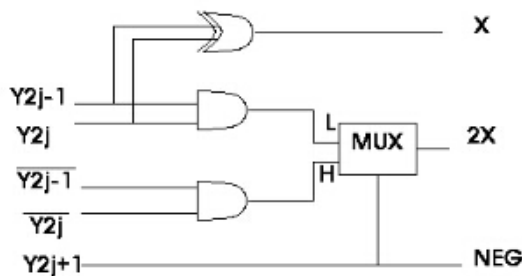
B.BE

Fig5: BE

The following equation below is MB multiplier{z} digits can be defined

$Z_J=Y_{2J}+Y_{2J-1}-2Y_{2J+1}$ with $Y_{-1}=0$.

The MBA encoder circuit in the above fig. the product of value of Z with multiplicand Y may be -2X,-X,0,X,2X. If performed left shift operation the generation of PP stage 2X may be generated(13). Negation can be done by changing 0's as 1's and 1's as 0's (1's complement) and then 1 is additional to appropriate 4:2 compressor from the fig. BE generates 3 o/p signals by charming 3 successive bit input to represent 5 possibilities. -2X,-X,0,+X and +2X
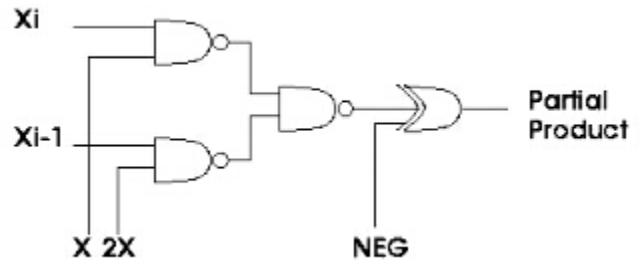

Fig6: PP generation

Each PP contains two consecutive bits from multicand based on requirement(14). If we required the output and its complement is generated. The above fig shows PP circuit generator. For negative value of X we take 2's complement. The various adders are, RCA, CLAA, CSA.

The CLAA and CSA adders are fastest adders and frequently used. The multiplication of X is done by after completing the shift operation on X that is –X is again shifted to left by one bit position.
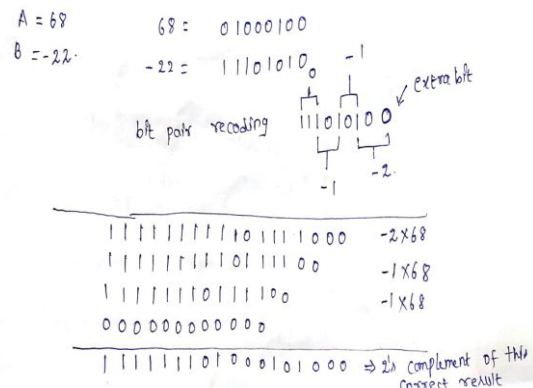

Fig7: example of MBM process

C. Booth Decoder

The decoder depending on the bits scanned in the multiplier by BE signals. Based on signals the

decoder will produce the PPs. To produce PP the operation indicating the signals achieved by decoder on multiplicand. Multiplier unit takes input signals from BE and the multiplicand and complement value of multiplicand i.e., A and A' and that generates the PP.
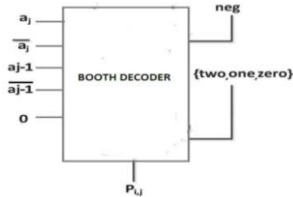

Fig8: Booth decoder

The MBE circuit generates negative signals and decide to pass either input or its 2's complement. The other input select line is a combination of {two, one, zero}. It will pass the last state of input if two is high else if both two and neg is high. Input is 2's complemented last state of input, the output is A if one is high or else its complement. Only right shifting is done if zero is high.

D. Final Addition

The WT structure is results into two rows: It contains S and Cy bits, once the addition operation is performed on PP's. By using faster adder circuits the two rows are added. The theme is to increase speed of addition in final addition stage, that will reduce the evaluation time of multiplication. A hybrid adder design is proposed for last stage.

TABLE 2: Delay and area analysis of adder designs

Adder Design	Number of LUTs	Delay(ns)
CLA	6 out of 28,800	4,461
Hybrid Adder	5 out of 28,800	4.017

TABLE 3: Comparison table for MBM

Multiplier Design	Number of LUTs	Delay(ns)
Modified Booth Wallace Tree with CLA	230 out of 28,800	4.8
Proposed Modified Booth Multiplier	212 out of 28,800	3.710

V.CONCLUSION

A novel MBM is proposed in this paper. In final stage of MBM design CLA design is substitute with the Hybrid adder. Hybrid adder has lower delay and occupy less area compare to CLA design. The architecture from conventional method had maximum area. Here, significant improvement in carry computation is achieved by Hybrid-adder with proposed multiplier.

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