An Efficient Multiplication of Braun and BW Multiplier

K.Sireesha[1]
P.G. Student
AITS
Kadapa, India

Dr.T.Lalith Kumar[2]
Dept. of ECE
AITS
Kadapa, India

T.V.Nirmala[3]
Dept. of ECE
AITS
Kadapa India

K.Md.Haneef[4]
Dept. of ECE
AITS
Kadapa, India

S.Saleem[5]
Dept. of ECE
AITS
kadapa, India

Abstract

Multipliers and Adder play a main part in the functioning of different systems used in signal processing system and DSP systems. The carry save multiplier and BW multipliers use the parallel architectures. Hence they are the most frequently used multipliers for positive number and negative number multiplication operations. Any circuit design, the three main conditions are calculated the result of design circuits are delay or speed, power and area. This paper discussing the designed and implementation of modified BW and BMs for positive and negative number multiplication respectively, and calculate the analysis of speed and power and area of these two multipliers. The three different logics are used to design the adder that are basic CMOS, domino dynamic logic and split path data driven dynamic logic. These three different adders are used to design the multipliers. An reduce power consumption and reduce the delay but increase the speed and reduce the area is observed in BM and BW multiplier.

Keywords- 2:2 converter adder, 3:2 converter adder, Baugh- wooley multiplier, BM, domino dynamic, CMOS logic, split path data driven dynamic logic.

I. INTRODUCTION

The basic component of computational circuits is multipliers. All digital circuits are employing the multipliers. The different of multipliers are used for some applications in DSP and communication systems. Most instructions are involves multiplication. These results dominate the timing of operation. Hence it necessary to design and implement high speed multiplication. One of the issues is power consumption(1) in design of multipliers. To reduce the power consumption. The addition of partial product is modified to reduce the power. Power consumption is main part of circuits design. Hence it needs some parameters that are low power high speed.BW and BMs are parallel architecture and mostly used multipliers are signed and unsigned operations. These multipliers are operating on parallel, but speed is increase [6]. The design of multipliers is mainly focussed on design low delay and low power consumption multipliers. The increase the speed of multiplication to more efficient computation as the time taken the process is reduced. This in turn improves the performance of the communication system. Thus a high speed adder ultimately influence the effective functioning of higher modules employed for wide range of communication applications.

The prepared of the paper is as follows a explain literature review is given in section II. Different adder and multipliers architecture and enhancement in section III and IV respectively. Section V observes the simulation results. Conclusions in section VI.

II. LITERTURE REVIEW

The main component is multipliers in communication applications and signal processing. Different categories of multiplier architectures are discussed here pramod (1).The key features of their working and also different multipliers architectures are presented by pramod.in case of multiplication operations faster processing time along with rearrangements of partial products are obtained to get high precision. Negative number multiplication and positive number multiplication are performed using BW multiplier (3). To obtain the positive sign of all sectional products signed operands are multiplication is performed using 2's complement method (9). The coordinate multiplier examples are the BM and carry save multiplier (1),(2). BM is a parallel multiplier where imperfect products are computer concurrently and then the carries are added and carries ripples in the adder in the last stage (4).The goal of this paper is increasing speed of data and reducing power. To execute the above mentioned we need high precision

for floating points requires complex hardware and consume more power then fixed point number (10). Logarithmic multipliers are selected (16).I am uses the SPD3L for the adder design. This reduces the delay between the components and thus the multiplier speed increases (3). Suggest novel architectures in which the full adder employed in the multiplier architecture is using domino logic.

III.CONFIGURATION OF ADDERS

Many different adder configurations such as adder using XOR gate ,full adder, and using two half adder can be design which consists of 32 transistors. Here 28 transistors CMOS adder and split path data driven dynamic logic is used which are faster compared to the conventional adder. These adder are then used to construct the two multipliers architectures and each adder configuration influences the performance in unique way.

A. Cmos Adder

The 1-bit full adder is used to add 3 input bits and output is obtain in terms of sum and carry out. Conventional equation of 3:2 converter suggests that a sum and carry are independent of each other. However it is seen that their dependency between them. To account for this dependency, adder architecture. Is modified to reuse the carry modified equations for sum and carry are represented by using A and B.

$$S=ABCi+ACo+BCo+CiCo$$

$$Co=AB+AC+BCi$$

$$S=ABCi+(A+B+Ci)Co$$

$$Co=A(B+C)+BCi$$

The basic CMOS full adder can be constructed by using NMOS and PMOS devices the design of 1-bit full adder is fairly simple and the architecture complexity is minimal. The CMOS full adder can be presented by using 28 transistors. It is consists of 24 transistors and 2 inverters.

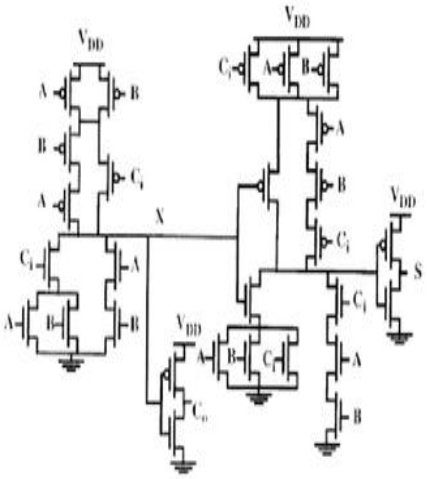

Fig1: a: full adder using CMOS logic

B. Domino logic

The dynamic logic uses clk signal to realize logical circuits. these circuits consumes less area as a single active pull up is used.CMOS dynamic domino circuits operates using a sequence of pre-charge phase and valuation phase s synchronized using a clk signalling the pre-charge phase the output signal is to a predefined value, which is logical high for a NMOS based circuits(11).during a evaluation phase, the output signal can change its state depends on the input signal. Due to the options of a typical pull up network consisting of PMOS devices, dynamic domino circuit it exhibit high switching speed while occupying low area as compared to the corresponding CMOS design.

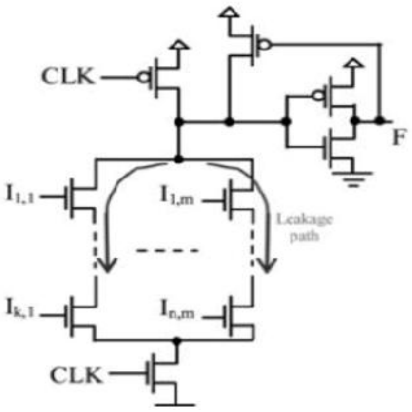

Fig2: dynamic implementation of SOP function.

These design makes them highly desirable in the application of a high performance micro processors while dynamic logic are series connection it leads to charge sharing disadvantages. To overcome these drawbacks, domino circuits with keeper transistors are used.

C. Split path data driven dynamic logic

Data driven logic circuits has a drawbacks that the pull up networks has cascaded of PMOS.These PMOS need large width and length ratio for faster re charge which in terms increase parasitic capacitances and hence dynamic power.spd3l circuits tries to overcome these drawbacks the only idea is to split the pull down network of the generic gate into evaluation sub networks one per each products subtraction. hence the no of cascaded connected design in pup network and input capacitances is reduced. Therefore power and delay also reduced. Each transistor size also reduced.

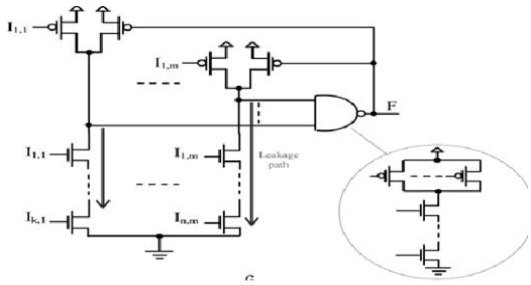

Fig3: SPD3L implementation

IV.ARCHITECTURESOF MULTIPLIERS

Multipliers which are used in parallel architecture are functionally faster compared to the other multipliers (7). Hence multipliers such as carry save multipliers (1) and BW multipliers (13) are mostly used.

A. BM

Carry save multiplier is known for its normal structure (7), its operation is based on shift and added method. The partial product is generated by products of the multiplicand with one multiplier bit. It is shifted with respect to they bit orders and then added.n-1 adders are used. Where n is the multiplier magnitude. The addition can be performed using carry chain adder, to reduce delay and length the carry chain adder can be replaced by CSA which sum and carry signals are passed to the adders of the next stage. Final product is obtain in last stage adder using carry chain adder (2).

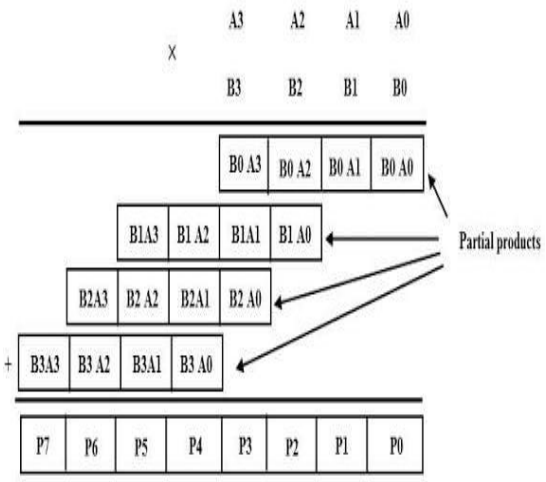

Fig4:: 4-bit un sign multiplication

Fig e and fig d is the example of BM and architecture of BM respectively is as shown in below figures.

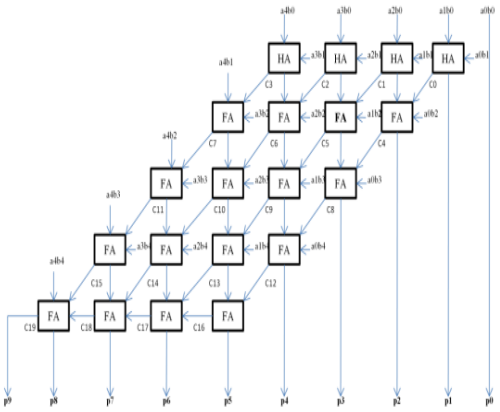

Fig5: architecture of 5 bit BM

B. BW multiplier

In BW multiplier the negative number operands are represented in 2's complemented. While in partial products are ordered such that the negative sign is move to the last step, which in turn maximise the regularity of the array. While multiplying a 2's completed numbers directly each of the partial products to way added is assigned numbers. Again each partial product has to be sign extended to the width of the final product is ordered form a correct sum using CSA structure, bi-partial product matrix. We approach in an efficient way of adding extra

entries to the bit matrix suggest to avoid having to deal with the negatively waited bits (9).

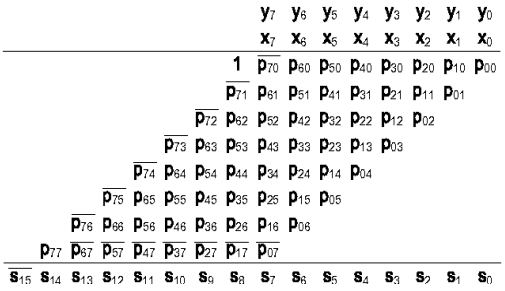

Fig6: signed multiplication using BW multiplier

To the design of the circuit with the help of cadence virtuoso tool. The process technology chooses in 180nm. The procedure to the installation is

I. Design of 1-bit full adder
II. Design of modified adder using domino dynamic and SPD3L.
III. Design of BW and carry save multiplier using the full adder.
IV. Installation of BW and carry save multiplier using a derived address.
V. Simulation and synthesis of modified multipliers.

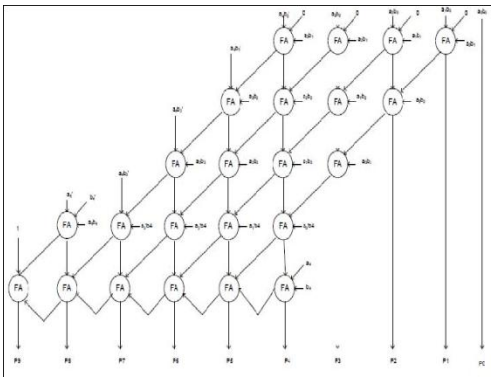

Fig7: architecture of BW multiplier

V.CONCLUSION

In this paper is discussed on Braun multiplier and Baugh Wooley.the Braun multiplier is used to perform the unsigned multiplication. Baugh multiplier is used to perform the signed multiplication. The Baugh wooley multiplier operation is based on 2's complemented method. The complemented method is used to increase the speed of sign multiplication. The three logic are used to design the full adder that are basic CMOS logic, domino dynamic logic and split path data driven dynamic logic. That full adder is replaced by conventional Baugh wooley and Braun multiplier. The basic CMOS adder is using design the multiplier but area, power and delay is large. To overcome this disadvantages use the domino logic. The domino logic is used to design the multiplier. The domino logic is better for unsigned multiplication because power, area and delay is low. the domino logic is used for signed multiplication but power, area and delay is high .these disadvantages overcome by using split path data driven logic. The SPD3L logic is used to designed multiplier. This logic is mostly used for signed multiplication because power, area and delay is less. my proposed system is these three adder are replaced the multipliers and then improved the delay, power and area.

VI.REFERENCES

[1] Pramod S. Aswale, Mukesh P. Mahajan, Manjul V. Nikumbh, and Omkar S. Vaidya, "Implementation of Baugh-Wooley Multiplier and Modified Baugh Wooely Multiplier using Cadence (Encounter) RTL,"
[2] International Journal of Science, Engineering and Technology Research (IJSETR), vol. 4, issue 2, pp. 293 – 298, Feb. 2015.
[3] Fathima Nazrin K., Dhivya V., and M. Darani Kumar,"Hybrid Low Power Design for Adders using SPD3L," International Journal of Advanced Information Science and Technology (IJAIST), vol. 12, pp. 1 – 6, April 2013.
[4] M.B.Damle and S. S. Limaye, "Low-power Full Adder array-based Multiplier with Domino Logic," IOSR Journal of Electronics and Communication Engineering (IOSRJECE), vol. 1, issue 1, pp. 18 – 22, June 2012.
[5] Chetan C.S., Vinay B. Biradar, Vishwas P.G., and Premananda B.S., "Performance Enhancement of 32-bit Carry Select Adder by Employing RTL Optimization Techniques", International Research Journal of Engineering and Technology, IRJET, vol. 2, issue 3, pp. 2273 – 2277, June 2015.
[6] Lakshmi Narayanan G., and Venkataramani B., "Optimization Techniques for FPGA-Based Wave Pipelined DSP Blocks," IEEE Transaction on Very Large Scale Integration. VLSI Systems, vol. 13, no. 7, pp. 783 – 792, July 2005.
[7] Benini L., Micheli G.D., Poncino M., and Scars Ri, "Glitching Power Minimization by Selective Gate Freezes," IEEE Transaction on Very Large Scale Integration (VLSI) Systems., vol. 8, no. 3, pp. 287 – 297,
[8] June 2000.
[9] Anitha R., and V. Bagyaveereswaran, "Braun's Multiplier Implementation using FPGA with Bypassing Techniques," International Journal of VLSI Design & Communication Systems (VLSICS), vol. 2,issue 3, pp. 201 – 212, Sept. 2011.
[10] M.Sjalander, and P. Larsson Edefors, "Multiplication Acceleration through Twin Precision," IEEE Transaction on VLSI Systems, vol. 17, pp. 1233 – 1246, Sept. 2009.
[11] M.V.P. Kumar, S. Sivanantham, S. Balamurugan, and P.S. Mallick, "Low power reconfigurable multiplier with reordering of partial products," in Proceedings of International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN), pp. 1 – 6, 2011.
[12] Premananda B.S., Samarth S. Pai, Shashank B., and Shashank S. Bhat, "Design of Area and Power Efficient Complex Number Multiplier," in Proceedings of Fifth IEEE

International Conference on Computing, Communication and Networking Technologies (ICCCNT), pp. 1 – 5, July 2014.

[13] Vivek V. Babu and S. Mary Vijaya Lense, "Delay Optimized 16-Bit Twin Precision Baugh Wooley Multiplier," International Journal of Emerging Technology and Advanced Engineering (IJETAE), vol. 4, issue 3, pp. 90 – 95, March 2014.

[14] Shweta B., Tejal S., Kiran S., and Kamde Archana G., "Implementation of Modified Baugh Wooley Signed Multiplier," International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE), vol. 5, issue 2, pp. 2317 – 2321, Feb. 2017.

[15] Jipsa A. and Jyotirmoy P., "Design and Implementation of High Speed Baugh Wooley and modified Booth Multiplier using Cadence RTL," 796 International Journal of Research in Engineering and Technology (IJRET), vol. 3, issue 8, pp. 56 – 63, August 2014.

[16] Pramodini M., and Rashmi R., "An Efficient Baugh-Wooley Architecture for Both Signed & Unsigned Multiplication," International Journal of Computer Science & Engineering Technology (IJCSET), vol. 3, issue 4, pp. 94 – 99, April 2012.

[17] Anitha R., Alekhya N., Lincy Jesima W., and V. Bagyaveereswaran, "Comparative Study of High performance Braun's Multiplier using FPGAs," IOSR Journal of Electronics and Communication Engineering (IOSRJECE), vol. 1, issue 4, pp. 33 – 37, May 2012.

[18] Rajatha B.R., Pooja K.S., Sadhvika G.B., and Premananda B.S., "Implementation of Operand Decomposition in Signed Logarithmic Multipliers," in Proceedings of IEEE International Conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT), pp. 2126 – 2129, May 2016