High Speed and Area Efficient CSLA with Novel MFSU

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Abstract

Adders are one of the main components that execute arithmetic computations, and they are typically used in MAC (multiplier-accumulator) operations for signal processing systems. As a result, the performance of the adder has a significant effect on the performance of the system. Although the Ripple Carry Adder (RCA) is one of the most common types of adder, it has a longer carry propagation delay (CPD). In contrast, the CSLA can improve the CPD, but it requires a larger chip area and consumes more power. To overcome these limitations a high-speed, energy efficient carry select adder (CSLA) dominated by carry generation logics is presented. This architecture is composed of three functional stages – a Primary Carry Unit (PCU), an Intermediate Wave Carry Unit (WCU) and a Final Selection Unit (FSU) – that are partitioned with the appropriate bit-width. The CSLA is partitioned into bit-slice logics to reduce the propagation delay. But this architecture increases the area. To overcome this problem, the CSLA is proposed with modified FSU that reduces the usage of logic gates. The proposed architecture skips the carry computation in the first stage of each bit-slice block. The proposed CSLA is implemented for various input bit widths. The results show that the proposed CSLA reduces the computational delay by 7% and area by 4% to the conventional ones.

Keywords—*MAC (Multiplier accumulator), CSLA (Carry Select adder), RCA(Ripple carry adder), PCU(Primary carry unit),WCU(wave carry unit), FSU(Final selection unit),CPD(carry propagation delay)*

I. INTRODUCTION

The explosive growth of VLSI Technology the demand and popularity of portable devices has driving designers to strive for smaller silicon area.The central electronic circuit used for addition is adders.

Adders are fundamental for wide variety of digital system. Many adders exist but the fast adding with low area and power still challenging. There are different types of adders such as Ripple carry adder(RCA), Carry skip adder(CSKA),Carry look ahead adder (CLA), Carry save adder(CSLA),etc.

Among them RCA shows compact design but their computation time is longer. It has lowest speed amongst all adder because it has large propagation delay but occupy less area. Then ,in CLA can drive fast result but it leads to increase in area, among these adders CSLA have small area.

We have designed an efficient logic design for CSLA. This paper presents a "High speed" and "Area efficient" CSLA with Bit slice Logic.All input variables in the proposed CSLA are carryfunctions and each functional block in the CSLA also generate carry functions as outputs.

In our proposed system a new CSLA with Modified Final selection unit consists of combinational logic instead of the typical RCAs and MUXs are used for conventional implementation.

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II. ADDERS

Adder are a digital circuit that performs addition of two numbers . In Many kinds of processors adders are used in the arithmetic logic units (ALU). They can also utilized in other parts of the processor. They are used to calculate addresses , table indices, increment and decrement operators and similar operations such as addition ,subtraction ,multiplication.

A. Ripple Carry Adder

The design of a ripple carry adder is simple and that allows fast design time , however the Ripple carry adder is relatively slow .Because each full adder must wait for the carry bit which is rippled from the previous full adder . The propagation delay can easily be calculated by inspection of the full adder circuit.

B. Carry Lookahead Adder

For the purpose of reducing the computation time Carry lookahead adders used to add two binary numbers . They work with the assumption by creating two signals for each bit position based on whether a carry is propagated through from a less significant bit position or killed in that bit position. Some advanced and high speed carry lookahead architectures are the Manchester carry chain , Brent Kung adder and the Kogge stone adder.

C. Carry Select Adder

A carry select adder is one of way to implement an adder , which is a logic element that computes the sum of two n-bit numbers .

The carry select adder is simple and fast having a gate level depth. For the purpose of adding two n-bit numbers with a Carry select adder is done with two adders in order to perform the calculation twice, one time with the assumption of the carry is being zero and the other assuming the carry will be one . After the two results are calculated the final sum as well as the final carry out is then selected with the multiplexer, afterthe correct carry –in is known . The bit width in each carry select block can be uniform , or variable . If the ideal number of full adder elements per block is equal to the square root of the number of bits being added, that will yield an equal number of MUX delays. The carry select adder design can be complemented in the way of area reduction with a carry lookahead adder structure to generate the MUX inputs, thus it produced even greater performance and potentially reducing area.

III. BIT SLICE LOGIC

Bit slicing is a efficient technique for constructing a processor from modules of processors of smaller bit width for the purpose of improve the word length . Every component modules processes one bit field or slice of an operand. The grouped processing components would have the capability to process the require full word length of a particular software design.

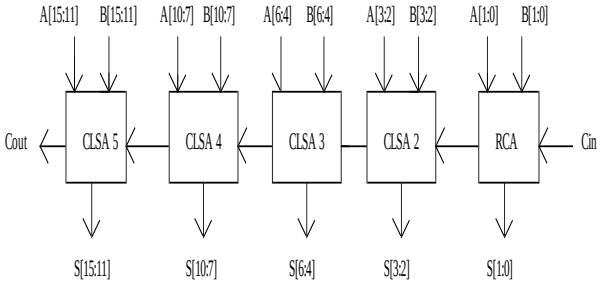

Fig 3.1 Bit Slice Structure of Proposed system

The processors used in Bit Slicing, usually include an ALU of 1, 2 , 4, 8, and 16 bits and control lines. Bit slicing died out due to the advent of the microprocessor. Nowadays it is been used in ALUs for quantum computers and had been used as a software technique. Fig 3.1 shows the bit slice structure of the proposed system. In this Ripple carry adder is used for carry generation in the initial stage. Then the 16 bit is sliced into small different bit width and assigned to the Carry select adder for the computation of carry.

IV. PROPOSED SYSTEM

This paper proposes a new CSLA that consists of combinational logic instead of the typical RCAs and MUXs used for conventional implementations In proposed system, we provide CSLA with modified FSU that In proposed system , we provide CSLA with modified FSU that reduces the usage of logic gates. The proposed architecture skips the carry computation in the first stage of each bit slice block. It is implemented for various input bit widths.The use of modified FSU in the structure instead of previous FSU , further reduces the number of LUTs used in the structure and increase the speed.

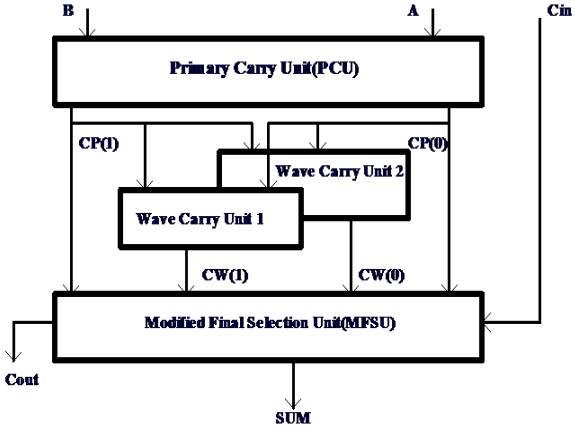

Fig 4.1 Block Diagram of Proposed System

The Fig 4.1 shows the Block diagram of a Proposed system. It consist of three functional stages such as Primary carry unit (PCU), Wave carry unit (WCU), Final selection unit (FSU). The three functional units are partitioned with the appropriate bit width. It skips the carry computation in the first stage of each bit slice block. It is implemented for various input bit widths. Two Wave carry units are work simultaneously for the inputs 0 and 1. The required carry are select by the Final selection unit (FSU). The Final selection unit requires the initial input Cin . The final sum and the Cout is calculated by the Final Selection Unit (FSU).

A. Primary Carry Unit

The PCU generates the primary carry with two inputs Aand B at an early stage. It produces output CP0 and CP1. The PCU consists of a NAND gate and OR gate for each bit and does not require Cin as a input. Thus the PCU block provide a constant delay regardless of the size of the input bit width since it is not affected by the carry input . This results has a crucial part in reduction in the overall circuit delay.

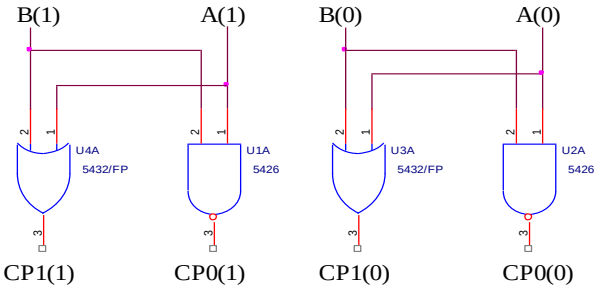

Fig 4.1Circuit Diagram of Primary Carry Unit

B. Wave Carry Unit

The two WCU units work simultaneously assuming a carry input for 0 and 1, and it is chosen at FSU by Cin. The PCU sends their outputs CP0 and CP1 to WCU0 and WCU1 respectively. WCU0 and WCU1 produce outputs as CW0 for Cin =0 and CW1 for Cin = 1, which are vertical carry propagation to FSU.

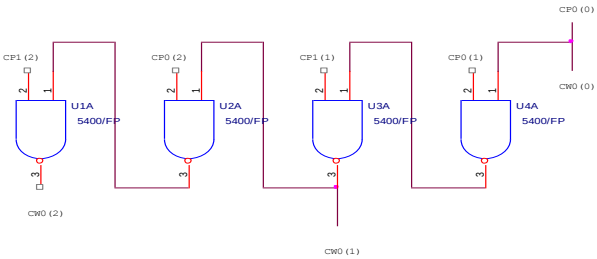

Fig 4.2 Circuit Diagram of Wave Carry Unit

C. Final Selection Unit

The FSU calculates the final outputs sum and Cout. Unlike the PCU and WCU the FSU requires the initial Cin as an input. The PCU and WCU provide input variables to the FSU. The FSU also has a constant delay regardless of size of the bit width since a bit slice logic directly produces the final output.

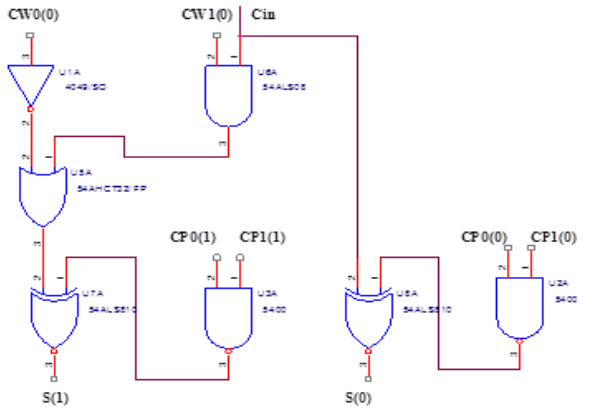

Fig 4.3 Circuit Diagram of MFSU

Fig 4.3 shows the circuit Diagram of the Modified Final selection unit. This functional stage is important in the reduction of area and the propagation delay. The number of gates which are used in the Final selection unit is reduced than the existing system structure in order to reduce the Area required and the Propagation delay. The outputs from the Wave carry unit(WCU) WCU0 and WCU1 are act as a input for the MFSU. Simple logical functions are used for the calculations of final Sum and Cout.

V. SIMULATION TOOL

Xilinx ISE Version 13.2 is the simulation tool used for the design synthesis. Verilog language is chosen for written coding. Hardware description languages , Verilog and VHDEL is a similar to software programming languages because they include ways of describing the propagation time and signal strengths. Sequential statements were placed inside a begin/end block and executed in sequential order within the block. However the blocks themselves are executed concurrently making Verilog a dataflow Languages. Verilog concept of 'wire' consists of both signal values and signal strengths . This system values allows abstract modeling of shared lines, where multiple sources drive a common net.

VI. SIMULATION RESULTS

Simulation of the carry select adder with novel MFSU structure was done using ModelSim . The Hardware Description Language used in Verilog Xilinx ISE 13.2 was used to perform the Verilog HDL compilation. The number of LUTs used in the structure is the parameter used for area analysis.

A. Area Analysis

Technique	LUTs	Slices	Logic Gates	MUXF5
CSLA with carry generation logic existing	44	25	307	4
CSLA with MFSU proposed	43	24	297	3

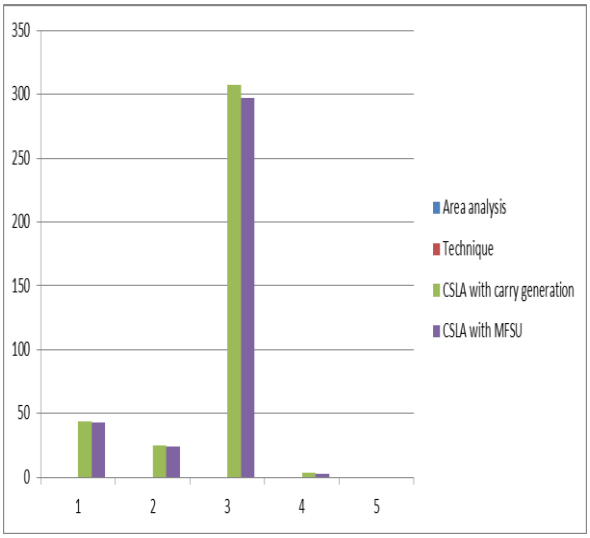

Fig 6.1 Area Analysis

B. Delay Analysis

Technique	CSLA with carry generation	CSLA with MFSU
Delay (ns)	17.722	16.525

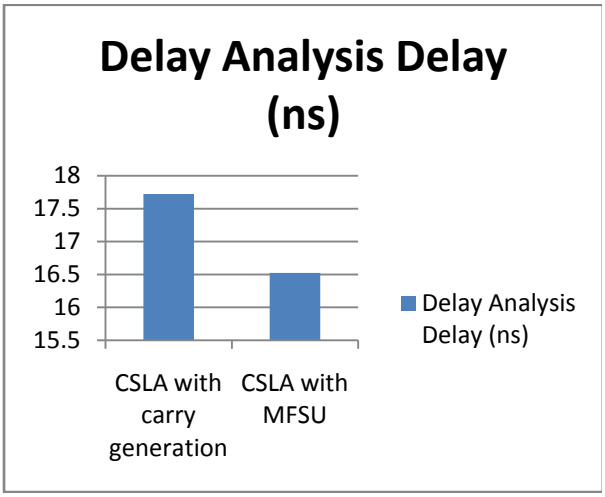

Fig 6.2 Delay Analysis

VII. CONCLUSION

Finally we assess the efficiency of the proposed CSLA by comparing their area and propagation delay with existing system structure. Because of using the modified FSU the area and the propagation delay of the proposed CSLA structure is reduced while comparing to the existing system. The result of CSLA with novel MFSU with bit slice logic produces variation in the area and propagation delay. The number of LUTs used in the proposed structure is reduced about considerable amount from the existing system. As a result the proposed CSLA reduced the computational delay by 7% and area by 4% to the conventional ones.

REFERENCES

[1] Basant Kumar Mohanty, Senior Member, IEEE, and Sujit Kumar Patel "Area–Delay–Power Efficient Carry-Select Adder" IEEE Transactions On Circuits And Systems—Ii: Express Briefs, Vol. 61, No. 6, June 2014

[2] K.K.Parhi,VLSI Digital Signal Processing. New York, NY, USA: Wiley,1998.

[3] A. P. Chandrakasan, N. Verma, and D. C. Daly, ―Ultralow-power electronics for biomedical applications,‖Annu. Rev. Biomed. Eng., vol. 10, pp. 247–274, Aug. 2008.

[4] O. J. Bedrij, ―Carry-select adder,‖ IRE Trans. Electron. Comput.,vol. EC-11, no. 3, pp. 340–344, Jun. 1962.

[5] Y. Kim and L.-S. Kim, ―64-bit carry-select adder with reduced area,‖ Electron. Lett., vol. 37, no. 10, pp. 614–615, May 2001.

[6] Y. He, C. H. Chang, and J. Gu, ―An area-efficient 64-bit square root carry select adder for low power application,‖ inProc. IEEE Int. Symp. Circuits Syst., 2005, vol. 4, pp. 4082–4085.

[7] B. Ramkumar and H. M. Kittur, ―Low-power and area-efficient carry-select adder,‖IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 371–375, Feb. 2012.

[8] I.-C. Wey, C.-C. Ho, Y.-S. Lin, and C. C. Peng, ―An area-efficient carry select adder design by sharing the common Boolean logic term,‖ inProc. IMECS, 2012, pp. 1–4.

[9] S. Manju and V. Sornagopal, ―An efficient SQRT architecture of carry select adder design by common Boolean logic,‖ inProc. VLSI ICEVENT, 2013, pp. 1–5.

[10] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd ed. New York, NY, USA: Oxford Univ. Press, 2010.