

Design of Low Power Sense Amplifier Flip Flop using GDI and FinFET Techniques

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Abstract -- This proposal is based on the analysis of basic memory elements called flip-flops. In order to achieve a design that is both highly efficient and high performance, it is necessary to take care while designing these memory elements i.e. flip-flops and latches. The proposed technique enhanced with new SAFF using GDI technique in which GDI latch has been used. The proposed method is designed with dual gate FinFET device to improve performance of this device which is most frequency used in memory devices. FinFET is a promising alternative to conventional MOSFET - which has reached its limits and has too much leakage for too little performance gain. FinFET is being recommended as the basis for future IC processes because of its power/performance benefits, scalability, superior controls over short channel effects etc. The FinFET based circuits provides better results in switching activity when compare with conventional CMOS technology. It results power efficient circuits. The new flip-flop uses a new output stage latch topology using GDI technique that significantly reduces power consumption and has improved power-delay product (PDP). In circuit implementation, transistor sizes are optimized with respect to the power delay product (PDP). The simulation results shows that the proposed method is more efficient than the conventional circuits, while considering the parameters like PDP, average power consumption, and leakage power consumption. Simulations are carried out by TANNER EDA(T-SPICE)<-SPICE and finally the power comparison is done with various flip flops.

Key words- Flip-flop, GDI, FinFET, Low Power.

I. INTRODUCTION

From the past few decades, the major challenge for the VLSI designer were area, performance, cost and power consumption. And also VLSI technology has been growing to a larger extent. All credits for this goes to the use of Integrated Circuits in Embedded Systems, Mobile Technology, Computing System etc. With ever increasing growth of technology, the demand for low power consumption is also increasing, due to high power consumption not only reliability of device is reduced but

it also makes packing and cooling of device difficult. Thus power consumption becomes major limitation for no of electronic systems. The low power interests are driven both by evolutionary and revolutionary trends. The low power requirement thus calls for global solution. The solution can be classified into two faces, supply and demand. On the supply side we need better denser and smarter batteries efficient power conversion and regulation, improved heat dissipation, distribution and cooling technique etc., on the other hand we try to reduce the demand for low power by better processes and device technique efficient computation structures design technique etc. For high performance VLSI chip-design, the choice of the back-end methodology has a significant impact on the design time and the design cost. A cell library includes a number of cells with different functionalities, where each cell may be available in several sizes and with different driving capability.

Flip-Flops are the basic storage elements used extensively in digital system designs, which adopt intensive pipelining techniques and employ several FF-rich modules such as register files, shift registers, and FIFO. The power consumption of the FFs employed in a typical digital system design, along with that of clock distribution networks, constitutes as high as 20%-45% of the total system power. FF designs are thus critical to the power consumption performance of the system design and may also considerably impact the chip area. FF designs undergo continuous improvement with the advances in new process technology. Although numerous FF designs have been developed, recent design emphases have been developed recent design switched gradually from ultrahigh speed toggling to extremely low power operations. The Gate diffusion input (GDI) is a novel technique for low power digital circuit design. This technique reduces the power dissipation, propagation delay, area of digital circuits and it maintains low complexity of logic design. The GDI circuits were implemented with much less transistors, a significant power overall power reduction was observed, while maintaining minimal performance penalty. GDI Flip-Flops were also presented, showing improvements in both area and power, compared to existing Flip Flop style.

II. REVIEWS OF EXISTING FLIP FLOP DESIGNS

In Existing system various flip flop such as TGFF, SRFF, ACFF, TCFF, LRFF were designed. Thus the design achieve circuit complexity reduction.

A. TRANSMISSION GATE FLIP FLOP

A transmission-gate-based FF (TGFF) is arguably the most widely used FF currently. One possible drawback of this design is the excessive work load on the clock signal where complementary signals are required. The consequence is the presence of a considerable dynamic power even when the data switching activity is low..

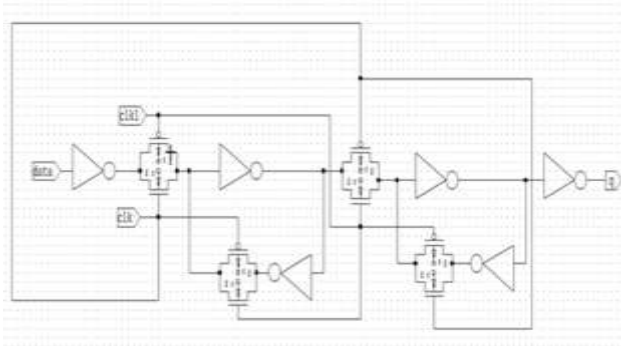


Fig. 1.TGFF

A classic master-slave-type TGFF design indicating that it comprises two TG-based latch designs. This design suffers from a high capacitive clock loading problem (a total of 12 transistors driven by the clock), which indicates a sustained power consumption even when the input remains static.

B. SET RESET FLIP FLOP

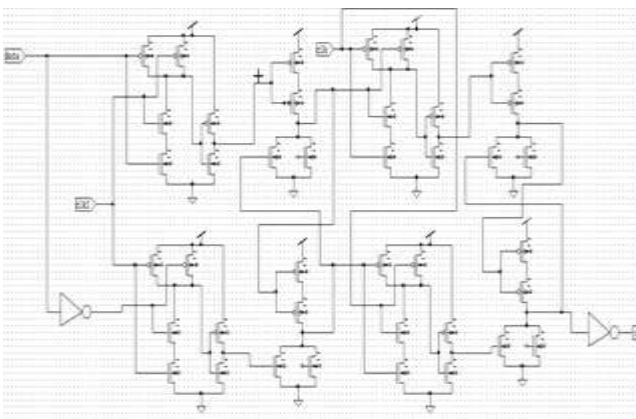


Fig. 2.SRFF

The basic building block D-flip flop is a SR Flip flop. the SR flip flop has two data inputs S & R. The s input made high to store 1 in the flip flop and R input made high to store 0 in the flip flop. In SR Flip flop a total of about 44 transistors are used. This design also suffers from high capacitive clock loading problem, so in order to overcome the problem TCFF & LRFF were designed.

C. ADAPTIVE COUPLING FLIP FLOP

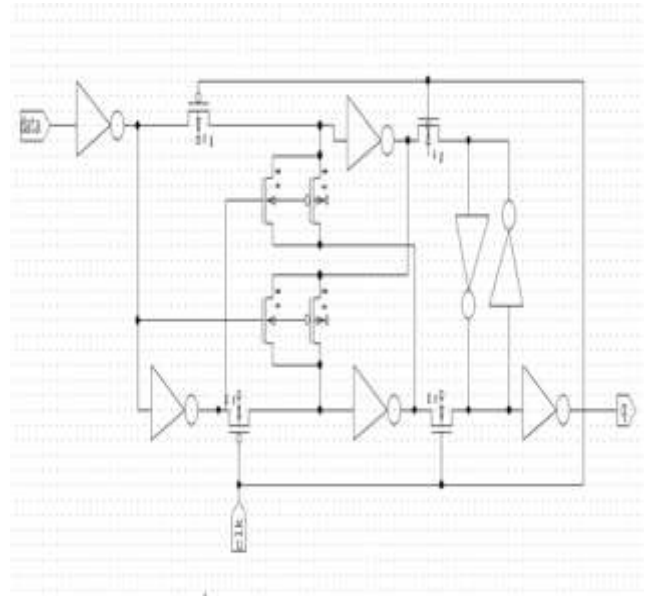


Fig. 3.ACFF

The adaptive-coupling type FF (ACFF) is based on a 6-transistor memory cell. To overcome the power consumption problem, two FF designs employing an adaptive coupling (ac) technique has been proposed. Unlike conventional TGFF designs, this design uses a differential latch structure with pass-transistor logic to achieve TSPC operation. The TGs are replaced with either n- or p-type pass transistors. To overcome the impact of process variations on the master latch, a pair of level restoring circuits is inserted into the cross coupled paths of the master latch. In this design, only four MOS transistors (two pMOS and two nMOS) are driven by the clock signal, and the transistor count is lowered to 22. A lighter clock loading in addition to the circuit simplification of the FF design can lower the power consumption significantly. In this design, the data contention problem in the slave latch deteriorates as the data switching activity increases, and the advantages of power saving are thus diminished. The level restoring circuit pair of the master latch results in a longer setup time. Moreover, this design suffers from a power leaking problem when certain input and internal node combinations occur.

D. TOPOLOGICALLY COMPRESSED FLIP FLOP

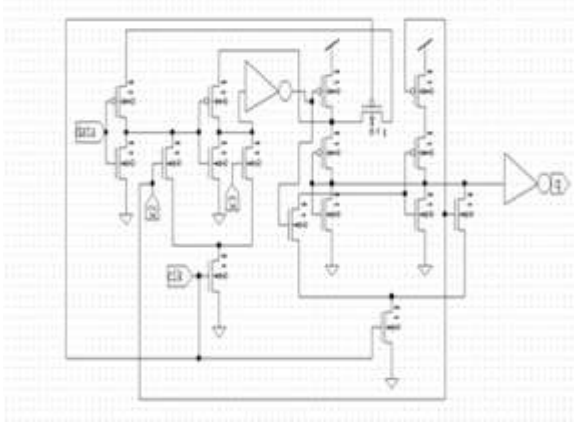


Fig. 4.TCFF

Another SR-latch-based TSPC FF design named topologically compressed FF (TCFF) obtained through a topologically compressed scheme. The master latch adopts the configuration of a MUX with feedback and can be implemented with two AND-OR-Invert (AOI) gates and an inverter. The latch is transparent when the clock signal CK is 0. The inputs pass through the AOI gates and the output of the inverter; that is, node x3 is always complementary to the input data. When CK turns 1, the contribution from the input data is blocked and x3 remains unchanged because of a closed path formed by the upper AOI and the inverter. The slave latch also comprises two AOI gates and an inverter. The complementary inputs from the master latch are fed to AND terms, which are also controlled by the clock signal, of the two AOI gates. Only one phase of the clock signal is used in this design. The TCFF design is based on three optimization principles are only a single phased clock is used and reduce the number of transistors driven by the clock reduce the total transistor count.

E. LOGIC STRUCTURE REDUCTION FLIP FLOP

The enhanced design, named logic structure reduction FF (LRFF), can be considered as an enhancement of the TCFF design in different performance aspects. This design is achieved by various optimization measures. The first measure is the logic reduction for a shorter setup time, The second one is circuit simplification for lowering the power consumption, The third one is the elimination of the node floating case to avoid the static power leaking problem. The benefit of this logic structure reduction is twofold. First, it simplifies the circuit for power saving. The second logic structure reduction scheme is applied to the second AOI gate of the master latch so the total number of transistors is only 19.

Only one single phase of the clock is required, and the fan-out for the clock signal is four (one pMOS and three nMOS transistors). When CPL is introduced, the circuit complexity of its p-logic network is largely reduced, even though the design is not a dynamic logic.

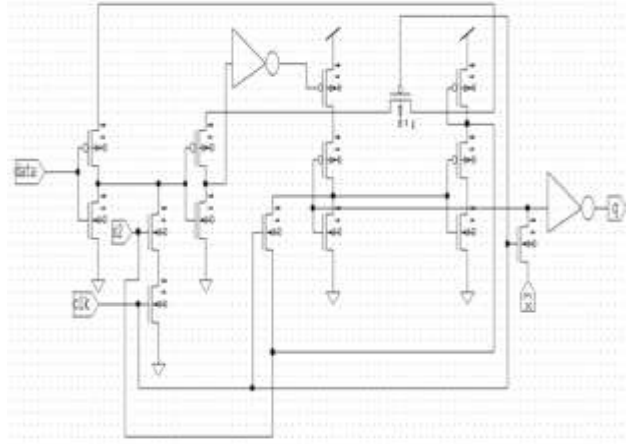


Fig. 5.LRFF

III. PROPOSED METHODOLOGY

The proposed methodology designed with GDI and FinFET structure is shown in the figure 6. A new Sense amplifier flip flop designed of about 14 transistors with DGPMOS and DGNMOS in which input is given to the gate of the transistors rather than drain terminal. This consumes almost very less power than existing methods.

A. SENSE AMPLIFIER FLIP FLOP

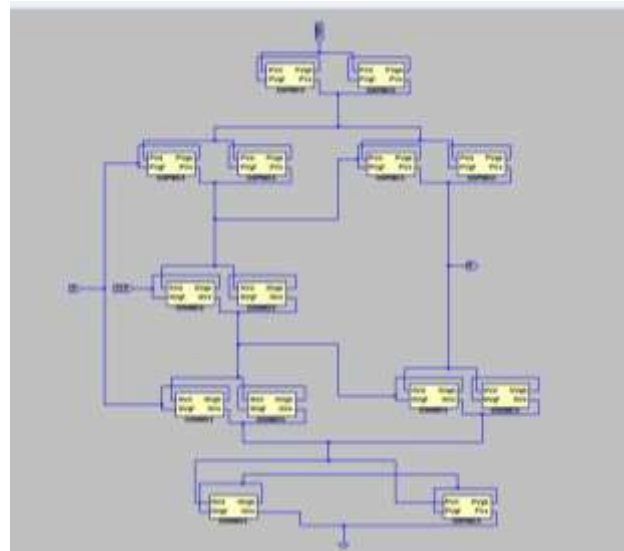


Fig 6.SAFF

SAFF flip-flop consists of two stages: a pulse generator (PG) and a slave latch (SL). The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage. Sense Amplifier based Flip-flop (SAFF) is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch, depending whether the output is to be set or reset. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value.

IV.SIMULATION RESULTS

The simulation results were obtained from TSPICE in 180nm CMOS process at room temperature VDD is 1V. Various flip flops with schematic waveform were designed and power comparison done for each flip flop.

Total no of Transistors: The total number of transistors is measured which contribute more area and power consumption in the integrated circuit design.

Power: It is the total power consumption of flip flop in terms of μw (micro watt).the maximum power denotes the maximum power consumption of flip flop. The minimum power describe the minimum power requirement to trigger the flip flop. The simulation result for various flip flops are given below,

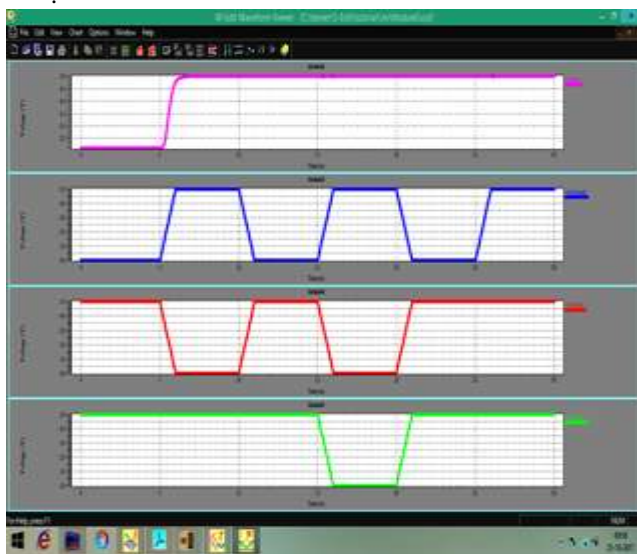


Fig.7.Output waveform of TGFF

The waveform of TGFF is shown in the Fig 7. When the data is apply '1' at the time of clock as rising edge is also 1 then clk1 is '0', then the output of Q is '0'and the next state output will become '1'. because it act as the D flip flop operations.

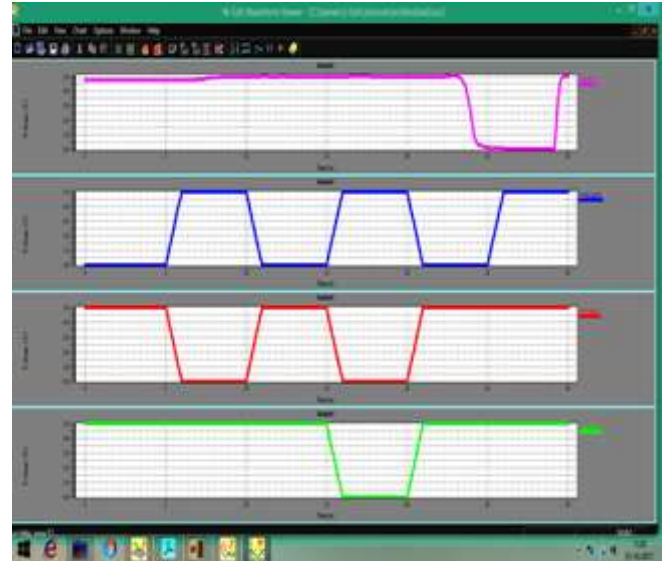


Fig 8.Output waveform of SRFF

The waveform of SRFF is shown in the Fig 8. When the data is apply '1' at the time of clock as rising edge is also 1 then clk1 is '0', then the output of Q is '1'and the next state output will become '0'.

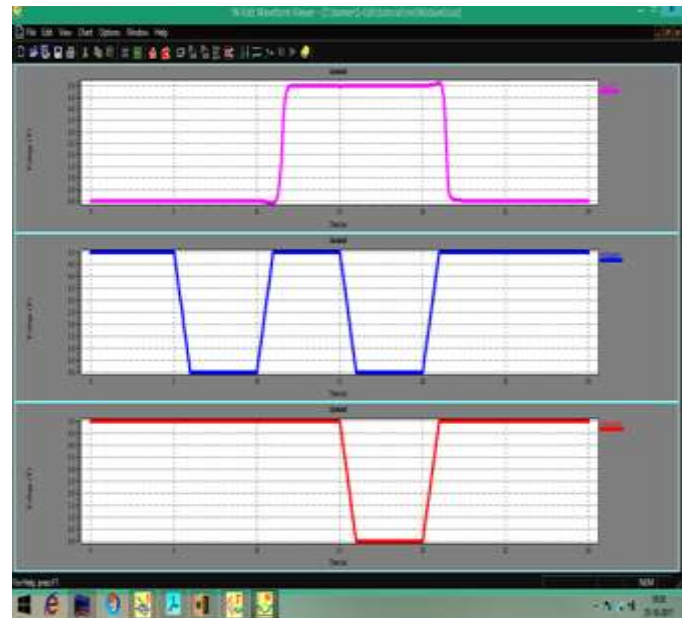


Fig 9.Output waveform of ACFF

The Fig 9 shows that waveform for ACFF. when the data apply is '1', the clock is high, the output Q obtained is '0'.

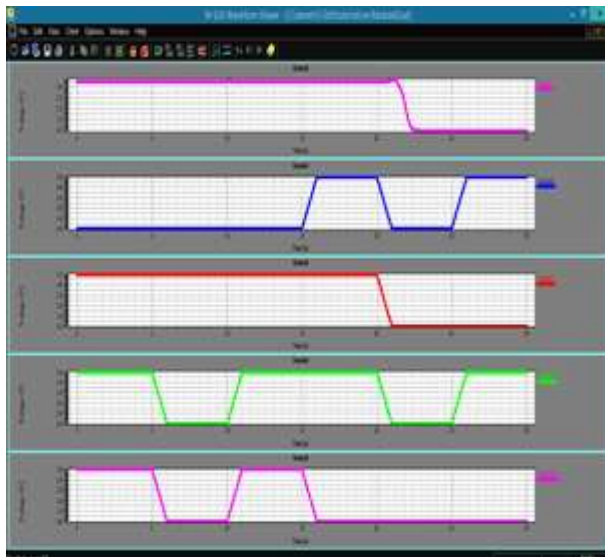


Fig 10. Output waveform of TCFF

The waveform of TCFF is shown in the Fig 10. When the data is apply '1' at the time of clock as rising edge is also 1, the additional inputs such as x2 is high and x3 is the complement of x2, then the output of Q is '1' and the next state output will become '0'. because it act as the D flip flop operations.

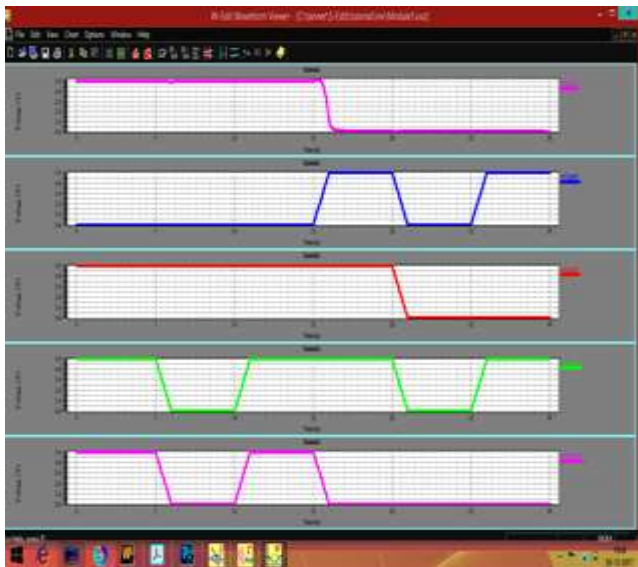


Fig.11. Output waveform of LRFF

The waveform of LRFF is shown in the Fig 11. When the data is apply '1' at the time of clock as rising edge is also 1, the additional inputs such as x2 is high and

x3 is the complement of x2, then the output of Q is '1' and the next state output will become '0'. because it act as the D flip flop operations.

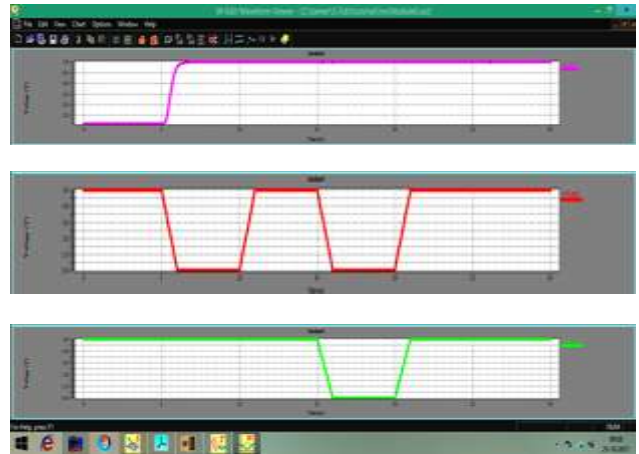


Fig.12. Output waveform of SAFF

The waveform of SAFF is shown in the Fig 12. When the data is apply '1' at the time of clock as rising edge is also 1, then the output of Q is '0' and the next state output will become '1'. because it act as the D flip flop operations.

Table I. Power comparison table

Flip flops	SRF F	ACF F	TCF F	TGF F	LRFF	SAFF
No. of transistors	44	22	21	20	19	14
Average Power (Watts)	6.57	4.64	4.32	4.18	3.55	2.38
Max. Power (μ Watts)	4.26	3.25	3.14	3.02	2.39	1.24
Min. Power (μ Watts)	2.31	1.39	1.18	1.16	1.16	1.14

The Table I shows the power analysis in different types Flip-Flops such as TGFF, SRFF, ACFF, TCF, LRFF, SAFF is compared with average, maximum, minimum power in watts. From this design methods various parameters are tabulated and compared. The parameters compared are number transistors used in each design of flip-flops and power consumption by flip-flops. From this sense amplifier flip flop with 14 transistors consume less power than other flip flops. Fig13 shows the comparison chart of six flip flops which denotes the average power, maximum power and the minimum power of TGFF,SRFF,ACFF,TCFF,LRFF,SAFF.

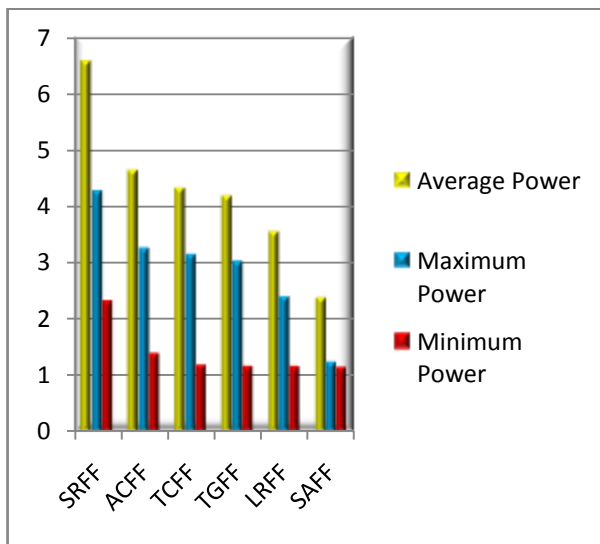


Fig.13 Power Comparison Chart

In this chart various flip flops such as TGFF, SRFF, ACFF, TCF, LRFF, SAFF were charted with respect to average power, minimum power, maximum power. Hence power consumed is low in SAFF when compared to other flip flops. In proposed method the power consumed is very much low when compared to the existing methodology and as well as transistor count is effectively reduced.

V.CONCLUSION

In this proposal, the various Flip flops design like TGFF, SRFF, ACFF, TCF, LRFF, SAFF were designed. These flip-flop were been designed in Tanner tool, and with LT-Spice the resulting waveforms and layout for those flip flops are also obtained. The comparison table also added to verify the designed methods. In this proposed design a Flip flop is designed with GDI technique using dual gate FinFET device. This method is designed to reduce area (number of transistors), and to reduce power consumption of the circuit. While using GDI technique the number of transistor required

designing a flip flop is reduced obviously. To reduce the power consumption the dual gate FinFET device is used. Then the resulting circuit consumes less power than the conventional circuit. Hence, proposed design proved to be better as compared to modified design in terms of power consumption, PDP as well as area. FinFETs stand poised to enable the next big leap for computer, communications, and consumer devices of all types. FinFETs have attractive qualities, such as excellent control of short channel effects, the ability to tune their performance for energy efficiency or performance, which means they can be used as the basis of flexible SoC processes.

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