SSRG International Journal of Electronics and Communication Engineering
ISSN: 2348-8549/ https://doi.org/10.14445/23488549/IJECE-V13I9P105

Volume 13 Issue 9, 74-82, September 2026

Original Article

Carbon Nanotube Field Effect Transistor based Voltage Differencing Inverting Buffered Amplifier with Enhanced Analog Performance

Manoj Kumar Tomar[1], Vimlesh Singh[1], Laxya[2*]

[1]*Department of ECE, SET, MRIIRS, Faridabad, India.*
[2]*Department of ECE, Maharaja Agrasen Institute of Technology, Delhi, India.*

[2*]*Corresponding Author : laxya.singla@gmail.com*

Received: 02 March 2026 Revised: 25 March 2026 Accepted: 11 September 2026 Published: 29 September 2026

Abstract *- This article describes how to develop and operate a Voltage Differencing Inverting Buffered Amplifier (CNTFET-VDIBA) using Carbon Nanotube Field Effect Transistors (CNTFETs). It utilizes the superior characteristics of CNTFETs to facilitate enhanced transconductance, a wideband range of operation, and a low power demand compared to conventional CMOS alternatives. The effect of increasing numbers of CNTs on device performance was thoroughly studied and characterized. Simulation results specify that by increasing the number of CNTs significantly improves transconductance. The proposed VDIBA, CNT has the highest transconductance of around 1.32mS, while maintaining the high BW. The 3-db BW was observed to be 7.9 GHz, enabling this proposed VDIBA to apply for high-frequency analog signals. These results demonstrate that CNTFET-based VDIBA is a feasible substitute to CMOS, providing ultra-low power consumption, scalability, and high-performance analog building blocks for future integrated circuits.*

Keywords *- Carbon nano tube, ABB, VDIBA, Power efficient, Low power, Current mode, CMOS.*

1. Introduction

Analog Building Blocks (ABBs) represent the basic elements for designing analog and mixed-signal integrated circuits. Data conversion, signal processing, sensor interface, and voltage-differencing amplifiers are just a few of the various uses for current conveyors, operational amplifiers, and buffered amplifiers. The performance of ABBs determines the overall efficiency, speed, power consumption, and scalability of analog systems. However, traditional silicon technology used to fabricate ABBs using Complementary Metal-Oxide-Semiconductor processes encounters serious scaling limits with nanoscale dimensions. As a result, great efforts have been made within the research community to find new semiconductor materials and device architectures that can offer better analog performance while maintaining compatibility with the existing fabrication Technology available in the industry or research organization of the world. Among these new technologies, carbon nanotube field-effect transistors have become popular amongst researchers in recent years. CNTs are cylindrical nanostructures composed of rolled graphene sheets. Due to quasi-one-dimensional geometry, CNTs show exceptional electrical properties combined with high mechanical strength, making them highly promising for future electronic applications. Because of these advantageous characteristics, CNTFETs are particularly applicable for low-power, low-voltage analog devices. Compared to their silicon MOSFET counterpart, CNTFETs provide a significant improvement in the current drive capability, on/off current ratio, and linearity of the whole device while supplying voltages considerably lower than 1 V. This potential of reduced power dissipation and boosted performance meets the increasing demand of energy-efficient and high-frequency analog building blocks in current and future integrated circuits. Among the various materials and device structures proposed so far, CNTFETs are particularly important for analog circuit design due to their unique electrical and structural features, along with the thermal properties. Transistors based on CNTs exploit exclusive features such as high carrier mobility and substantial current-carrying capability, which differentiate CNTFETs from traditional metal-oxide-semiconductor field-effect transistors. Analog circuits demand devices that offer high linearity, wide bandwidth, and improved noise performance, and CNTFETs have demonstrated strong potential in meeting these requirements in recent literature.

Unlike their digital counterpart, analog building blocks like amplifiers, filters, and current mirrors do benefit from the favorable electrical behavior and scalability of carbon nanotubes. The tunable electronic properties of the CNTs,

including the chirality and diameter, make for variable performance that can be used in order to optimize the analog operation at the nanoscale level. Extensive research on analog building blocks using CNTFET technology deals with modeling, implementation, and comparative assessments of basic analog circuits built with CNTFETs, identifying both benefits and existing challenges compared to traditional CMOS analog blocks.

The results try to validate the viability of CNTFETs for use as base components in future analog and mixed-signal integrated circuits. In comparison to their conventional CMOS counterparts, CNTFET-based analog circuits, for example, current conveyors, voltage-differencing amplifiers, as well as operational transconductance amplifiers which have demonstrated superior gain, bandwidth, and power-efficiency figures of merit in very recent studies. One particularly important ABB has been identified as the Voltage Differencing Inverting Buffered Amplifier because it incorporates a voltage-differencing stage with buffered and inverted output, enabling a variety of analog signal processing applications.

Recent research has also investigated CNTFET implementations of voltage-differencing analog building blocks. Sunca Ulusoy and Alçı reported a low-voltage CNTFET-based VDIBA and demonstrated its use in a universal filter. This work confirms the suitability of CNTFETs for VDIBA architectures but also indicates that performance depends strongly on the selected nanotube chirality, number of tubes, supply voltage, bias current, and device-model assumptions. Other studies have developed CMOS, FGMOS, bulk-driven, and adaptive-biased VDIBA structures [18-22]. Nevertheless, a systematic study of the effect of CNT count on VDIBA transconductance, bandwidth, power consumption, and linearity under a clearly specified CNTFET simulation methodology remains limited. The objective of this work is therefore to evaluate a CNTFET-based VDIBA using a 32-nm device configuration and to quantify the effect of the number of nanotubes on its principal analog parameters

2. Circuit Description of CNT-VDIBA

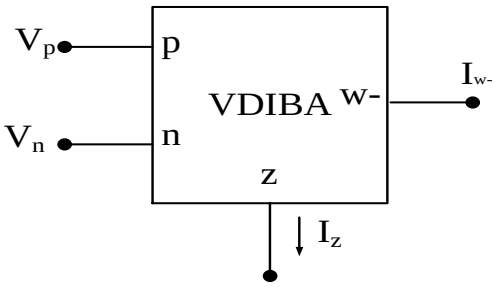
Sumio Iijima originally introduced Carbon Nanotubes (CNTs) in the early 1990s, are nanoscale cylindrical structures consisting of a rolled-up single layer of graphene, essentially a sheet of graphite, into a seamless tubular shape [12]. The CNTFET-based VDIBA represents an advanced analog circuit element that utilizes the unique Electrical characteristics of CNTFETs to deliver enhanced power efficiency, high operational speed, and compactness. Integration [13].

The input stage uses a differential pair of CNTFETs, which evaluates the voltage difference between the two input nodes and converts that difference into a corresponding current, as shown in Figure 1(a) [14]. This current is then inverted and routed via a CNTFET-based current mirror circuit, ensuring accurate current replication with minimum losses. The output buffer produced by the CNTFET converts current into a voltage signal, allowing for easy transfer to the next stage in the circuit due to a low output impedance.

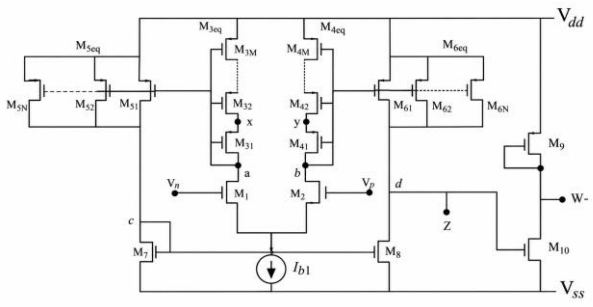
Figure 1(b) represents the conventional VDIBA implementation in Gupta et al. [15]. In the proposed CNT-VDIBA design, the differential input pair is formed by incorporating CNTFETs, where M1 and M2 represent the CNT-based differential pair.

Due to the ability of CNT devices to provide superior electrical properties, current mirror circuits formed by CNTFET arrangements in pairs M3 through M5, M4 through M6, and M7 through M8 will be able to accurately replicate their input current and provide improved electrical performance over their silicon counterparts. The inverting buffer stage is constructed with CNTFETs M9 and M10 [15], which offer low distortion and wider bandwidth characteristics.

By replacing conventional CMOS-MOSFETs with CNTFETs, the proposed CNT-VDIBA achieves enhanced transconductance, improved current driving capability, and greater efficiency, while still maintaining low power consumption, as shown in Table 2. This design takes advantage of the superior performance characteristics of carbon nanotubes, making the circuit well-suited for advanced analog signal processing applications.



(a)



(b)

Fig. 1 (a) VDIBA circuit symbol, and (b) CMOS VDIBA [15].

The following describes the VDIBA's terminal features [15].

$$\begin{bmatrix} I_p \\ I_n \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \\ I_{w-} \end{bmatrix} \quad (1)$$

The transconductance (g_m) is electronically tunable through bias currents. The g_m [2] is represented as follows:

$$g_m = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} I_b} \quad (2)$$

C_{ox} is defined as "gate-on oxide capacitance" for a unit area, and μn represents "effective carrier mobility" in this context. The effective channel width of the differential Metal Oxide Semiconductor transistor is represented by the letter W, and its effective channel length is represented by the letter L. Last but not least, I_b denotes the "bias current" that passes through the transconductance stage [16].

3. Design Considerations and Analysis

Figure 2 displays the design scheme for the CNT-VDIBA. The CNT replaces the conventional VDIBA, providing an improvement in transconductance through the electrical properties of CNTFET.

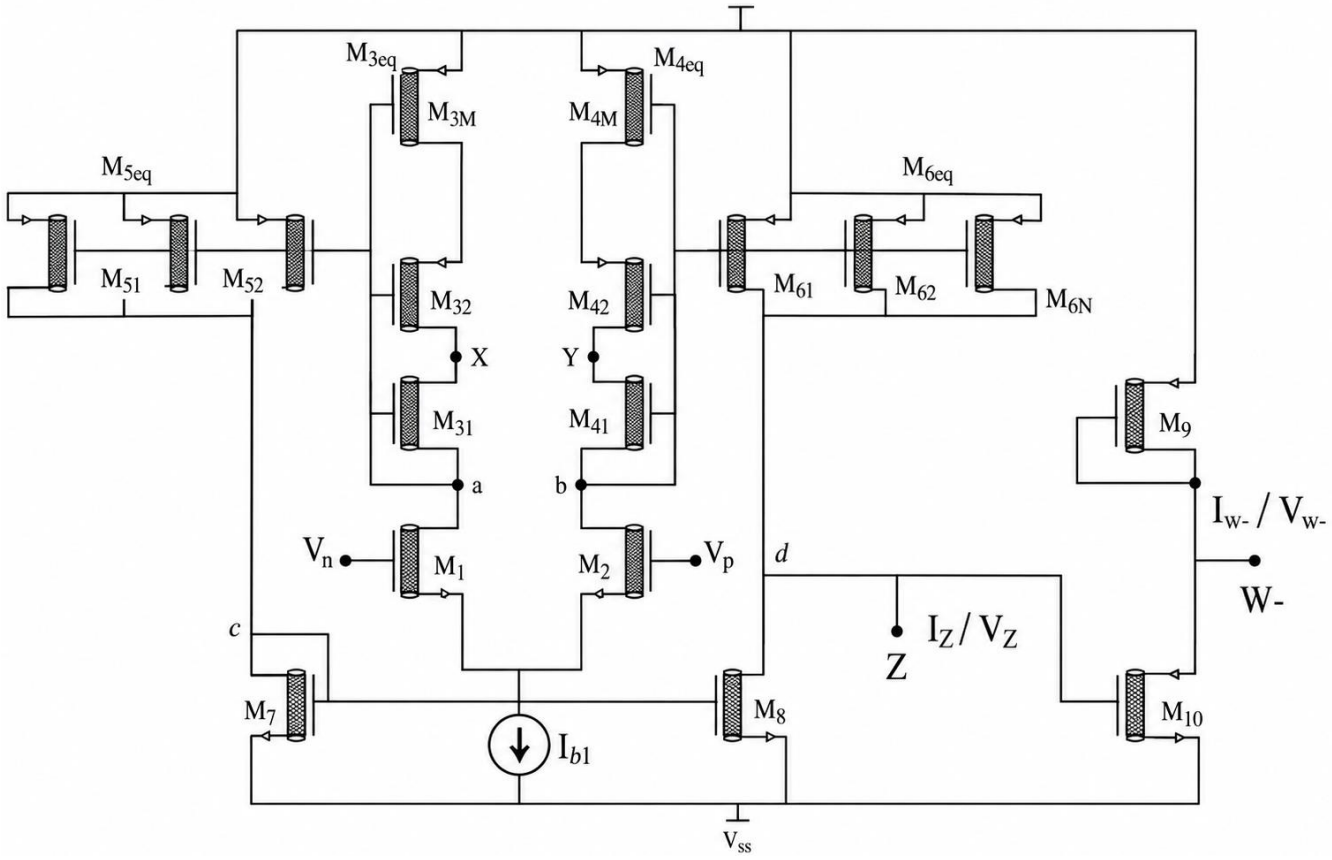


Fig. 2 Implementation of the proposed CNTFET-VDIBA

D_{CNT}" which is the carbon nanotube diameter in nano meters, "Eg" is the bandgap energy, and "e" is electron of the nanotube that is linked to its chirality vector indices "(n, m)" by [3] and A=2.49A°

$$D_{cnt} = \frac{A\sqrt{(n^2+m^2+mn)}}{\pi} \quad (3)$$

$$W = (N-1) * S + D_{cnt} \quad (4)$$

Where "S" is the distance between two CNT or Inter CNT,

N is No. of Carbon Nanotube, "W" is the width of CNT

4. Simulation Results

Simulation Methodology: The proposed CNTFET-VDIBA was simulated using HSPICE with the Stanford 32 nm CNTFET compact model. The supply voltage was maintained at ±0.6 V, and the bias current was fixed at 50 μA. The CNTFET threshold voltage was approximately 0.29 V (as defined by the adopted compact model). Unless otherwise specified, all simulations were performed at a temperature of 27 °C (300 K). AC analysis was carried out over a frequency range of 1 Hz to 10 GHz to extract the transconductance and

3-dB bandwidth characteristics. These conditions were used to obtain the reported 7900 MHz bandwidth.

The final results of simulation from the newly designed CNT-based VDIBA prototype will be compared to the previously designed CMOS-based VDIBA in [15] and the original CMOS circuit based upon the original CMOS technology node parameters with a 32 nm CNTFET technology node using SPICE simulations. The CNTFETs are driven by ±0.6 V power sources with an unchanged bias current, which is 50 µA for all simulation runs, as shown in Table 1.

$$FOM_{gm/p} = 1320\mu s/25\mu W = 52.8\mu s/\mu W \quad (5)$$

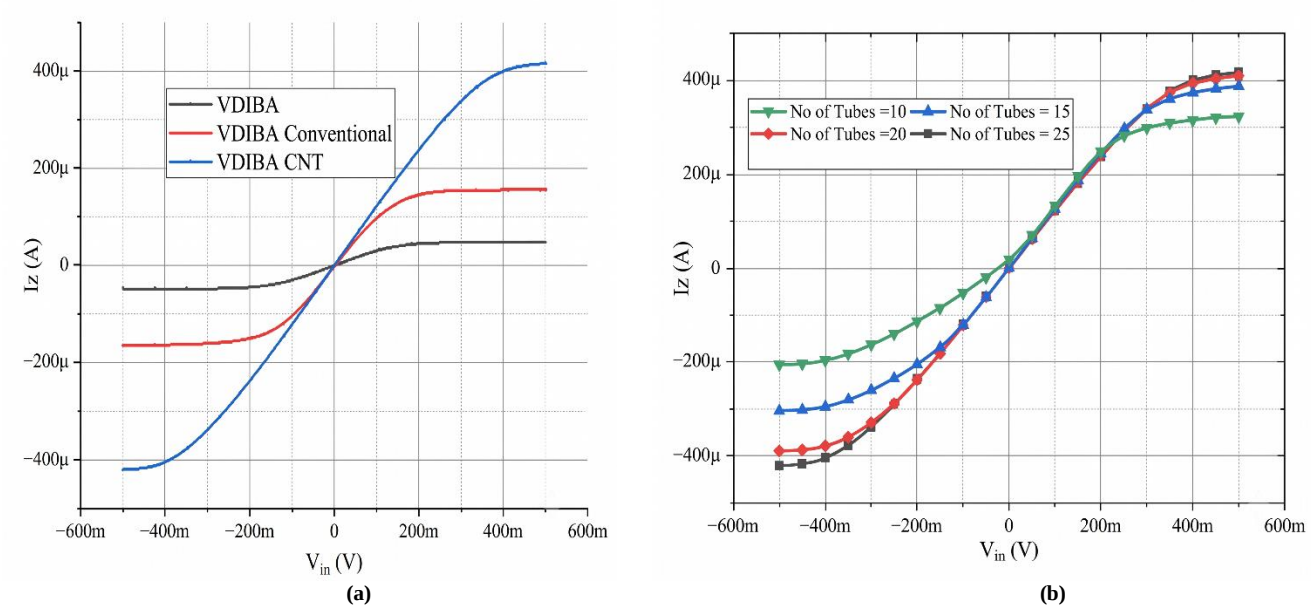
Table 1. CNTFET technology parameters, the device dimensions

Transistor.	Number of Carbon Nanotubes (N).	Chirality of tube (m, n).	Physical Channel Length (L_{ch}).	Inter-Pitch CNT(S).	High-k dielectric.
M_1-M_2, M_{31}-M_{3M}, M_{41}-M_{4M}, M_{51}-M_{5N}, M_{61}-M_{6N}, M_9-M_{10}	25	(19,0)	32nm	20nm	16
M_9-M_{10}	5	(19,0)	32nm	20nm	16

The Figure of Merit is shown in Equation (5).

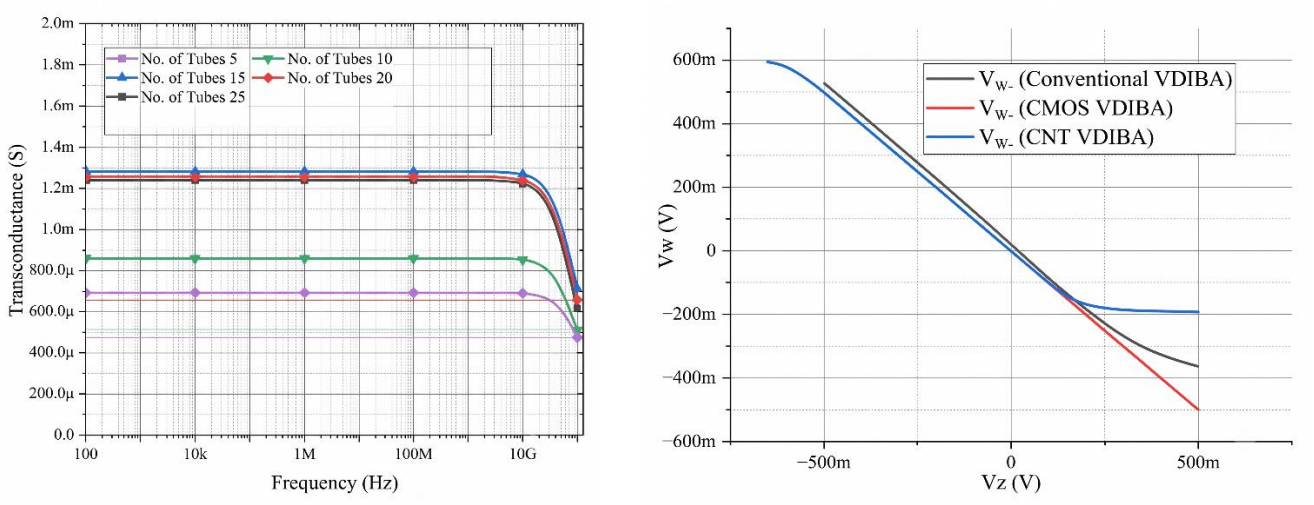
The characteristics of a new device based on carbon nanotubes, a CNT-VDIBA (a virtual digital integrated circuit), are shown in Figure 3(a). Figure 3(a) shows the output current (Iz) that is produced whenever a +ve voltage is connected to +ve node (V_p) and -ve node (V_n), which is grounded. Output voltage (V_w) and voltage at the intermediate node (Iz) have a linear relationship, as shown in Figure 3(b). For the voltage range in which the CNT-VDIBA can function in a realistic application, the input voltage has a linearity of ±500mV.The transconductance of the CNT. As illustrated in Figure 4(a), the performance of the VDIBA is dependent on the number of carbon nanotubes employed in the CNT-VDIBA implementation. For N≥ 25, the transconductance attains its maximum value. Furthermore, Figure 4(b) indicates that the linear operating range of the inverting buffer extends to approximately ±500 mV.

The ideal V_w−characteristic is included to represent the expected behaviour of an ideal inverting buffer [17], while the remaining curves compare the responses of the proposed CNT-VDIBA and the conventional VDIBA. This comparison demonstrates the enhanced linearity and reduced deviation from the ideal response achieved by the proposed design.



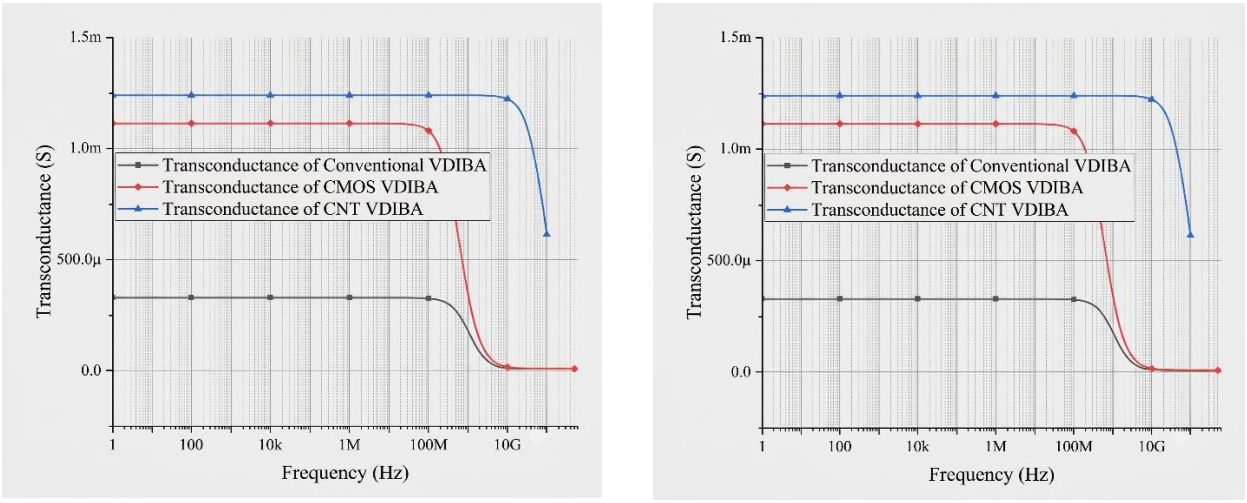
(a) **(b)**

Fig. 3 (a) Variation of Iz with Vin, and (b) Variation of Iz at different no. of carbon nanotubes with V_{in}.



(a) **(b)**

Fig. 4 (a) Variation of transconductance at different no. of carbon nanotubes with frequency, and (b) Variation of Vw with Vz.



(a) **(b)**

Fig. 5 (a) Variation of transconductance with frequency, and (b) Voltage buffer with frequency.

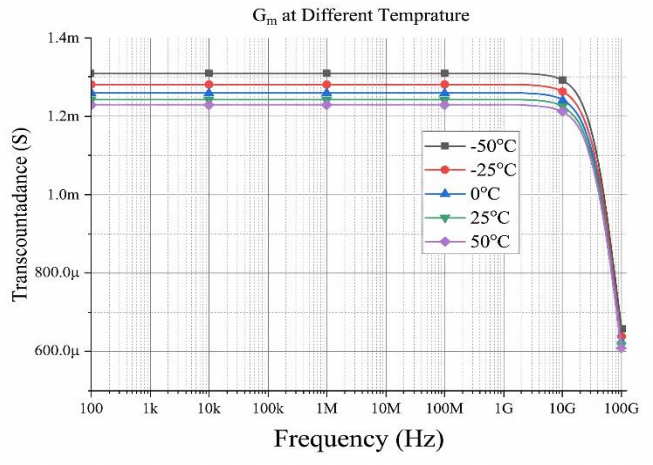


Fig. 6 Variation of transconductance at different temperature with frequency

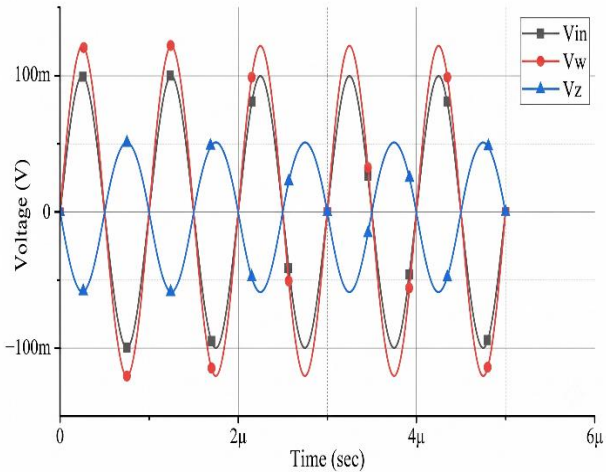


Fig. 7 Transient analysis of the proposed VDIBA circuit

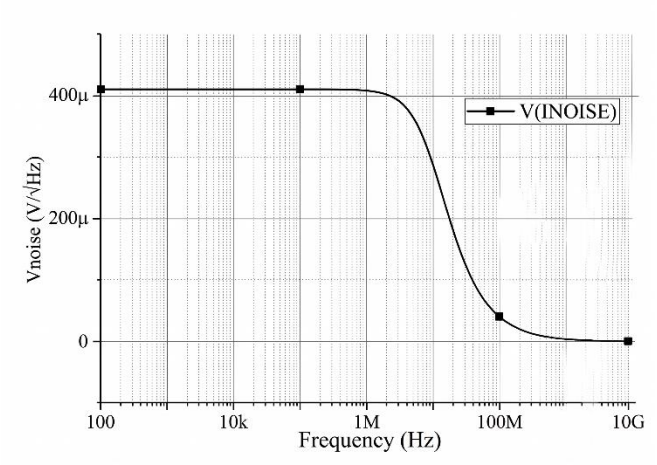


Fig. 8 Variation of input noise with frequency

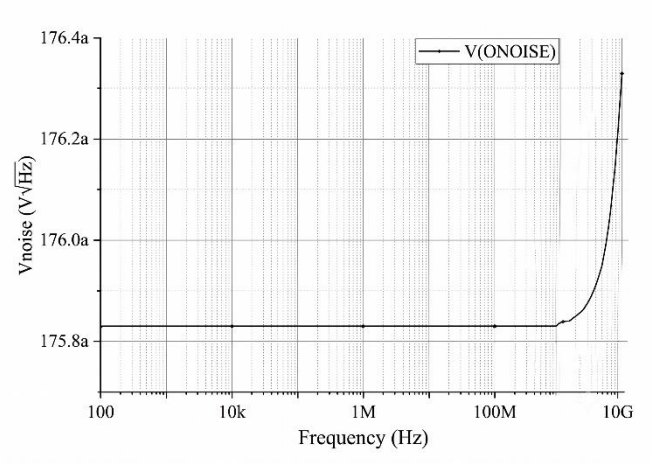


Fig. 9 Variation of output noise with frequency

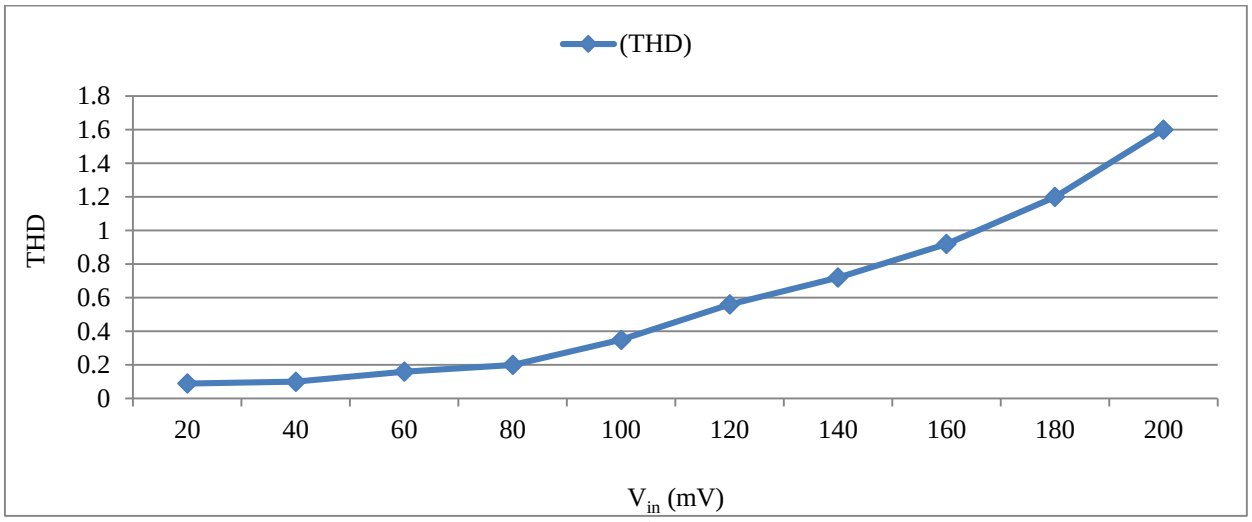


Fig. 10 Variation of THD with V_{in}

Figure 5(a) represents Transconductance of the desired circuit with frequency, while Figure 5(b) illustrates Voltage gain at the intermediate stage of the circuit. In Figure 6(a) Transconductance is measured at different temperatures so that optimization of the circuit is done. The characteristics of the suggested VDIBA circuit in time domain is represented in Figure 7. The suggested CNT-VDIBA circuit was given an excitation of 200mVpp/1MHz input source, and the output voltages V_z and V_{w-} plotted in Figure 7. The observed values of noise from simulations are quite low as compared to Conventional VDIBA, represented in Figure 8 & Figure 9. Total Harmonic Distortion (THD) is a critical metric for evaluating circuitry performance. As depicted in Figure 10, there is a direct correlation between THD and change in input voltage (V_{in}) at an input signal frequency of 1 MHz. The linear relationship continues until approximately V_{in} = 0.025. For all other lower input voltages, THD remains 1.6. In addition to comparing THD with respect to input voltage, performance optimization on CNTFET can be done by altering the quantity of CNT tubes denoted by N, tube diameter denoted by DCNT and pitch denoted by S. Figure 11 (a) and Figure 11(b) provide graphs illustrating the consequence of different tube counts on the efficiency metrics of CNTFET-VDIBA. As shown in Figure 12, the power consumption associated with CNTFET-VDIBA is significantly less than that for standard CMOS.

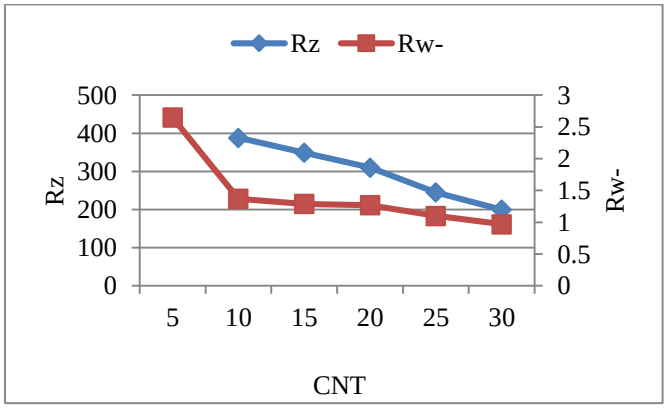


Fig 11(a) Variation of R_Z and R_{W-} with no. of CNT

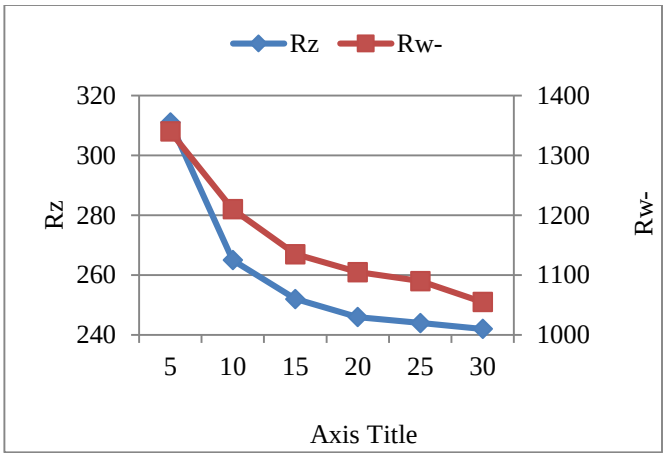


Fig. 11 (b) Variation of R_Z and R_{W-} with inter-pitch

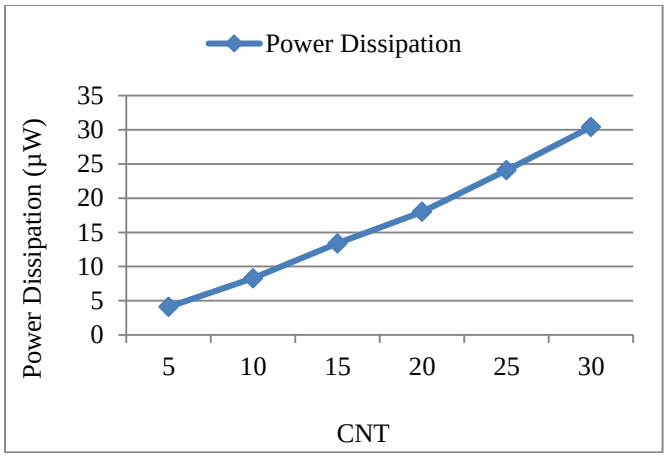


Fig 12. Power dissipation variation with respect to the number of CNT

Table 2. Performance parameters of different structures, comparison of CMOS-based VDIBA and CNT VDIBA

Reference no.	Technology (nm)	Power Supply (V)	No of Transistors	Passive components	Linear input voltage range of TA (mV)	Linear input voltage range of Buffer (mV)	Transconductance (µS) at bias current (IB)(µA)	Inverting buffer transfer ratio	3dB of TA (MHz)	3dB of inverting Buffer (MHz)	Power consumption (µW)	THD (%)
17	32	± 0.3	6	1	± 100	± 100	15.823 at I_B = 50	-	-	-	14.32 µW	-
18	90	± 0.6	12 MOS	3 Resistor	± 50	- 500 to 200	3.58 x 10^3 at I_B = 220	0.94	334	3750	4.54	3.2
19	180	± 0.75	5 MOS	1 FGMOS	± 250	- 750 to 500	582 at I_B = 100	0.98	92.47	1580	1.5	< 1
20	180	± 0.4	13 MOS	2 FGMOS	± 300	- 400 to 160	223 at I_B = 50	0.98	1124	2350	0.569	-----
13	180	± 0.6	12 MOS	2 Resistor	± 500	----	1024 at I_B = 150	1.07	263	----	0.56	0.4
21	180	± 0.7	6	0	± 400	----	149 at I_B = 100	0.96	2000	5600	1.3	-----
22	180	± 0.9	20	----	± 150	± 200	3100 at I_B = 50	1.10	437	2500	3.1	0.49
Proposed work	32	± 0.6	14	0	± 600	± 600	1320 at I_B =50	.995	**7.9 GHz**	1700	25 µW	1.6

This block was not designed using CNTFET technology. Therefore, its performance was compared with that of existing technologies, and the results demonstrate that the proposed block achieves better performance in terms of the evaluated parameters.

5. Comparison and Discussion

Table 2 presents a comprehensive survey of existing literature to provide an overview of key performance metrics. To the best of the authors' knowledge, all pertinent structural and design parameters from the referenced works have been incorporated. However, direct quantitative comparison is constrained by disparities in supply voltages, technology nodes, device dimensions, and biasing conditions across the reported implementations. The proposed circuit preserves the fundamental VDIBA architecture while replacing conventional CMOS devices with CNTFETs. Therefore, the observed improvements in transconductance, bandwidth, and power efficiency should primarily be attributed to the superior device characteristics of CNTFET technology, including higher carrier mobility, improved current-driving capability, and reduced parasitic effects, rather than to a fundamentally new circuit topology. Although the proposed implementation demonstrates the practical advantages of employing CNTFETs in VDIBA realization, the present work does not independently quantify the relative contributions of circuit architecture and device technology. A rigorous decomposition of these effects would require implementing identical VDIBA architectures using both CMOS and CNTFET technologies under the same technology node, supply voltage, bias current, loading conditions, and simulation environment. Such a controlled comparative study is beyond the scope of this work and is considered an important direction for future research.

6. Conclusion

A novel transconductance-enhanced CNTFET-based VDIBA is proposed in this work. The performance improvements of the proposed CNT-VDIBA are validated through SPICE simulations using 32 nm technology parameters. Simulation results indicate that the circuit achieves a transconductance of up to 1.32 mS, with a 3 dB bandwidth of 7900 MHZ at a bias current of 50 µA. These results reflect a significant enhancement in transconductance, with a marginal reduction in bandwidth compared to the conventional VDIBA. Furthermore, the proposed design exhibits improved DC gain, enhanced linearity, and better power efficiency relative to the traditional VDIBA structure. The proposed CNT-VDIBA exhibits a Total Harmonic Distortion (THD) of 1.6. Additionally, the architecture demonstrates low power consumption while achieving enhanced DC gain, improved linearity, and superior power efficiency.

List of Abbreviations

CNT = Carbon Nano Tube.
ABB = Analog Building Block.
THD = Total Harmonic Distortion.
CMOS = Complementary Metal-Oxide-Semiconductor.
CNTFET = Carbon Nano Tube Field Effect Transistor.
NR=Not Reported

Availability of Data and Materials

This article includes required data and supportive information.

Conflict of Interest

There is no conflict of interest, financial or otherwise, as declared by the authors.

References

[1] D. Biolek et al., "Active Elements for Analog Signal Processing: Classification, Review, and New Proposals," *Radio Engineering*, vol. 17, no. 4, 2008. [Google Scholar]

[2] K.C. Smith, and A. Sedra, "The Current Conveyor—A New Circuit Building Block," *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1368-1369, 1968. [CrossRef] [Google Scholar] [Publisher Link]

[3] Laxya et al., "CNFET Based Voltage Differencing Transconductance Amplifier," *IOP Conference Series: Materials Science and Engineering*, vol. 225, pp. 1-7, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[4] Norbert Herencsar et al., "New Resistorless Tunable Voltage-Mode Universal Filter using Single VDIBA," *Analog Integrated Circuits Signal Processing*, vol. 76, no. 2, pp. 251-260, 2013. [CrossRef] [Google Scholar] [Publisher Link]

[5] C. Toumazou, F.J. Lidgey, and D.G. Haigh, *Analogue IC Design: The Current-Mode Approach*, Institution of Engineering and Technology, pp. 1-666, 1993. [CrossRef] [Google Scholar] [Publisher Link]

[6] Jie Deng, and H.S. Philip Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application-Part I: Model of the Intrinsic Channel Region," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3186-3194, 2007. [CrossRef] [Google Scholar] [Publisher Link]

[7] Jie Deng, and H.S. Philip Wong, "A Circuit-Compatabile Spice Model for Enhancement Mode Carbon Nanotube Field Effect Transistor," *2006 International Conference on Simulation of Semiconductor Processes and Devices*, Monterey, CA, USA, pp. 166-169, 2006. [CrossRef] [Google Scholar] [Publisher Link]

[8] Jie Deng, and H.S. Philip Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3195-3205, 2007. [CrossRef] [Google Scholar] [Publisher Link]

[9] Ale Imran et al., "Optimized Design of a 32-nm CNFET-Based Low-Power Ultrawideband CCII," *IEEE Trans Nanotechnology*, vol. 11, no. 6, pp. 1100-1109, 2012. [CrossRef] [Google Scholar] [Publisher Link]

[10] Seema Jogad et al., "CNTFET Based Class AB Current Conveyor: Design, Analysis and Waveform Generator Applications," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 34, no. 1, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[11] Seema Jogad et al., "CNTFET-Based Active Grounded Inductor Using Positive and Negative Current Conveyors and Applications," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 34, no. 5, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[12] Sumio Iijima, "Helical Microtubules of Graphitic Carbon," *Nature*, vol. 354, no. 6348, pp. 56-58, 1991. [CrossRef] [Google Scholar] [Publisher Link]

[13] Shweta Kumari, and Maneesha Gupta, "Design and Analysis of Tunable Voltage Differencing Inverting Buffered Amplifier (VDIBA) with Enhanced Performance and Its Application in Filters," *Wireless Personal Communications*, vol. 100, no. 3, pp. 877-894, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[14] Niharika Narang, Bhawna Aggarwal, and Maneesha Gupta, "DTMOS and FD-FVF based Low Voltage High Performance Voltage Differencing Transconductance Amplifier (VDTA) and its Application in MISO Filter," *Microelectronics Journal*, vol. 63, pp. 66-74, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[15] Priyanka Gupta et al., "Realization of a New CMOS Transconductance Boosted Voltage Differencing Inverting Buffered Amplifier (TB-VDIBA) using Series Parallel Current Mirror (SPCM)," *Journal of Circuits, Systems and Computers*, vol. 34, no. 10, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[16] Ale Imran, S.D. Pable, and Mohd. Hasan, "A Comparative Study of CMOS & CNFET Based Current Conveyor at 32nm Technology Node," *2010 International Conference on Computer and Communication Technology (ICCCT)*, Allahabad, India, pp. 276-281, 2010. [CrossRef] [Google Scholar] [Publisher Link]

[17] Şeyda Sunca Ulusoy, and Mustafa Alçı, "A Low Voltage High Performance CNTFET-based VDIBA and Universal Filter Application," *Analog Integrated Circuits and Signal Processing*, vol. 120, no. 1, pp. 1-8, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[18] Shweta Kumari, and Maneesha Gupta, "New CMOS Realization of High-Performance Voltage Differencing Inverting Buffered Amplifier and its Filter Application," *Analog Integrated Circuits and Signal Processing*, vol. 92, no. 1, pp. 167-178, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[19] Maneesha Gupta, Richa Srivastava, and Urvashi Singh, "Low-Voltage Low-Power FGMOS based VDIBA and its Application as Universal Filter," *Microelectronics Journal*, vol. 46, no. 2, pp. 125-134, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[20] Okkes Gokalp Sokmen et al., "A Novel Design of Low-Voltage VDIBA and Filter Application," *Electronics and Electrical Engineering*, vol. 22, no. 6, pp. 1-6, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[21] Richa Srivastava et al., "Low-Voltage Bulk-Driven Self Cascode Transistor based Voltage Differencing Inverting Buffered Amplifier and its Application as Universal Filter," *Microelectronics Journal*, vol. 102, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[22] Priyanka Gupta, Saji M. Antony, and Diksha Jain, "A New CMOS Realization of High Performance Adaptive Biased Voltage Differencing Inverting Buffered Amplifier," *Journal of Circuits, Systems and Computers*, vol. 34, no. 12, 2025. [CrossRef] [Google Scholar] [Publisher Link]