Design and Implementation of 64-bit Multiplication using CLAA & CLSA

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ABSTRACT: *In this paper deals with the comparison of the VLSI style of the carry look-ahead adder (CLAA) based mostly} 32-bit signed and unsigned whole number number and also the VLSI style of the carry choose adder (CSLA) based 32-bit signed and unsigned whole number number. Multiplication could be a elementary operation in most signal process algorithms. Multipliers have giant space, long latency and consume hefty power. so low-power number style has been a vital half in low- power VLSI system style. A system's performance is mostly determined by the performance of the number as a result of the number is mostly the slowest part within the system. moreover, it\'s usually the foremost space intense. Hence, optimizing the speed and space of the number could be a major style issue. Carry choose adder is one among the quickest adders utilized in several applications to perform quick arithmetic functions. This work evaluates the performance of the planned styles in terms of delay, speed(frequency)and memory. The CLAA based mostly} number uses the delay time of 99ns for activity multiplication operation wherever as in CSLA based number conjointly uses nearly identical delay time for multiplication operation. however the realm required for CLAA number is reduced to thirty one procurable the CSLA primarily based number to completethe multiplication operation*

.***Keywords*** *–CLAA, CSLA, Delay, Area, Array Multiplier*

I. INTRODUCTION

Speed of operation is that the most significant constraint to be thought of whereas planning multipliers. thanks to device movableness shrinking of device ought to be high and power consumption ought to be low. High-speed knowledge path logic systems area unit one among the foremost substantial areas of analysis in VLSI system style. In digital adders, the speed of addition is proscribed by the time needed to propagate a carry through the adder. The total for every bit position in an elementary adder is generated consecutive solely when the previous bit position has been summed and a carry propagated into following position. Ripple carry adders exhibits the foremost compact style however the slowest in speed. Whereas carry look ahead is that the quickest one however consumes a lot of space. Carry choose adders act as a compromise between the 2 adders.

A new idea of hybrid adders is bestowed to hurry up addition method. The CSLA isn\'t space economical as a result of it uses multiple pairs of Ripple Carry Adders (RCA) to get partial total and carry by considering carry input Cin = zeroand Cin = 0, then the ultimate total and carry area unit hand-picked by the multiplexers (mux).In this project we tend to area unit about to compare the performance of various adders enforced to the multipliers supported space and time required for calculation. On comparison with the carry look-ahead adder (CLAA) based mostly} number the realm of calculation of the carry choose adder (CSLA) based number is smaller and higher with nearly same delay time. Here we tend to area unit addressing the comparison within the bit vary of n*n (32*32) as input and 2n(64) bit output.

Multiplication could be a {mathematical operation|mathematicalmethod|operation|calculation|computation|computing} that at its simplest is associate abbreviated process of adding associate variety number} a such number of times. Multiplication is that the elementary mathematical process vital in many processors and digital signal process systems. Multiplication of 2 k bit variety required multi quantity addition method that may be complete in k cycles of shifting and addition with hardware, code or software package. Multiplication primarily based operations like multiply and accumulate (MAC) and scalar product area unit among a number of the oft used intensive arithmetic functions presently enforced in several digital signal process (DSP) applications like convolution, quick fourier transform(FFT),filtering and in microprocessors in its arithmetic and logic unit. moveable multimedia system and digital signal process (DSP) systems, which generally need low power consumption, short style cycle, and versatile process ability, became progressively standard over the past few years. As several multimedia system and DSP applications area unit extremely multiplication intensive in order that the performance and power consumption of those systems area unit dominated by multipliers. sadly, moveable devices principally operate with complete batteries, however multipliers consumes great amount of power. Digital signal process systems want multiplication algorithmic programs to implement DSP algorithms like filtering wherever the multiplication algorithm is directly among the essential path. in conjunction with signal process applications, multimedia, and 3D graphics, performance, in most cases, powerfully depends on the effectiveness of the hardware used for computing multiplications, since multiplication is, besides addition, massively utilized in these environments. Consequently, it's greatly imperative to develop power-efficient multipliers to compose a superior and low-power moveable multimedia system and DSP system. because the scale of integration keeps growing, a lot of and a lot of subtle signal process systems area unit being enforced on a VLSI chip. These signal process applications not solely demand nice computation capability however conjointly consume hefty quantity of energy. whereas speed and space stay to be the 2 major style tools. the upper speed results to enlarged power consumption, thus, low power2 architectures are the selection of the long run. the requirement for low-power VLSI system arises from 2 main forces.

First, with the steady growth of in operation frequency and process capability per chip, giant currents ought to be delivered and also the heat thanks to giant power consumption should be removed by correct cooling techniques. Second, battery life in moveable electronic devices is proscribed. Low power style directly ends up in prolonged operation time in these moveable devices. This has given thanks to the expansion of recent circuit algorithms, with the set up of reducing the ability consumption of multiplication algorithms with having high-speed structures and applicable Performance. The number is fairly giant block of a computer system. the dimensions of number is directly proportional to the sq. of its resolution i.e. size of number..

1.1 CLASSIFICATION OF MULTIPLIER

There are two kinds of multiplier as shown in fig. 1.1

a) Serial multiplication algorithms
b) Parallel multiplication algorithms

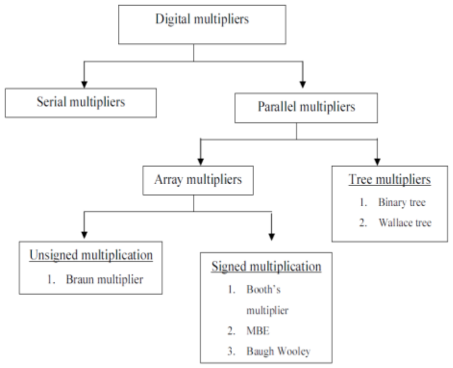


Fig 1.1 Classification of multipliers

1.2 MULTIPLICATION OF SIGNED AND UNSIGNED NUMBER

Multiplication of unsigned numbers will be done by straightforward multiplication algorithmic program. If the sign of the number and number area unit completely different, sign of the merchandise is negative. The magnitude is increased within the same approach because the unsigned numbers. If each area unit negative, the sign of the result\'s positive. The sign needs area unit met by the overall rule: the sign of the merchandise id exclusive or of the sign of the amount.multiplied in the same way as the unsigned numbers. If both are negative, the sign of the result is positive. The sign requirements are met by the general rule: the sign of the product id exclusive or of the sign of the number.

ADDERS:

Addition is that the commonest and infrequently used mathematical process on chip, digital signal processor, particularly digital computers. Also, it is a building block for synthesis all different arithmetic operations. Therefore, relating to the economical implementation of associate arithmetic unit, the binary adder structures become a awfully essential hardware unit.

The primary category consists of the terribly slow ripple-carry adder with the tiniest space. within the second category, the carry-skip, carry-select adders with multiple levels have little space needs and shortened computation times. From the third category, the carry-look ahead adder and from the fourth category, the parallel prefix adder represents the quickest addition schemes with the most important space complexities.

RIPPLE CARRY ADDERS (RCA)

The well-known adder design, ripple carry adder consists of cascaded full adders for n-bit adder, as shown in figure four.1.It is created by cascading full adder blocks nonparallel. The perform of 1 stage is fed on to the carry-in of following stage. For associate n-bit parallel adder it needs n full adders.

1.3 CARRY SELECT ADDERS (CSLA)

The carry choose adder comes within the class of conditional total adder. Conditional total adder works on some condition. total and carry area unit calculated by forward input carry as one and zero previous the input carry comes. once actual carry input arrives, the particular calculated values of total and carry area unit hand-picked employing a electronic device. the standard carry choose adder consists of k/2 bit adder for the lower 1/2 the bits i.e. least important bits and for the higher 0.5 i.e. most important bits (MSB's) 2 k/ bit adders. In MSB adder's one adder assumes carry input in concert for activity addition and another assumes carry input as zero.

The perform calculated from the last stage i.e. least important bit stage is employed to pick the particular calculated values of output carry and total. the choice is completed by employing a electronic device. this method of dividing adder in 2 stages will increase the realm utilization however addition operation fastens. it\'s composed of 2 four-bit ripple carry adders per section. each total and carry bits area unit calculated for the 2 alternatives of the input carry, '0' and '1'.The perform of every section determines the carry in of following section, that then selects the suitable ripple carry adder. The terribly initial section incorporates a carry in of zero. Time delay: time to reason initial section + time to pick total from later sections.

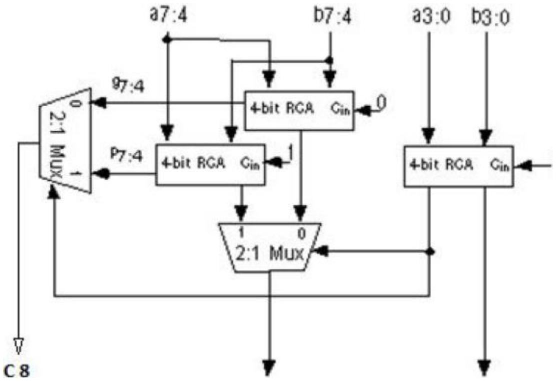


Fig: Carry Select Adder

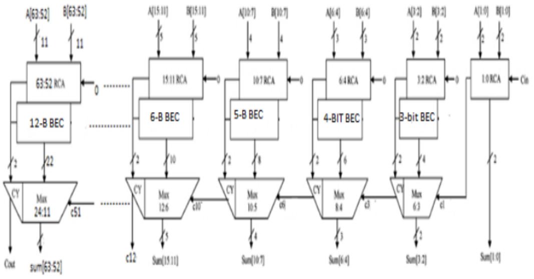


Fig: Block Diagram of Regular 64 bit Carry Select Adder

1.4 CARRY LOOK AHEAD ADDER

The carry look ahead adder (CLA) solves the carry delay downside by hard the carry signals before, supported the input signals. it's supported the actual fact that a carry signal are generated in 2 cases:

1) once each bismuths ai and bi ar one,
2) once one among the 2 bits is one and also the carry-in is.1Thus we will write The on top of 2 equations may be written in terms of 2 new signals

Pi and Gi , that ar shown in Figure.

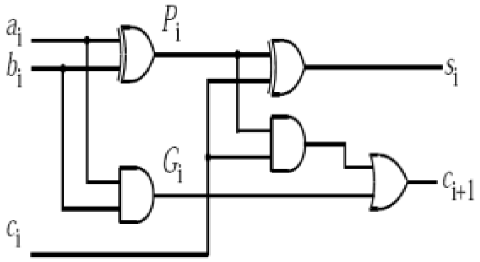


Fig: Full Adder Stage at Stage I with Pi and Gi

Let Gi is the carry generate function and Pi be the carry propagate function, Then we can rewrite the carry

function as follows:

Gi = Ai· Bi.

Pi = (Ai xor Bi).

Si = Pi xorCi.

Ci+l= Gi + Pi.Ci.

2.0 MULTIPLICATIONALGORITHM

There are 3 representations we have a tendency to consider: Signed Magnitude: merely multiply the magnitudes as unsigned integers. cypher the sign via XORing the signs of the numbers. One’s complement: 1st complement the negative operands. Multiply and verify the sign. Complement the result if negative.

Two's complement: there's an excessive amount of overhead in computing enhances. would like associate rule to multiply signed numbers directly. once the number is negative and also the multiplier factor is positive we have a tendency to might merely use the unsigned right shift rule. we'd got to perform signed additions and punctiliously sign extend partial merchandise.

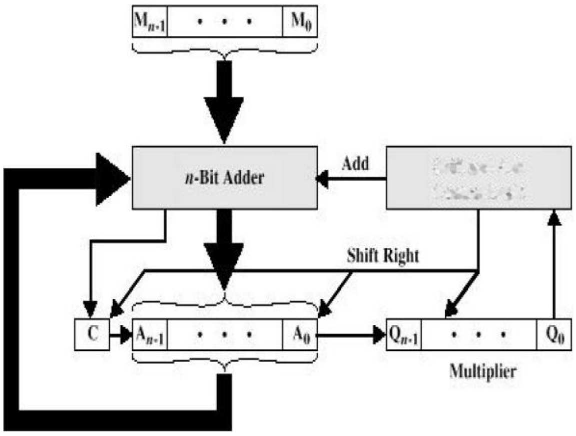


Fig:Multiplier of two n-bit values.

3.0 SIMULATION RESULTS:

The HDL simulation of the 2 multipliers is given during this section. In this, waveforms, temporal arrangement diagrams, the look outline and also the power analysis for each the CLAA and CSLA primarily based multipliers ar shown within the figures. The HDL code for each multipliers, victimisation CLAA and CSLA, ar generated. The HDL model has been developed victimisation Modelsim6.4b.The multipliers use 2 32-bit values.

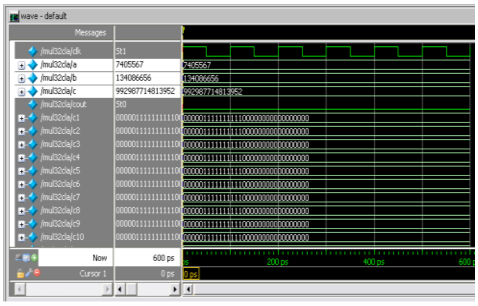

```
wave - default
Messages
/mul32cla/clk     St1
/mul32cla/a       7405567              7405567
/mul32cla/b       134086656            134086656
/mul32cla/c       992987714813952      992987714813952
/mul32cla/cout    St0
/mul32cla/c1      000001111111111100   000001111111111000000000000000000
/mul32cla/c2      000001111111111100   000001111111111000000000000000000
/mul32cla/c3      000001111111111100   000001111111111000000000000000000
/mul32cla/c4      000001111111111100   000001111111111000000000000000000
/mul32cla/c5      000001111111111100   000001111111111000000000000000000
/mul32cla/c6      000001111111111100   000001111111111000000000000000000
/mul32cla/c7      000001111111111100   000001111111111000000000000000000
/mul32cla/c8      000001111111111100   000001111111111000000000000000000
/mul32cla/c9      000001111111111100   000001111111111000000000000000000
/mul32cla/c10     000001111111111100   000001111111111000000000000000000
Now               600 ps               ps     200 ps     400 ps     600 p
Cursor 1          0 ps                 0 ps
```

Fig: 64 bit multiplier using CLA

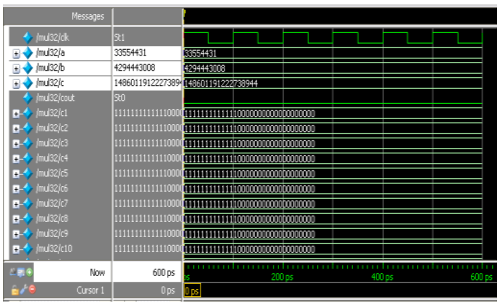
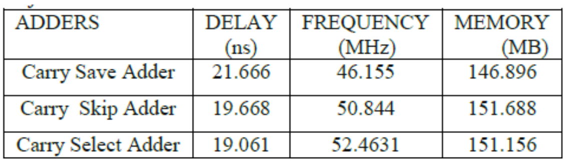

```
Messages
/mul32/clk     St1
/mul32/a       33554431             33554431
/mul32/b       4294443008           4294443008
/mul32/c       148601191222738944   148601191222738944
/mul32/cout    St0
/mul32/c1      1111111111111110000  1111111111111000000000000000000000
/mul32/c2      1111111111111110000  1111111111111000000000000000000000
/mul32/c3      1111111111111110000  1111111111111000000000000000000000
/mul32/c4      1111111111111110000  1111111111111000000000000000000000
/mul32/c5      1111111111111110000  1111111111111000000000000000000000
/mul32/c6      1111111111111110000  1111111111111000000000000000000000
/mul32/c7      1111111111111110000  1111111111111000000000000000000000
/mul32/c8      1111111111111110000  1111111111111000000000000000000000
/mul32/c9      1111111111111110000  1111111111111000000000000000000000
/mul32/c10     1111111111111110000  1111111111111000000000000000000000
Now            600 ps               ps     200 ps     400 ps     600 ps
Cursor 1       0 ps                 0 ps
```

Fig:64 bit multiplier using CSLA

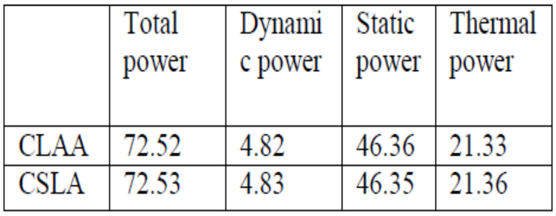
Performance Analysis of Adders

In this analysis table shown in figure, the delay time is sort of same, space|the world|the realm} and also the area delay product of CSLA {based|based mostly|primarily primarily based} multiplier factor is reduced to 06 that when compared to CLAA based multiplier factor.



ADDERS	DELAY (ns)	FREQUENCY (MHz)	MEMORY (MB)
Carry Save Adder	21.666	46.155	146.896
Carry Skip Adder	19.668	50.844	151.688
Carry Select Adder	19.061	52.4631	151.156

The power performance analysis for the CLAA and CSLA primarily based multipliers ar drawn within the sort of the diagram shown in figure and also the table on top of. Here the ability dissipation ar some same for each CLAA &amp; CSLA.



	Total power	Dynamic power	Static power	Thermal power
CLAA	72.52	4.82	46.36	21.33
CSLA	72.53	4.83	46.35	21.36

4.0 CONCLUSION

Performance analysis of assorted adders is analyzed in terms of delay, frequency and memory from these carry choose adder is best parameter values than alternative adders. and also the regular carry choose is any changed for speed and space potency. A style and implementation of a HDL-based 32-bit Signed and unsigned multiplier factor with CLAA and CSLA was given. the ability analysis some same for each CLAA &amp; CSLA. therefore a 06 the world delay product reduction is feasible with the employment of the CSLA {based|based mostly|primarily primarily based} thirty two bit signed Array multiplier factor than CLAA based thirty two bit signed Array multiplier factor.

5.0 FUTURE WORK

This thirty two bit multiplier factor may be any extended to sixty four bit multiplier factor and 128 bit multiplier factor victimisation the projected methodology for multiplication operation may be done as future work.

REFERENCES

[1] Ramkumar, B. and Harish M Kittur,(2012) “Low Power and Area Efficient Carry Select Adder”,IEEE Transactions on Very Large Scale Integration (VLSI) Systems, pp.1-5.

[2]V.Vijayalakshmil, R.Seshadd, Dr.S.Ramakrishnan, (2013) Design and Implementation of 32 BitUnsigned Multiplier Using CLAA and CSLA 978-1-4673-5301-IEEE.

[3] P. Asadi and K. Navi, "A novel highs-speed 54-54 bit multiplier",Am. J Applied Sci., vol. 4 (9), pp. 666-672. 2007.

[4] W. Stallings, Computer Organization and Architecture Designing forPeljormance, 71h ed., Prentice Hall, Pearson Education International,USA, 2006, ISBN: 0-13-185644-8.

[5] 1. F. Wakerly, Digital Design-Principles and Practices, 4th ed.,Pearson Prentice Hall, USA, 2006. ISBN: 0131733494.