

Review: Design and Implementation of Reed Solomon Encoder and Decoder

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Abstract

This paper presents a literature survey related to Reed Solomon encoder and decoder. In this project fast encoding and decoding algorithm using Reed Solomon codes is developed for the processing of self correcting logic in erroneous condition which is widely used in numerous applications. The main goal of this work is to make the data or information error free that is to be transmitted and also help the reader to understand the theory of RS codes and its encoding and decoding in order to make the errors detectable and correctable.

Keywords - FPGA, Key Equation Solver (KES), Reed Solomon (RS), Syndrome Calculation (SC) and VHDL.

I. INTRODUCTION

In practical communication system, data or information gets corrupted by noise during transmission. Today there is an increasing demand for development of reliable communication and wireless systems. Hence it is important to detect and correct errors in the information received over communication channels. Therefore error control coding is important in communication system design for various applications. The suitable ECC can be chosen depending on the code that is capable of detecting and correcting maximum number of errors, error type and the performance of encoding and decoding units in terms of speed. The RS codes were introduced firstly in a paper named “Polynomial codes over certain finite fields” in 1960 for burst error correction [11].

II. REED SOLOMON CODES

BCH and Reed-Solomon codes are the most widely used error correcting codes (ECC). The RS codes are more particularly used in communication and storage system because of its capability of correcting both burst and random errors. These are the non-binary systematic cyclic linear block codes [6]. These codes operate on symbols that consist of several bits. The most commonly used symbol size for non-binary codes is 8-bits, or a byte [8]. The information is operated by the RS codes by dividing the message stream into blocks of data and redundancy is added per block depending only on the current inputs. The codeword is formed by affixing the parity symbols to the data symbols which is

represented in Fig. 1. The symbols in RS coding are elements of a finite field or Galois Field (GF). The encoding and decoding of Reed Solomon codes is done by using GF arithmetic [6]. RS codes have the highest code rate of all binary codes. In this study, a Reed Solomon (255, 239) error correction code is modelled to detect and correct 8 symbol-errors in the transmitted data. The design is implemented on Spartan 6 FPGA device.

III. REPRESENTATION OF RS CODES

The RS codes are represented as RS (n, k) with m-bit symbols, where n is the block length and k is the no. of original message symbols. Number of parity digits can be calculated by subtracting original message symbols from block length which is shown as,

$$n - k = 2t \quad (1)$$

The relationship between the symbol size, m, and the size of the codeword n, is given by,

$$n = 2^m - 1 \quad (2)$$

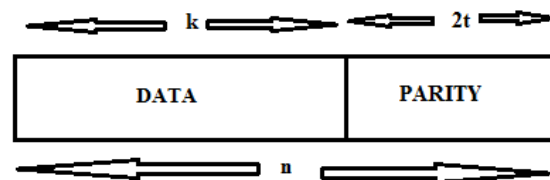


Fig 1: The Structure of RS Codeword

IV. LITERATURE REVIEW

SR. NO.	NAME OF AUTHOR	PAPER TITLE	PUBLICATION	APPROACH AND CONCEPT ABOUT WORK	ADVANTAGES
1.	G.C.Cardarilli, S. Pontarelli, M. Re, and A. Salsano	Concurrent Error Detection in Reed–Solomon Encoders and Decoders	IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 15, No. 7, July 2007	In this paper self checking RS encoder and decoder architecture using error correction codes are presented.	It also removes the error/faults present in RS encoder and decoder which compromise the reliability of whole system.
2.	Aqib Al Azad and Md Imam Shahed	A Compact and Fast FPGA Based Implementation of Encoding and Decoding Algorithm Using Reed Solomon Codes	International Journal of Future Computer and Communication, Vol. 3, No. 1, February 2014.	Here a compact and fast FPGA based implementation technique for encoding and decoding of RS codes is used for Error detection and correction.	The design can also be synthesized to other FPGA architectures.
3.	Rajeev Kumar Patial Priyanka Dayal	FPGA Implementation of Reed-Solomon Encoder and Decoder for Wireless Network 802.16	International Journal of Computer Applications (0975 – 8887) Volume 68–No.16, April 2013.	Here pipelining is introduced in RS decoder to improve the performance. The performance of RS encoder RS (255,239) for IEEE 802.16 is shown and RS decoder is checked for both RS (255,243) and RS (255,239).	In this paper less number of LUT’s are used in RS (255,243) as comparison to RS (255,239).
4.	G. C. Cardarilli, S. Pontarelli, M. Re, and A. Salsano	Analysis of Errors and Erasures in Parity Sharing RS Codecs	IEEE Transactions on Computers, Vol. 56, No. 12, December 2007.	This paper analyses performance of PS codes and extends the results to memory systems in which permanent faults and transient faults can be represented as erasures and random errors.	A designer can choose between different PS code implementation in order to meet requirements such as hardware complexity, BER, speed and throughput.

5.	Abhinav Agarwal, Man Cheuk Ng, and Arvind	A Comparative Evaluation of High-Level Hardware Synthesis Using Reed–Solomon Decoder	IEEE Embedded Systems Letters, Vol. 2, No. 3, September 2010.	In this paper information about what type of hardware structures should be generated to achieve specific performance targets using RS decoder is presented.	Here a high level HDL i.e. Bluespec System Verilog is used which makes it easy to express the necessary architectural elements to achieve the desired performance.
6.	Diplaxmi Chaudhari, Mayura Bhujade, Pranali Dhumal	VHDL Design and FPGA Implementation of Reed Solomon Encoder and Decoder for RS (7, 3)	International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 3, March 2014 563.	In this paper, Reed-Solomon (RS) encoder and decoder for RS (7,3) codec and their hardware implementation in Actel ProASIC3 (Field Programmable Gate Array (FPGA) kit is analyzed.	Here Berlekamp Massey algorithm is used for solving key equations as it has least hardware complexity as compared to Euclidean algorithm.

V. RS ENCODER

RS codes are encoded by simply adding the parity symbols at the end of k-symbols message block [8] which is together called as codeword and is shown in figure 1 [6]. At the encoder side, the information is shifted into the left most bits by multiplying by X^{2t} , leaving a codeword of the form,

$$C(X) = X^{2t} m(x) + p(x) \tag{3}$$

Where $C(x)$ is the codeword polynomial, $m(X)$ is message polynomial and $p(x)$ is the redundant polynomial [8]. The parity symbol is the remainder which is obtained by dividing message block with the generator polynomial and it is represented as,

$$p(X) = (X^{2t} m(X)) \text{ mod } g(X) \tag{4}$$

So, generator polynomial is responsible for generating RS codeword, which has a unique property that all valid codewords are exactly divisible by the generator polynomial. The generator polynomial is shown as,

VI. RS DECODER

At the receiver side the received codeword is entered to RS decoder which we have to decode. The decoder first tries to check if this codeword is a valid codeword or not. If it not the codeword which was sent by the encoder it means that there are some errors occurred during

$$G(X) = (X+\alpha)(X+\alpha^2)(X+\alpha^3) \dots (X+\alpha^{2t})$$

$$= g_0 + g_1X + g_2X^2 + \dots + g_{2t-1}X^{2t-1} + X^{2t} \tag{5}$$

where α is a primitive element in $GF(2^m)$, and $g_0, g_1, g_2, \dots, g_{2t-1}$ are the coefficients from $GF(2^m)$ [8].

The architecture of RS encoder is shown in figure 2 below.

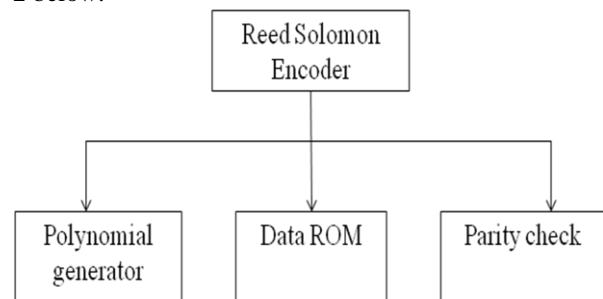


Fig 2: Block Diagram of RS Encoder [6]

transmission. This portion of the decoder processing is called error detection. If the errors are detected then the decoder tries to correct these errors using error correction part [8].

Fig.3 shows the architecture of Reed Solomon decoder which is made up of two main parts:

1. Error detection part which is also called as “Syndrome Computation” block.
2. Error correction part, this part consists of three blocks:
 - First is the decoding algorithm which is used to find the coefficients of error-location polynomial $\sigma(x)$ and error-evaluator polynomial $W(x)$ and it is sometimes called as “Key equation solver”.
 - Second is the Chien search block which is used to find the roots of $\sigma(x)$ i.e. the error location polynomial which presents the inverse of the error locations.
 - And the third block is the Forney algorithm block which is used to find the values of the errors. Hence we can correct the received vector from the values and locations of the errors which we get from the above two blocks by XORing with the error vector.

The description of each block is given below:

1. Syndrome Computation block:

Here the syndrome values are calculated. The syndrome is a remainder obtained by dividing the received codeword by the generator polynomial.

$$\frac{R(x)}{g(x)} = P(x) + \frac{S(x)}{g(x)} \quad (6)$$

2. KES Block:

The Key equation solver (KES) block provides two polynomial - error locator polynomial and error magnitude polynomial which calculates the error location and magnitude [6].

3. CSEE Block: Chien Search and Error Evaluator block identifies the error location while computing its error magnitude [6].

4. FIFO register:

The received word symbols are stored in FIFO register. Since the error vector is produced in the reverse order of the received codeword, the FIFO register is applied to match the order of bytes in error vector and received codeword [6].

5. Controller:

The controller is used to control and synchronize all four modules -SC, KES, CSEE and FIFO Registers.

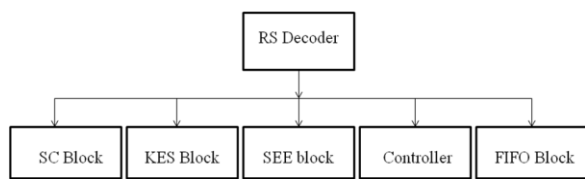


Fig 3: Block Diagram of RS Decoder [6]

VII.CONCLUSION

The design of encoder and decoder is described in VHDL and will be implemented on Spartan 6 FPGA device using Xilinx software. The RS Decoder corrects a symbol, by replacing the incorrect symbol with the correct one, whether the error was occurred in one bit or all of the bits. Thus, if a symbol is wrong, it might as well be wrong in all of its bit positions and hence because of this reason RS codes have tremendous burst-noise advantages over binary codes [15]. For reliable communication in the presence of noisy channel efficient error detection and correction techniques are shown in this paper. RS codes can be extended or shortened because they are based on the finite fields. Reed Solomon codes provide a wide range of code values that can be chosen to optimize the performance. RS codes have wide application and are used in Wireless Communication such as mobile phones, microwave links, in Deep Space and Satellite Communications Networks, mass storage devices such as hard disk drives, DVD, barcodes and Broadband Modems (ADSL,VDSL, SDSL, HDSL etc). Now-a-days technologies are getting compact and faster, so we hope our work will add new dimension in that trend.

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