12 bit Time Interleaved ADC in 65nm Technology

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Abstract

This paper presents an architecture of a 4-Time Interleaved ADC (TIADC) having sampling rate of 2GSps and resolution of 12-bit. The input signal is sampled at 2GHz with aid of a 4-phase clock generator providing a 90° phase shift. The design is operated at 1.2-V power supply with digital control running at frequency of 1.953MHz. The designed TIADC has a 2GS/s sampling rate, ENOB of 11.21b, SNDR of 69.249 dB, SFDR of 79.09 dB and consumes total power of 40.32 mW. The TIADC architecture is implemented using UMC 65nm CMOS technology.

Keywords— *Analog to digital converter (ADC), Time interleaving, sampling rate, resolution, CMOS, ENOB, SNDR, SFDR*

I. INTRODUCTION

The performance of modern digital communication systems is highly dependent on the design of analog-to-digital converters (ADCs) [1], and in order to provide more flexibility and precision for the emerging communication technologies, high-performance ADCs with low power consumption are essential. The sampling rate and conversion time are two key ADC performance metrics. For DSP applications, ADCs form a major bottleneck since it is difficult to simultaneously achieve high sampling rate and high resolution. Among various existing ADC architectures, the Time-Interleaved Analog-to-Digital converter (TI-ADC) has emerged a popular choice for achieving high sampling rates and resolutions. A TI-ADC operates on principle of interleaving the outputs of ***M***-identical ADCs with set resolution as that of an individual ADC channel but with M times higher bandwidth. The equivalent time-interleaved ADC will always be less energy-efficient than its constituent interleaved channels because of the overhead associated with time-interleaving. The energy per conversion of an ADC, defined as the ratio of the power and the sampling frequency, typically increases with the sampling frequency as shown in Fig. 1.

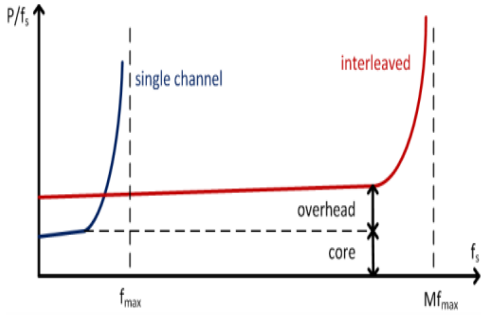


Fig. 1. Energy per conversion Vs sampling frequency for a single-channel and a Time interleaved SAR ADC

This paper presents a number of new insights into the operation and performance of interleaved ADCs. Specifically, the authors study how interleaving is beneficial, [2] provides details about the advantages of TI-ADC and the affects of channel mismatches on the performance of TI ADC. [3] & [4] discuss the techniques used to mitigate the effects of these errors. [5] presents a 64-time interleaved 10bit SAR ADC suitable for high data rate optical communication.

The proposed work with 4-time interleaved ADC achieves higher data rates with less complexity in clock generation therefore avoiding the need to consider variations in clock. [6] presents a 4-time interleaved ADC with 6-bit resolution having sampling rate of 2.6 GS/s, the design offers low power consumption but complexity is increasing by having ADC slices arranged in a pipelined binary search using dynamic non-linear amplifier. This design provides only 6-bit resolution but requires pipeline stage implementation for every bit that increases complexity.

The paper is organised where in section II describes the advantages of interleaving, particularly the improvement of the Figure of Merit (FOM) and the reduction of metastability error rate. Section III presents design of digital and analog blocks. Section IV shows some simulation results. Finally, the authors summarize and conclude the paper in section V.

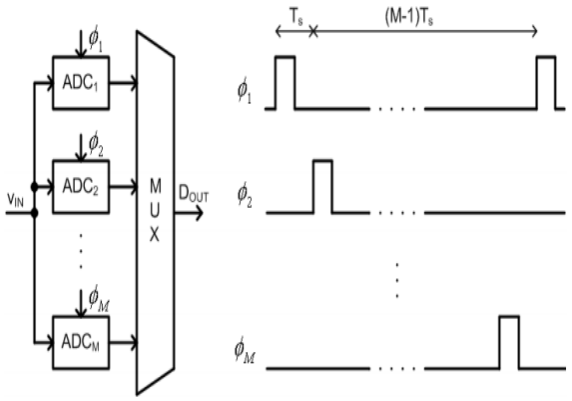


Fig. 2. M-Time Interleaving Block Diagram and its Clock Phases

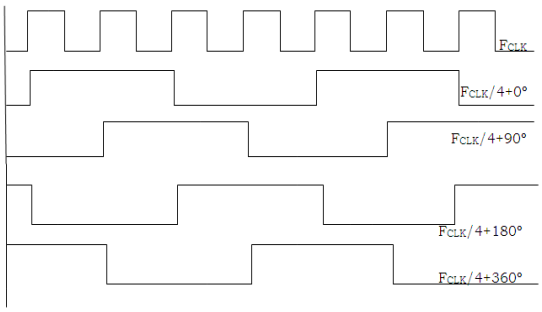


Fig.3 Clock phases 4-phase Clock Generator

II. ADVANTAGES OF INTERLEAVING

In order to allow greater acquisition and conversion times, identical ADCs, each having a front-end sampler can be interleaved in the time domain. This arrangement requires clock phases that uniformly span 360 Fig. 3. The digital outputs can be multiplexed to reconstruct the data, but in many applications the slower outputs are preferred as they ease the subsequent processing. The maximum analog input frequency is denoted by f_{in} , the period of each of the clocks in Figure 1 by $T_{ck}=1/f_{ck}$, and the overall sampling rate by $f_s=Nf_{ck}$. We assume that the sampling capacitor in each channel is determined by kT/C noise and consider resolutions around 10 bits and sampling rates around 1 GHz. Most of the concepts are presented for N=2 but can be generalized for higher values of N as well.

A. Maximum Speed

The extent to which interleaving improves the conversion rate depends on the relative speeds of the sampler and the quantizer in each channel. In a typical case, the quantizer's long conversion time calls for interleaving, but the maximum number of channels is ultimately limited by the sampler's performance. To formulate this bound, first suppose a single Nyquist-rate channel is designed for minimum acquisition time through the use of known techniques such as switch bootstrapping. If the ADC allots $T_{ck}=1/(2f_s)=1/(4f_{in})$ seconds to acquisition and requires K time constants, K τ_{acq} for the resolution of interest, then $T_{ck}/2= K\tau_{acq}$ and hence

$$f_{in} \leq \frac{1}{4K\tau_{acq}} \qquad (1)$$

In addition, the small-signal bandwidth of the sampler (in the acquisition mode) must exceed so as to avoid significant attenuation

$$f_{in} \leq \frac{1}{2\pi\tau_{acq}} \qquad (2)$$

For resolutions higher than a few bits, (1) guarantees (2). However, as the number of interleaved channels and hence the maximum input frequency increase, (2) eventually dominates. For channels, we express (1) as $N/(4 Kr_{acq})$ and equate the result to (2), obtaining

$$N \leq \frac{2K}{\pi} \qquad (3)$$

Thus, if the samplers are the speed bottleneck, then interleaving beyond $N= 2K/\pi$ provides little improvement. In general, for an M-bit system to settle to 0.5 LSB, we have K= (M+1)ln2 and hence

$$N< (M+1)\ln 2$$
$$< 0.44(M+1)$$

For example, a 10-bit ADC designed for maximum speed negligibly benefits from interleaving if ***N≥ 4***.

B. Power-Speed Tradeoffs

An important attribute of time interleaving is the flexibility that it affords in the power-speed tradeoff. Recent work on successive-approximation (SAR) ADCs has extensively exploited this attribute to achieve low figures of merit[7],[8]. We define FOM as the power consumption divided by the product of 2^{ENOB} and $\min(f_s, 2f_{in})$, where ENOB denotes the effective number of bits at an input frequency of f_{in}.

Interleaving improves the FOM because, as the conversion speed of a single channel approaches the limits of the technology, the power-speed tradeoff becomes nonlinear, demanding a disproportionately higher power for a desired increase in speed. For example, op amps and comparators eventually reach diminishing returns in their speed as their power consumption is raised. From another perspective, each

ADC architecture incurs a certain "timing overhead" that does not easily scale with power.

Due to the relatively unsalable timing overheads in each architecture, the figure of merit of ADCs tends to degrade at higher speeds. For example, the FOM rises from 10 fJ per conversion step for the 8-MHz 12-bit ADC in [9] to 500 fJ per conversion step for the 3-GHz 12-bit ADC in [10]. This trend can be ameliorated through the use of time interleaving. In order to quantify this proposition, we assume a simple case where the critical times in an ADC can be lumped into an unscalable overhead T_{OV}, and a linearly power-scalable remainder, $T_{CK} - T_{OV}$. For a single channel, $T_{CK} = T_S$ and $T_S - T_{OV} \propto 1/P_1$ where P_1 denotes the power drawn by the scalable functions in the ADC. The single channel thus demands a power shown in (4) (plus the power consumed by the unscalable functions) to reach a sampling rate of $1/T_S$,

$$P_1 = \frac{\alpha}{T_S - T_{OV}} \qquad (4)$$

where α is a proportionality factor. For N interleaved channels, on the other hand, the scalable remainder is equal to $T_{CK} - T_{OV} = NT_S - T_{OV}$, yielding an overall power consumption of

$$P_N = \frac{N\alpha}{NT_{S-T_{OV}}} \qquad (5)$$

for the scalable functions. It follows that:

$$\frac{P_N}{P_1} = \frac{N(T_S - T_{OV})}{NT_S - T_{OV}} \qquad (6)$$

This equation (6) formulates the power advantage of interleaving as N increases.

C. Clock Network Power Consumption

Interleaving can potentially lower the power consumption of the clock network. The system of Figure 1 requires M= 4 clock phases that must be distributed across the ADC chip. Let us first consider a single-channel pipelined ADC whose amplifiers, comparators, and capacitors are designed so as to meet certain thermal and kT/C noise requirements. Such a design presents to the clock a total MOS switch capacitance of C_{MOS} and a total interconnect capacitance of C_{int} , drawing a power of at least $f_S(C_{MOS} + C_{int})V^2_{DD}$ in the clock path.

Now, we interleave M channels, each running at $f_{CK} = f_S / M$, and make the following observations: 1) determined by kT/C noise, the capacitors in each channel cannot be reduced; 2) the widths of the clocked MOSFETs can be scaled down by a factor of M if we allow all settling times to increase by the same factor and 3) the total interconnect length per channel is relatively constant because, while most of the MOSFETs are scaled down, the clock phases must still travel from a central point on the chip to all M channels. Thus, the clock power dissipation is now equal to, $(f_S / M)M(C_{MOS} / M + C_{int})V_{DD}^2 = f_S(C_{MOS} / M + C_{int})V_{DD}^2$, somewhat lower than that of the single-channel ADC, interleaving can indeed reduce the clock dissipation component.

D. Metastability

Time interleaving can substantially reduce the probability of metastable states in ADCs. This attribute proves particularly useful in multistep (e.g., pipelined or SAR) architectures as they do not permit comparator pipelining (unless the conversion time is increased). Suppose a single-channel ADC employs a comparator design having a regeneration time constant of τ_{reg} . The probability of a metastable state is given by $\alpha \exp(- T_1/ \tau_{reg})$ where α is a proportionality factor and T_1 is the nominal time allocated for the comparator decision. Thus, of a large number of conversions L, we expect that $\alpha \exp(- T_1/ \tau_{reg})$ are erroneous. Now, we interleave N such ADCs, assuming that the allowable comparator decision time can be increased to NT_1 . Each channel therefore exhibits an error rate equal to $\alpha \exp(- (NT_1)/ \tau_{reg})$, producing $\alpha \exp(- (NT_1/ \tau_{reg})L$ erroneous outputs for every conversions. Upon multiplexing the outputs, we obtain a total of NL conversions, of which $\alpha N \exp(- (NT_1)/ \tau_{reg})L$ are incorrect. That is, the probability of metastable states in the interleaved system is given by equation (7)

$$P_{met,N} = \alpha e^{\frac{-NT_1}{\tau_{acq}}} \qquad (7)$$

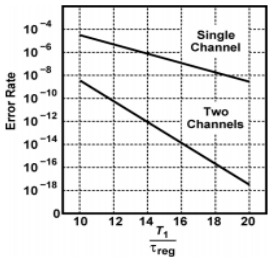


Fig.4. Reduction of Metastability Error as a Result of Interleaving

III. DISADVANTAGES OF INTERLEAVING

In addition to interchannel mismatches and the area penalty, interleaving entails a number of other issues as well.

A. *Multi-Phase Clock Generation and Distribution*

The large footprint of each channel in an interleaved system inevitably translates to long, complex interconnects for the clock phases (and/or the analog input). Thus, timing mismatches manifest themselves in both the generation and the distribution of the clock phases. For two channels, the use of predictive gating can reduce the timing mismatch to that between only two transistor pairs [11]. For four channels, frequency division provides a compact and efficient solution but for larger N, more complex techniques such as phase interpolation may be necessary. Retiming and gating prove useful in these cases as well.

Unfortunately, in practical implementation the interleaved channels can have different offsets, gains and bandwidths, and the phases of the sampling clocks are not necessarily equidistant. The effects of these mismatches on the spectrum of the output signal are analyzed in the following sections.

B. *Offset Mismatch*

An ADC offset is a random additive error typically coming from the comparator offset. In a single-channel ADC the offset error creates a DC tone that can be easily removed and is often ignored in many communication applications. The impact of the offset errors is much more detrimental in time-interleaved ADCs. If o(i) is the offset of the i^{th} channel, then, for a given input signal $v_{in}(t)$, and

assuming no other errors, the output signal can be written as:

$$D_{out}(n) = v_{in}(nT) + o((n - 1) \bmod M + 1)$$

where mod is a modulo operation. $o((n - 1) \bmod M + 1)$ is a periodic discrete signal with a period equal to M. This means that in addition to our desired signal $v_{in}(t)$, the spectrum of the output signal will have tones at frequencies that are multiples of f_S/M . The magnitude and relative strength of these tones depends on the amplitude and the shape of the introduced periodic error signal.

C. *Gain Mismatch*

Gain errors manifest itself as a change in the slope of the transfer function of an ADC. The gain error can come from a difference in reference voltages or from the sampling operation(e.g. charge injection). The gain of the i^{th} channel can be expressed as $1 + \Delta g_i$, where Δg_i (ADC) commonly use multiple ADCs whose sample clocks have staggered phases.

is the gain error in the i^{th} channel. The composite output of the time-interleaved ADC can be written as:

$$D_{out}(n) = v_{in}(nT) + \Delta g((n - 1) \bmod M + 1)v_{in}(nT).$$

$\Delta g((n-1) \bmod M + 1)$ is a periodic discrete signal with a period of M and can be represented in frequency domain by discrete tones at frequencies kf_S/M, $k = 0..M - 1$. If the input signal is a sinusoid with the frequency f_{in}, the mixing effect of multiplying the input signal with the periodic signal $\Delta g((n-1) \bmod M + 1)$ will create tones at frequencies $kf_S/M \pm f_{in}$. An example of the output spectrum with gain mismatches in the case of a 4-way time-interleaved ADC is shown in Fig. 4(b).

D. *Timing Mismatch*

The phase difference between the clocks of the neighbouring channels should ideally be equal to $2\pi/M$. The phase (or, equivalently, timing) errors are unavoidable in a practical implementation due to finite propagation of the clock signal and variations in the clock buffers and sampling switches. At high input signal frequencies even small timing mismatches can create significant errors. If we denote the timing mismatch in the i^{th} channel by $\Delta t(i)$, then, for a sinusoidal input signal, the output signal can be expressed as:

$$Dout(n) = \cos(\omega nT + \omega\Delta t((n - 1) \bmod M + 1))$$

The input signal effectively becomes phase modulated by the periodic signal $\omega\Delta t((n-1) \bmod M + 1)$ with period M that has spectral components at kf_S/M . The location of the spurs is same as the location of the spurs that stem from the gain mismatches. Unlike in the case of the gain mismatch, the magnitude of the spurs depends on the input frequency. This gives a way of isolating the gain mismatches by performing a low-frequency testing, where the artifacts due to timing mismatches are not visible. The timing mismatch can be corrected in the digital domain by means of a finite-impulse-response (FIR) filter or in the analog domain by means of a variable delay line.[3]

IV. PROPOSED TIME INTERLEAVING DESIGN

This section discusses the building blocks for the Time Interleaved Analog to Digital blocks. Many digitized test and measurement applications requiring both high resolution and high sampling speeds in excess of what can be delivered by a single Analog-to-Digital Converter

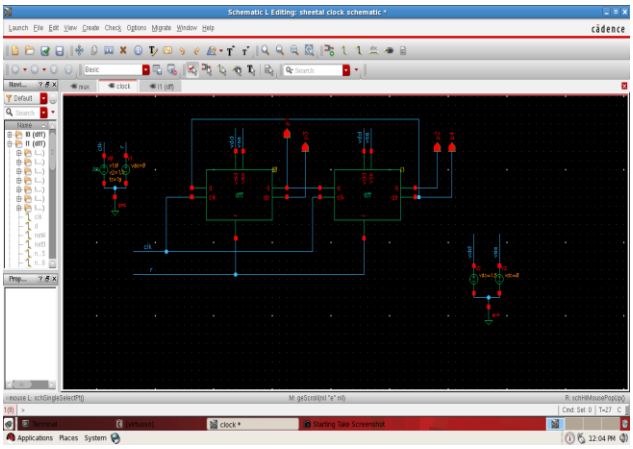


Fig. 5. Four-phase Clock Generator in UMC 65nm Technology

Mathematically, the concept is simple. Even though each ADC is clocked at the same speed, the evenly staggered clock phases result in an effective increase in sample rate.

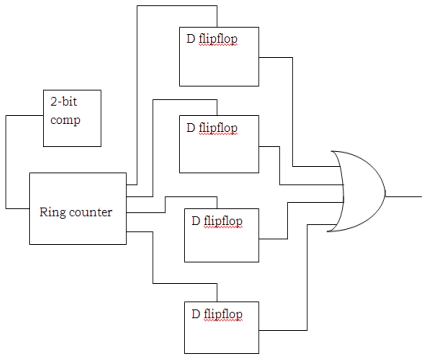


Fig. 6. 4:1 Multiplexer block diagram

A. 4:1-Multiplexer

Time interleaving of multiple analog-to-digital converters (ADCs) offer a simple and excellent method for increasing the sampling rate of existing high performance ADCs by multiplexing their outputs. Here four 500 Megasamples/sec with 12-bit of resolution digital signals are multiplexed to form an aggregate 2 Gigasamples/sec single digital output signal.

Steps involved in designing 4:1 multiplexer: 1. Design of D-flipflop with enable input, 2. Design of 2-bit comparator, 3. Design of 4-bit ring counter, 4. Final design of 4:1 mux using above 3 circuits.

Firstly, a D-flipflop with enable input is designed. Then a 2-bit identity comparator shown in Fig.6 (an Identity Comparator is a digital comparator that has only one output terminal for when A = B either "HIGH" A = B = 1 or "LOW" A = B = 0) is designed, output of which has 25% duty cycle is fed as input to 4-bit ring counter. The 4-bit ring counter is used to enable each of D-flipflop to switch the input to the output terminal.

B. Bootstrap Switch

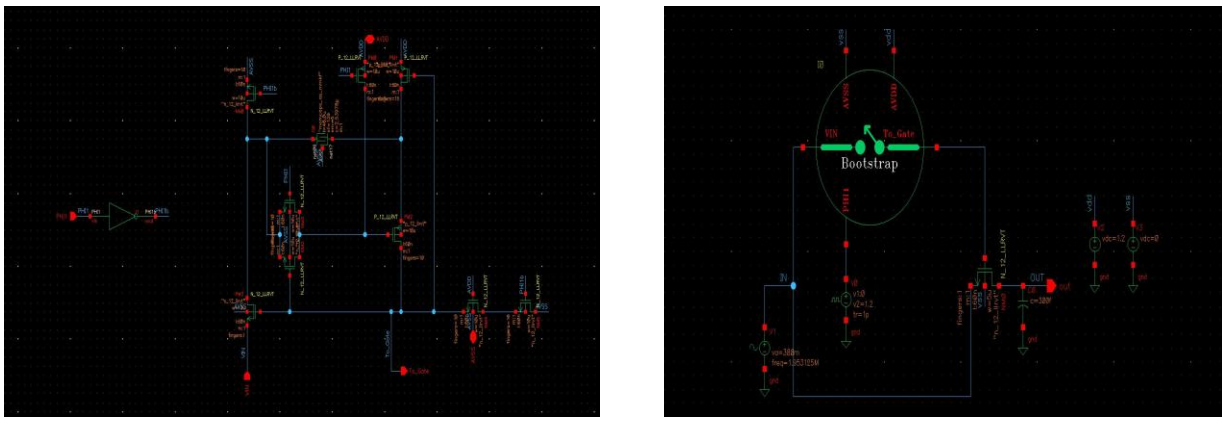
A time-interleaved Analog-to-Digital Converter (ADC) includes set of time multiplexed sub-ADC circuits, each sub-ADC circuit consists of a sample-and-hold circuit.

Each sample-and-hold circuit includes a bootstrap circuit for maintaining a constant voltage level between an input terminal of a switch and gate terminal of the switch, the switch to sample the input signal on a sampling clock edge and hold that sampled signal value for subsequent signal processing by the sub-ADC circuit, and a capacitor bank associated with the bootstrap circuit such that a setting of the capacitor value affects the voltage level.

The bootstrapped switch, shown in Fig. 7, performs the S/H function. With the bootstrapped switch, the gate-source voltage of the sampling transistor is fixed at the supply voltage V_{DD}, which makes the on-resistance a small constant value and thus improves the switch linearity.

C. Top Level Time Interleaving Design

In this work time interleaving is performed using ideal ADCs which are generated using Verilog A code. In the time-interleaved ADC illustrated in Fig. 8, the timing signal is used to divide the analog input signal into different sub-signals according to time. At the first sampling instant the input signal is sampled by sub-ADC**1.** At the next sampling instant, the input signal is sampled by sub-ADC **2**.This process continues as subsequent sampling instants are sampled by sub-ADC **3** and sub-ADC **4**. At the sampling instant immediately after the one sent to sub-ADC **4**, the input signal is again sampled by sub-ADC **1**.Thus, a given sub-ADC samples every fourth sampling instant. Because each sub-ADC only has to process every fourth sampling instant, the overall sampling frequency of the time-interleaved ADC can be increased.



(a) (b)

Fig.7. Bootstrap Switch (a) Transistor Level Circuit, (b) Cadence Implementation

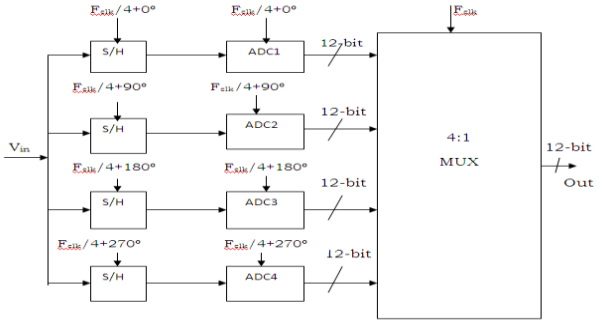


Fig. 8. 4-time Interleaved ADC Design

V. SIMULATION RESULTS

A. Input Frequency Calculation

When evaluating the dynamic performance of analog-to-digital converters (ADCs) using Fast Fourier Transforms (FFTs), one use coherent sampling. In general, coherent sampling produces the best quality in high-resolution FFTs. The purpose of coherent sampling is to force an integer number of input cycles within the sampling window.

Mathematically, coherent sampling is expressed as:

$$\frac{f_{IN}}{f_{SAMPLE}} = \frac{N_{WINDOW}}{N_{RECORD}}$$

where:

- f_{IN} is the input frequency of the ADC under test.
- f_{SAMPLE} is the sample frequency of the ADC under test.
- N_{WINDOW} is the integer number of cycles within the sampling window. This value must be an odd or a prime number.
- N_{RECORD} is the number of data points used to create your FFT. This value must be a power of 2.

If we consider 1024 samples ie $N_{RECORD}=2^{10}$ in one sine wave and clock frequency f_{SAMPLE} is 2 Ghz.

Then T_S=500ps

We get T_{IN} = 500ps*1024 = 512ns

So, the input frequency $f_{IN} = 1/T_{IN}$ = 1.953125Mhz

Transient analysis:

The time axis has been taken for two iterations i.e. from 0 to 1.024us, since the input frequency applied is 1.953125Mhz. The result is shown below

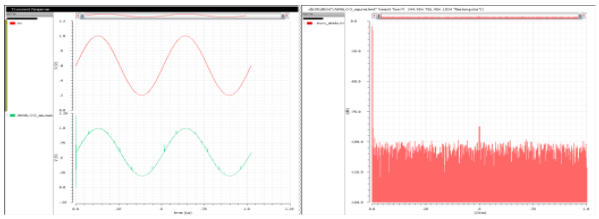


Fig. 10. Simulation Result of Time Interleaved ADC with Input Frequency of 1.953125M

Table 5.1 : TI-ADC Simulation Setup and Results

Sl. No.	Parameter	Value
1	Technology Process	65nm
2	Supply Voltage	1.2V
3	Sampling Rate	2GS/s
4	ENOB	11.21 bits
5	SNR	69.438 dB
6	SNDR	69.249 dB
7	SFDR	79.09 dB
8	Power - Individual SAR ADC	10 mW
9	Power – Time Interleaved Logic	0.32 mW
10	Total Power – 4-Time Interleaved ADC	40.32 mW

The primary purpose of this work is to reduce the timing complexity, analyze the additional power required for the implementation of TI aspect as compared to single channel ADC. Transient analysis have been performed to determine the behaviour of the circuit. In an earlier work performed by research group, the SAR ADC power measured is 10mW for individual ADC channel. As proposed work requires 4 redundant copies of ADC operating under same simulation setup consumes a total power of 40mW.

VI. CONCLUSION

The proposed work is implemented with motivation to provide a reliable solution that reduces the clock generation complexity and at the same time providing high data rate for communication transmissions. The channel mismatches include gain, offset and phase/timing mismatch. The affects of above mentioned mismatches on the performance of the TI ADC and techniques used to mitigate these errors are discussed. The detailed analysis of TI-ADC with 12-bit resolution is presented where an additional power required to enable TI aspect is only 0.32mW.

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