Design of Low Power Digit-serial Adder Filter

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Abstract

In the occurrence of DSP applications the weighted operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit that consumes low power is always a means to achieve a high performance digital signal processing system. Finite impulse response (FIR) filters are widely used in various DSP applications like data converters. Until many proficient techniques have been introduced for the design of low snag bit-parallel multiple constant multiplications (MCM) process which reduces the complexity of many digital signal processing systems. On the other hand, digit-serial adder architectures present remarkable n-bit designs which process dynamic size data, since digit-serial operators hold less area and power. The purpose of this work is to design and implementation of low power optimized digital Finite impulse response (FIR) filter architecture using VLSI technique. We design and analyze Transpose using MCM and digit serial adder. Experimental results found best performance results of Transpose using MCM and digit serial adder design in terms of area and power.

Keywords - *digit- serial adder architecture, FIR, Low Power, MAC, MCM.*

I. INTRODUCTION

In high freq data converters signal were present with noise therefore we needed to process the combination of this data to filter out desired data. there are two options to filter out this data i.e. soft computing and hardware implementation of filter.

soft computing demands development of code for filter, based on dsp processor or non dsp architecture processor. but still dsp processor needs development of filter code even though it's having mac (multiply accumulation) structure inside, there is no issue of non dsp processor it needs huge efforts to develop filter code without mac structure. it is an overhead to software developer to develop a code. again it is based on sequential programming and sequential execution, which needs much time to produce more output [9].

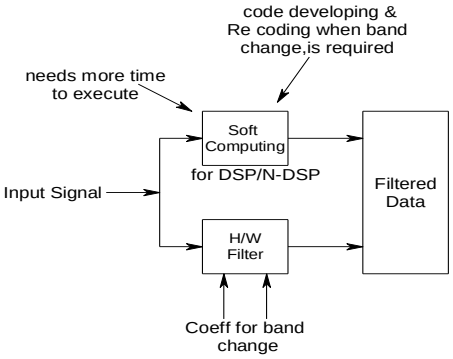


Fig-1 Proposed Design

It is an overhead to processor so, it demands h/w for such time consuming process. Hence soft computing is not suitable for run time variations.

Intended for the design of digital filters, the system function H(z) or the impulse response h(n) must be specified. Then the digital filter structure can be implemented or synthesized in hardware/software form by its difference equation obtained directly from H(z) or h(n).Each difference equation or computational algorithm can be implemented by using a digital computer or special purpose digital hardware or special programmable integrated circuit[15].

In order to implement the specified difference equation of the system, the required basic operations are addition, delay and multiplication by a constant.

FIR filter is a type of signal processing filter whose impulse response is of finite duration, because it settles to zero in finite time. FIR is also known as non recursive digital filter as they do not have the feedback.

In general FIR filter are normally designed to have a linear phase response and there is also great flexibility in shaping their magnitude response. In addition, FIR filters are inherently more stable and the effect of quantization errors is less severe than IIR filters.

Infatuated systems requiring different sample rates will need to be implemented in bit-serial, bit-parallel and digit-serial. Bit-serial technique process one input bit at a time and is functional for low-speed applications. These systems require fewer interconnections, less hardware. Bit-parallel systems process all input bits of a word in one clock cycle, and require the leading area, interconnection. These

systems are best for high-speed applications. Whereas digit-serial systems process more than one input bit in one cycle. These systems are perfect for mild speed applications, for which bit-serial method is too slow, and bit-parallel method is faster than essential. The number of bits processed per cycle is referred to as the digit-size. For concord digit-size, the design reduces to a bit-serial system, and for digit-size equal to the word-length, the design reduces to a bit-parallel system. In this paper, an efficient design methodology for low power optimized filter is presented.

II. ORIGIN OF FILTER COEFFICIENT AND RESULT OF FILTER

FIR filter are often preferred in many applications, since they provide an exact linear phase over the whole frequency range and they are always bounded i/p bounded o/p (BIBO) stable independent of the filter coefficients. The convolution sum relationship gives the system response as

$$R = \sum_{k=0}^{M-1} x(n-k)*h(k) \qquad \text{---------- eqn(1)}$$

Where R and x(n) are the output and input sequences, respectively. This equation gives the input-output relation of the FIR filter in the time domain. The realization for this equation is shown in following filter architectures which is the set of basic elements like latch, multiplier & adder [13].

By using Matlab 'fdatool' we have design the filter of 17 order, FIR type– equiripple, Density–20, Low pass,Fs-48Khz Fpass-9.6Khz and Fstop-10Khz. We get the required coefficient in floating point as the size of floating point representation is in 32/64/128 bit which will lead more area so we transform the floating point into integer with no change in filter response, after plotting the filter response of both float and integer of coefficient we conclude that, we can go with integer with no effect in filter response [3]. We get the 'h' as follows and Matlab convolution result as 'R'

h= [16 9 10 12 12 9 1 16 81 81 16 1 9 12 12 10 9 16];

------hvalue(1)
x=1:20; ----------xvalue(1)
R=conv(x, h) ----------mat_cmd(1)
R = 16 41 76 123 182 250 319 404 570 -------- mat_result(1)

III. FILTER ARCHITECTURE AND SIMULATION RESULTS

A. *Direct Form*

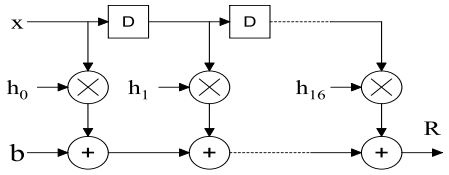


Fig- 2 Design for Direct Form

Direct form implementation using basic elements like latch, multiplier & adder. The input size is of 8 bit so latches are of 8 bit size, multiplier is of 8x8 so, results is of 16 bit, adder is of [16 + no of tap i.e.17] ~ 32bit, which is taken with consideration of maximum values of coefficient and input X. Multiplier & adder be implemented using std ieee library of
VHDL which is default in its definition [15].

B. *Transpose Form*

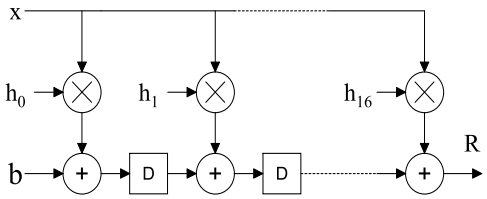


Fig- 3 Design for Transpose form

If the two digital filter structures have the same transfer function, then they are called equivalent structures. A simple way to generate an equivalent structure from a given realization structure is via the transpose operation. The transposed form is obtained by (i) reversing the paths, (ii) replacing pick-off nodes by latches and (iii) interchanging the input and output nodes. For a single input-output system, the transposed structure has the same transfer function as the original realization structure. As shown in figure by replacing pick-off node with latches the total cell area of transpose form get increased as compare to direct form. As well as total dynamic power also get increased [13].

Transpose form implementation is done using basic elements like latch, multiplier & adder. The input size is of 8 bit , here the main area intense element is latches with respective to DFF in-place of 8 bit size here 32 bit size is needed so area get increases, all other modules are same as that of direct form.

C. MCM Form

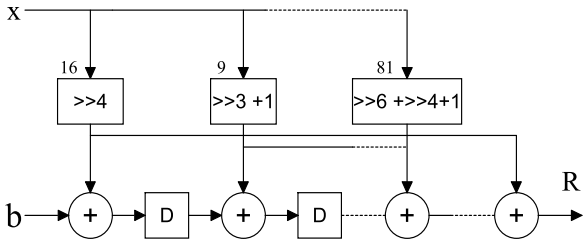


Fig-4 Design For Transpose MCM

Here we replace the conventional multiplier with shift add method of multiplication. Again as we were design filter with equiripple approach, so we can reuse multiplication result for the similar coefficient values, which considerably reduce the area and power with respective to direct and transpose form. Fig.5 shows the example of one of the coefficient (81X) from series [4].

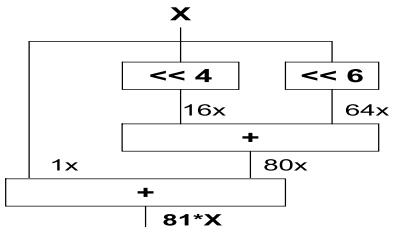


Fig-5 Shift- Adds Implementation Of 81X

D. Bit-Serial Adder

1010
+
1100
10110

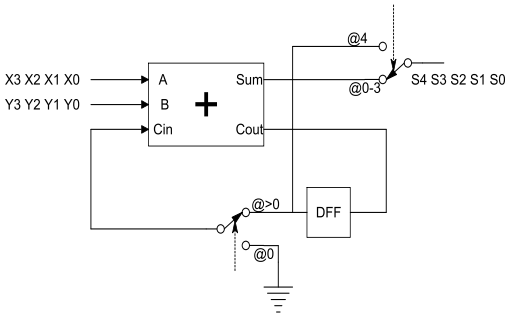


Fig-6 A Bit-Serial Adder For Word Length Of 4

Fig. 6 shows the bit-serial architecture for word length of 4 (W=4). This adder adds two four bit numbers X3X2X1X0 and Y3Y2Y1Y0 to get 4 bit sum S3S2S1S0 where bit 0 is the least significant bit and bit 3 is the most significant bit. Initially cin=0, we have to kept cin=0 using switch, after it we force full-adder with data X0Y0 we get the value of sum S0. For next iteration we connect cout to cin using switch and we force the full-adder X1Y1 we get the value of S1 and so on.

E. Digit-serial Adder

In parallel system speed, power is high and in addition area constraint is also high, to shrink the power and area we prefer bit-serial structural design but it might be slow in speed. Although we gain the power and area constraint but it lost the speed. So there is no need of such an architecture while balance the things, that is speed, area and power constraint. This is stimulus to design a digit-serial architecture.

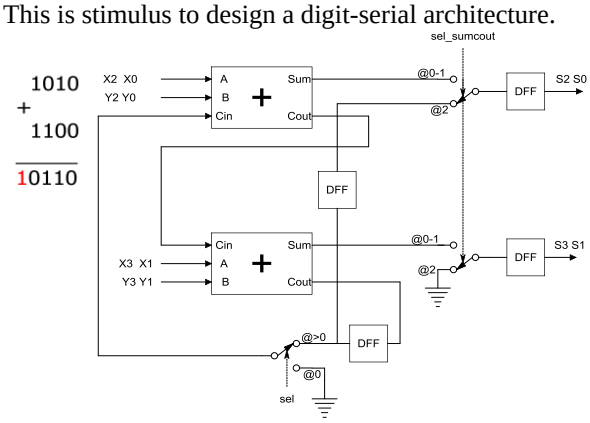
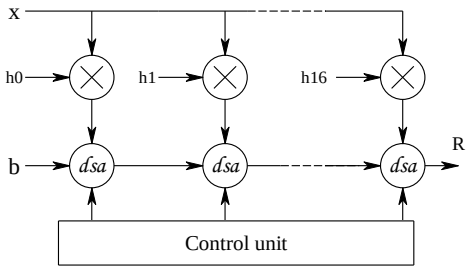


Fig-7 Digit Serial Adder For Digit-Size Two



dsa = digit serial adder (2 bit digit size)

Fig-8 Architecture For Digit Serial Adder (Transpose)

Total Dynamic power(mW)	7.3128
Total Cell Area(µm^2)	13424.326

Fig. 10 shows the design for digit serial adders using transpose and MCM along with the control unit which can reduce significant amount of power and area.

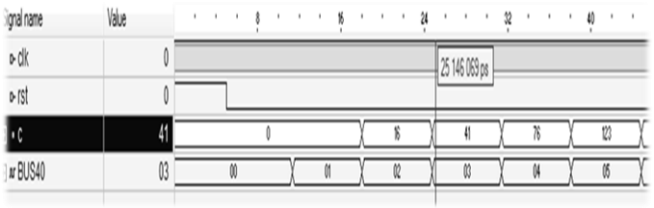


Fig-11 Simulation for Digit Serial Adder Using Transpose MCM

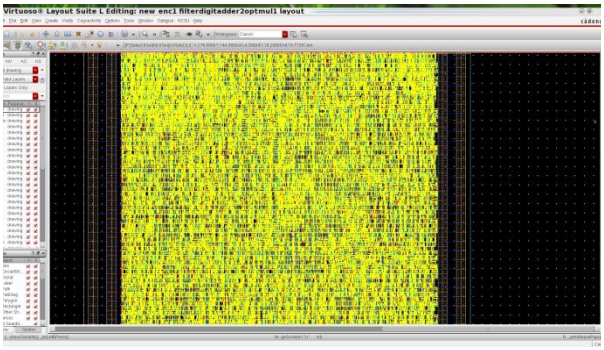


Fig- 12 Design Layout for Digit Serial Adder Using Transpose MCM

IV. CONCLUSION

This paper introduced the design architectures for the transpose using MCM and digit-serial adder operation for the realization of FIR filters. The experimental results indicate that the complexity of direct form, transpose form designs can be minimized by using the digit-serial MCM operation proposed here. It was revealed that the knowledge of digit-serial MCM FIR filter under the shift-add architecture yields vital area and power reduction when compared to the filter designs with other four i.e. direct, transpose, transpose using MCM, and transpose using digit serial adder form.

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