Realization of BIST Architecture using SRAM Cell Based on Input Vector Monitoring

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Abstract

To perform testing during normal operation of the circuit, without forcing the circuit to go offline is concurrent BIST testing. Built-In Self Test (BIST) techniques constitute an attractive and practical solution, to solve the problem of testing VLSI circuits and systems. In this paper, we perform input vector monitoring BIST scheme, by monitoring a set of vectors called windows during its normal operation and the testing of the circuit is also carried on along with its normal operation of the circuit.

Keywords – *BIST, CUT, Concurrent, Input Vector Monitoring, Online BIST.*

I. INTRODUCTION

In recent years, the advent of VLSI, has increased the complexity of digital circuits at an exponential rate. Increased circuit complexity also complicates the testing problem. A device is tested at different stages of manufacturing and hence it is a continual problem. It must undergo an acceptance test before it is integrated into a system .To ease testing, two new disciplines have emerged namely, design for testability (DFT) and BUILT-IN Self Test (BIST).Both these disciplines require adding extra logic to alleviate the testing problem. In DFT environment, the extra logic is active during the test mode(off-line)operation of a logic circuit and such logic is idle during normal operation of the circuit .BIST techniques, can be used either for on-line or off-line. The introduction of nanotechnologies and SOC devices brings forth new problems in semiconductor memory testing.So researchers have been attracted towards BIST architecture due to it ease toward testing. The use of BIST circuits and other embedded instruments is becoming more prevalent as devices become larger, faster, and more complex. These instruments can increase the device's test coverage, decrease test and debug time, and provide correlation between the system and ATE environments. Examples of some of these instruments are logic BIST, memory BIST (for both internal and external memory), bit-error-rate testing for serializer/deserializer (SerDes), power management and clock control logic, and scan register dump capabilities.

II. BIST TECHNIQUE

Built-In Self Test is a practical solution to provide the system with an attractive test solutions. BIST is an in built set up to provide the system with an effective and economic way to find the effectiveness of the system. For this testing BIST constitutes two types of modes on-line and off-line mode. Periodic testing of IC is done at system level should be done, to prevent accumulation of faults. Such periodic testing is done off-line that is system is stopped and tested using a set of vectors. But off-line mode provides a performance degradation since it affect the normal operation of the circuit. On-line mode is testing the Circuit , during its normal operation without going into off-line mode.there by it increases its performance and efficiency. On-line BIST uses normally occurring data as inputs and employs redundancy techniques to do concurrent checking. Concurrent means testing occurs simultaneously with normal functional operation (Realized by using coding techniques) and Non-concurrent means testing is Carried out while in idle state.

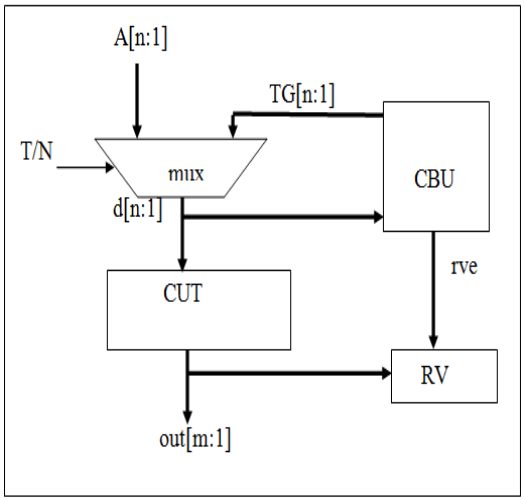

Figure 1.1: Input Vector Monitoring Concurrent BIST

III. PROPOSED ARCHITECTURE WITH INPUT VECTOR MONITORING

In the proposed architecture , a modified decoder and an SRAM logic block is used.A decoder has been modified by applying comparator signals and test generator enable signals with implementation of and gate and or gate.The decoder will have w

inputs and W outputs with control signals, comparator and test generator enable.

IV. MODULE DESCRIPTION

The BIST module has CUT, Mux , Response Verifier(RV) and Concurrent BIST Unit(CBU).In CBU it consists of sub-modules of Logic, Comparator , Modified decoder , Test Generator(TG) each one of the block is explained in detail in the below passages.
Mux: The data multiplexer of the BIST architecture select whether normal mode or test mode(BIST provided inputs). It act as a control element or as a switch ,indicating in which mode the circuit should operate, depending on the value of the signal labeled T/N.

Circuit Under Test (CUT): Circuit under test (CUT) can be the entire chip or only a part of the chip (e.g., a memory core or a logic block). Input test vectors are binary patterns applied to the inputs of the CUT and the associated output responses are the values observed on the outputs of the CUT. The CUT has n inputs and m outputs and is tested exhaustively hence the test set size is $N=2^n$.

Concurrent BIST Unit (CBU): CBU consists of sub–blocks of TG, Comparator, Decoder and Logic circuits.Test Generator: It is a test pattern generator module which receives its input from Logic module and its output is driven to mux.To provide the input vectors, generated from CBU.Comparator: It compares the outputs of test generator and Mux and provide its output to decoder and Logic. When the the output of the decoder is enabled ,the decoder module operates as a normal decoding structure.Response Verifier: The Response verifier stores the result of CUT and Logic .Once when the circuit attain all the hits ,the results in the response verifier are viewed latter.

V. FUNCTIONALITY OF THE PROPOSED ARCHITECTURE

The select line of mux T/N will decide whether the module will work in test mode or normal mode.If Test mode means,the inputs for the CUT are generated from the output of CBU denoted as TG[n:1].Test Generated module.If ,normal mode means the inputs for the CUT are generated by A[n:1].For both the mode the responses are captured in the response verifier(RV).The Circuit Under Test has n inputs, m outputs and is tested exhaustively.The test set size for the CUT is N = 2n. The BIST module consists of a CUT which is combinational with n input line,a Mux to determine whether to operate it in test mode or normal mode,a CBU and a RV to capture the responses of CUT with its corresponding . The basic idea is of monitoring a window of vectors,of size W ,which is W=2w,where w is an integer w < n.The input vector n is divided into two parts w and k,in which k is the higher order and the remaining w bits show the location of the current window.The vectors in the current window are monitored ,and if a vector performs a hit,RV is enabled. Once the vectors in the current window are monitored,then it goes to the next window.w bits are given to the modified decoder with the functionality as ,When tge is 1 ,all the output will be enabled.If cmp is disabled and tge is disabled then all the outputs will be disabled.when cmp is enabled and tge is disabled then the circuit will operate in normal mode.

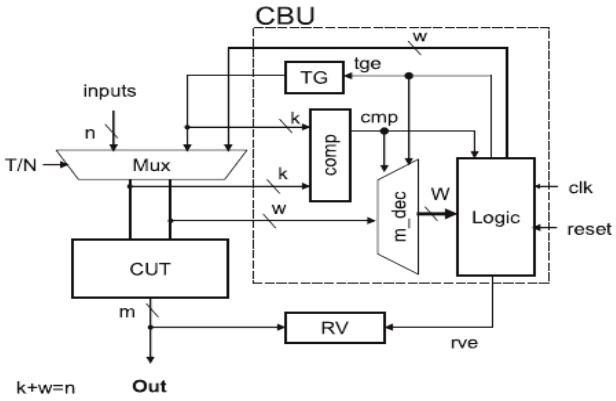

Fig 2:Logic Block

VI. OPERATION OF LOGIC MODULE

The logic module consists of W cells (operating like SRAM cell), an amplifier(sense) , then two D flip-flops, and a w-stage counter (where w = log2W). The tge signal was triggered by a unit flip-flop delay by the overflow signal of the counter. The clock signals(clk and clock) are enabled during the active low and high of the clock, respectively.

The functionality of the logic module can be explained in a set of five operations ,first need to reset the module ,then hit of the vectors are monitored whether they reached the windows already or they are appearing for the first time and then the tge operation is monitored .

The module is reset by an external reset signal. Once the reset was triggered , the tge signal is enabled and all the outputs of the decoder are enabled. So, DA1,DA2, . . . , DAW are one and the CD_ signal is enabled; therefore, a one is written to the right hand side of the cells and a zero value to the left hand side of the cells.

Then the hit of the vector is being monitored.During normal mode, the inputs to the CUT are taken from the normal inputs. The n inputs are also driven to the CBU as follows: the w low-order inputs are driven to the inputs of the decoder; the k high-order inputs are driven to the inputs of the comparator. When a vector belonging to the current

window reaches the inputs of the CUT, the comparator is enabled and one of the outputs of the decoder is enabled.

During the first half of the clock cycle (clk_ and cmp are enabled) the addressed cell is read; because the read value is zero, the w-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During the second half of the clock cycle, the left flip-flop (the one whose clock input is inverted) enables the AND gate (whose other input is clk and cmp), and enables the buffers to write the value one to the addressed cell.If the cell corresponding to the incoming vector contains a one (i.e., the respective vector has reached the CUT inputs during the examination of the current window before).The rve signal is not enabled during the first half of the clock cycle; hence, the w-stage counter is not triggered and the AND gate is not enabled during the second half of the clock cycle.

When all the cells are full (value equal to one), then the w-stage counter is all one. Hence, the activation of the rve signal causes the counter to overflow; hence in the next clock cycle (through the unit flop delay) the tge signal is enabled and all the cells (because all the outputs of the decoder are enabled) are set to zero.When switching from normal to test mode, the w-stage counter is reset. During test mode, the w-bit output of the counter is applied to the CUT inputs. The outputs of the counter are also used to address a cell. If the cell was empty (reset), it will be filled (set) and the RV will be enabled. Otherwise, the cell remains full and the RV is not enabled.
Once when these operations are completed the output from the logic module is stored in the RV where the output of the CUT are compared with the logic output .

VII. SIMULATION RESULTS

The verilog HDL coding and simulation of the design are done in Xilinx tool ISim 14.4.The simulated output of BIST architecture using Input vector monitoring is faster than its previous[1-7] results.It is been displayed with timing diagram of the logic and SRAM cells.

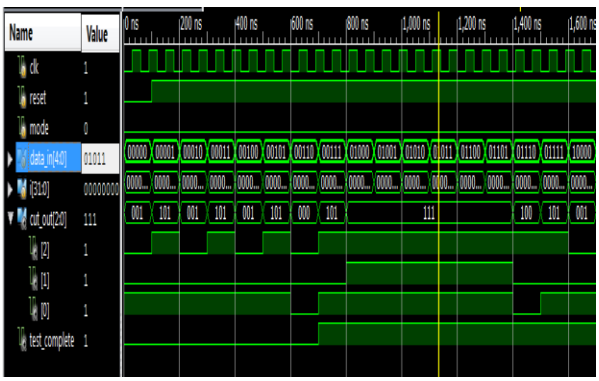

Fig 3:Simulated Result

VIII. CONCLUSION

In this paper, it present an Xilinx ISE simulated results for input vector monitoring BIST architecture using SRAM –cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The result shows that ,with the same hardware overhead, the proposed scheme achieves shorter CTL than other schemes.Like,in terms of hardware overhead the proposed scheme is 16% less number of gates than SWIM and 33% less number of gates than w-MCBIST. It resulted that decrease in hardware overhead obtains higher as the CTL decrease. The result show that the proposed scheme is more efficient than the existing system with in terms of hardware overhead and CTL.

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