Simulation of Communication Channels using FPGA / VHDL a Brief Review with Implementation Concepts using Hardware and Software

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Abstract

In this paper, a brief review about the design of communication channels using FPGS – VHDL environment is presented, which will be very useful to design the communication channels in the software environment. The simulation results shown depicts the novelty of the method developed & shows its effectiveness.

Keywords – *Communication, Channel, FPGA, VHDL, Tx, Rx, SISO, MIMO*

I. INTRODUCTION

Multiple Input Multiple Output (MIMO) Communication System is a new and emerging technology and is expected to play a very important role in 4G wireless systems. FPGA prototyping of MIMO provides an accelerated and repeatable test environment in a laboratory setting [1]. MIMO systems have evolved rapidly as a generic technology of communication in 4G wireless systems [2].

MIMO technology makes use of multiple antennas both at the transmitter section and at the receiver section to make excellent utilization of the available bandwidth and to reduce the effects of fading and signal loss. This technique also helps to increase the number of bits transmitted i.e. bitrate. Most recently MIMO systems are also used in wired power line communications for 3-wire installations. The prototyping of MIMO systems by using FPGA's or ASIC's provides an alternative testing environment for MIMO systems [3] as the practical realization and testing of MIMO technology is complex and costly. MIMO-OFDM is used in LTE [4].

Field Programmable Gate Arrays (FPGA) are integrated circuits which can be configured by the user or developer by using any hardware description languages (HDL) such as VHDL or Verilog. FPGA's provide a hardware testbed using which the testing and evaluation of many logic networks or circuits or systems can be done [1, 3]. FPGA's consists of large number of logic gates and memory blocks (RAM blocks) to implement complex digital computations.

An important challenge for the MIMO technology would be the design of the transmitter and receiver sections which involves complex algorithms at both sections [5, 7]. The design and testing part can be simplified by designing the circuits using hardware description languages (HDL) and Integrated Software Environment (ISE) which provides accurate simulations of the design. In order to provide a hardware testbed for the MIMO systems, the designs can be synthesized into FPGA's. This type of prototyping of the MIMO system will provide an excellent testbed under which testing of MIMO can be done and also important parameters such as delay in communication, bit error rate, SNR etc., can be determined.

Thus this type of prototyping of MIMO on an FPGA is also a convenient method to check the suitability of alternate algorithms and evaluating hardware tradeoff's. This prototyping provides verification of physical layer design ideas and makes the designing more economical [6]. FPGA's can also be used to implement a communication system directly as the complexity of baseband communications are high and there is always a need to do reprogramming due to changes in evolving standards.

II. LITERATURE SURVEY

FPGA based prototyping of MIMO systems provide excellent testbed for testing and evaluation of transmitter and receiver algorithms. Research in the field of MIMO and also on prototyping of MIMO on FPGA's are being carried out from many years. A brief survey of some of the important literatures in this field has been presented in the subsequent section.

A. Reference Paper 1

Amirhossein Alimohammad and Saeed Fouladi Fard, "FPGA-Based Bit Error Rate Performance Measurement of Wireless Systems",IEEE Transactions On Very Large Scale Integration (VLSI) systems, ISSN No: 1063-8210,volume 22, Issue: July 2014, Pages:1583-1592, Publication: 21 August 2013.

In this paper the development and testing of an FPGA based bit error rate tester for digital baseband communication systems have been developed. The bit error rate tester is developed for both multiple input multiple output (MIMO) and single input and single out put (SISO) digital communication systems. The paper demonstrates the techniques to develop a complete transmitter and receiver section for a 2×2 MIMO and SISO system. The transmitter system uses Golay coding technique for channel encoding, followed by a pseudorandom interleaver section and a 16-QAM modulation technique. The receiver section consists of ML detector, pseudorandom de-interleaver and decoder. The paper also discusses the issues of noisy channels and ways of data reception through noisy channels.

B. Reference Paper 2

Numan, M.W, Islam, M.T., Misran.N., "An efficient FPGA-based hardware implementation of MIMO wireless systems" Communication Systems Networks and Digital Signal Processing conference , ISBN: 978-1-4244-8858-2, pages: 152-156 Conference date: 21-23 July 2010.

This paper presents an efficient hardware realization of a 2×2 MIMO system which is designed and implemented on a Xilinx Virtex -4 XC4VLX60 field programmable gate array (FPGA). In this paper the design of MIMO involves a transmitter section consisting of Alamouti encoding and Inphase – Quadrature (I-Q) modulation schemes. The paper discusses the use of a new and completely different decoding technique for the MIMO system. The paper discusses the use of Matlab and VHDL for the development of the system where both matlab and VHDL simulations are done and both are compared to check for the similarities. The synthesis is done using VHDL.

C. Reference Paper 3

A. Alimohammad, S. F. Fard, and B. F. Cockburn, "FPGA-accelerated baseband design and verification of broadband MIMO wireless systems," in Proc. IEEE 1st Int. Conf. Adv. Syst. Testing Validation, Sep. 2009, pp. 135–140.

This paper discusses the prototyping of the physical layer of a 2×2 MIMO system on a Xilinx Virtex–E XCV2000E FPGA. The paper discusses the complete implementation of the baseband layer of a 2×2 MIMO with the transmitter section consisting of channel coding, interleaving and modulation. The receiver part consisting of ML detector, De-interleaving and channel decoding are also discussed. The paper finally discusses the design of a Bit error rate tester for the MIMO by comparing the received bits with a copy of the transmitted bits from the source.

D. Reference Paper 4

Yu Heejung, Kyon Ghee song, Kwhanghuyn Ryn "Design and FPGA implementation of MIMO-OFDM based WLAN system" Vehicular technology conference VTC-2006 spring IEEE 63, volume 3, pages 1333-1338, publication year: 2006.

This paper discusses the design of a transmission architecture based on dual band and MIMO-OFDM schemes and media access control (MAC) layer using the enhanced distributed channel access (EDCA) including a block acknowledgement method (ACK). The complete system is synthesized in an FPGA and verified. This paper discusses the development of a 2×2 MIMO system with convolution coding at the transmitter and Viterbi decoding technique at the receiver.

E. Reference Paper 5

Paulraj.A.J, Gore.D.A, Nabar.R.U, Bolcskei.H, "An overview of MIMO communications-a key to gigabit wireless", Proceedings of the IEEE, ISSN:0018-9219, volume:92, pages: 198-218,publication:08 November 2004.

In this paper the methodology of MIMO is discussed in detail, the advantages, disadvantages of MIMO are briefed. The paper also demonstrates the use of MIMO in wireless technology and shows that high data transfer rates in GB/s can be achieved. The paper proves the high capacity of MIMO system over single antenna systems by applying the Shannon's channel capacity formula.

F. Reference Paper 6

Murphy.P, Lou.F, Sabharwal.A, Frantz. J.P., "An FPGA based rapid prototyping platform for MIMO system", Signal Systems and Computer Conference 2004, Record of the 37 Asilomar conference , volume 1, pages:900-904, publication: 2003.

In this paper the design of an MIMO testbed in a Virtex-II FPGA is discussed. Rapid prototyping of MIMO transceivers for wideband channel is discussed. The testbed allows for real time operation of baseband processing and RF up/down conversion. Here the testbed is designed to allow maximum flexibility for research and design purposes. The paper also discusses the implementation of two wireless systems IEEE 802.11b and Alamoutti's transmit diversity scheme using the designed FPGA based MIMO testbed.

The above mentioned literatures discuss the MIMO technology and also give an insight into the prototyping of MIMO on FPGA. Different researchers have used different transmitting and receiving algorithms. A complete description of the transmitter and receiver design is only available in the

reference paper 1. But the design of the encoder and decoder can be further optimized to allow fast communication and minimize the delay in MIMO communication .After referring all the literatures the dissertation aims in creating a completely integrated and miniaturized MIMO system with a detailed transmitter and receiver sections and with a low communication delay.

III. BASICS OF MIMO COMMUNICATION SYSTEMS

Multiple-input multiple-output (MIMO), is a radio frequency wireless communication technology that uses multiple antennas at the transmitter and receiver, is being used in many of the new and upcoming wireless techniques such as LTE, HSPA+ etc. MIMO is used in these technologies as this technique can provide excellent spectral efficiency and an improved link capacity over conventional single antenna techniques. MIMO performs three main functions of spatial multiplexing, spatial diversity and smart antennas.

MIMO development began many years ago. It started with the use of Spatial diversity of antennas in 1990's and was followed by using spatial multiplexing also in 1993 as proposed by researchers Arogyaswami Paulraj and Thomas Kailath. Bell Labs demonstrated the first laboratory prototype of spatial multiplexing MIMO in 1998.Recently MIMO techniques also makes use of smart antenna technology also.

A. *General Diagram of MIMO Communication System*

The figure below shows general MIMO scenarios with M transmit antennas and N receive antennas. The transmitter section and receiver section can be seen along with a multipath channel.

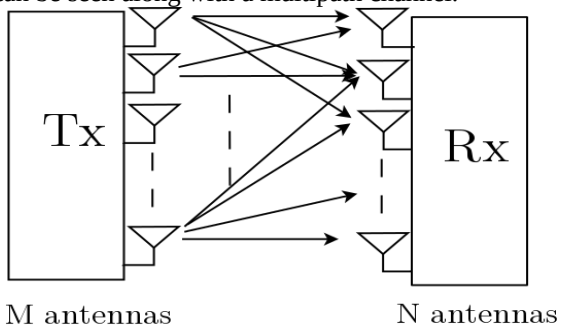

Figure 1: General Outline of MIMO system

As shown in the figure 1 an MIMO system can have M transmit and N receive antennas where the N transmitting antennas might send same signal or different signal to the receiver. Generally N and M are equal and sometimes different. The channel is generally wireless. As can be seen from the figure there are direct path transmission existing between the transmitters and receivers along with many multipath transmissions. The receiver will receive the signal and it decodes the signal accordingly, i.e, the first receive antenna will receive multiple signals through the multipath but it must detect only the signal sent from first transmitter, the same applies to another receivers.

B. *Features of MIMO*

Some of the important features of the MIMO are listed below and it is these features that enable the MIMO with excellent spectral efficiency and higher bit rates.

1) *Spatial Multiplexing*

Spatial multiplexing is a technique where different transmitters transmit different information signals through different antennas. Thus when multiple antennas are used at the transmitting side, the bit rate is increased with an order equal to the number of transmit antennas over a single antenna system. This increases the spectral efficiency as the multiple transmissions happen over a bandwidth that was dedicated for a single antenna transceiver system. Thus higher bit rate communication is guaranteed by spatial multiplexing of MIMO.

2) *Spatial Diversity*

Space diversity or antenna diversity is the use of multiple spatially separated antennas to send and receive redundant information so that the fading effects of channel can be mitigated. MIMO can achieve exactly the same by transmitting redundant data through different antennas and receiving the same across the receivers thus reducing the error rates of the system as well as solving the problem of fading in a practical wireless environment.

3) *Use of Smart Antennas*

In addition to the above mentioned properties MIMO systems can make use of smart antennas with beam forming techniques to improve the signal to noise ratios of the communication systems. By careful use of smart antenna technology the co channel effects can also be mitigated

C. *A 2×2 MIMO Systems*

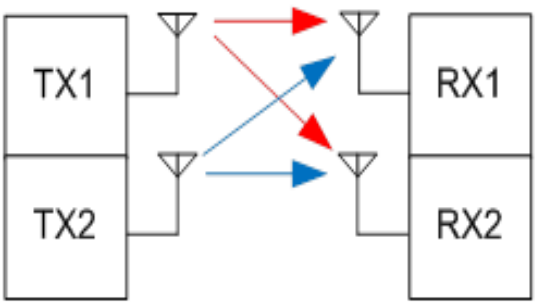

Figure 2: A 2×2 MIMO Communication System Representation

The above figure shows a 2×2 MIMO communication system which is a simplified version

of the generic system shown in figure1. This system has only two inputs and two output antennas .There is a direct path and a multipath between the transmitters and receivers. This type of system is common in some of the wireless communication systems. This type of configuration is generally selected for the study of MIMO systems as the prototyping of these systems are easier and simple.

This dissertation work also aims at developing a prototype of a 2×2 MIMO system along with its complete transmitter and receiver components. The advantage of this system is that it provides a platform to evaluate the performance of an MIMO and it can easily be extended to a m×m system by increasing the transmitters and receivers.

D. Applications of MIMO

MIMO is combined with OFDMA and is used in IEEE 802.16e.MIMO-OFDM is used in IEEE 802.11n. Mobile radio telephone standards such as 3GPP and 3GPP2 make use of MIMO. In 3GPP, High Speed Packet Access Plus (HSPA+) and Long Term Evolution (LTE) standards utilize MIMO. MIMO technology is also used in non-wireless applications such as home networking standard ITU-T G.9963. It is a power line communication system which uses MIMO to transmit multiple signals over multiple AC transmission wires.

E. Drawbacks of MIMO

MIMO systems require multiple parallel hardware costs. MIMO systems also suffers from increased power usage. Real time implementations of complex MIMO systems are challenging and time consuming.

IV. HARDWARE REQUIREMENTS

Artix Field Programmable Gate Arrays (FPGA) are developed by Xilinx. Artix FPGA's consume 50% lower power than the other FPGA's. The cost of artix FPGA's are also low compared to other family of FPGA's. The Artix family is designed to address the small form factor and low-power performance requirements of battery-powered portable ultrasound equipment, commercial digital camera lens control, and military avionics and communications equipment.

V. SOFTWARE REQUIREMENTS

The following section gives a brief description of the various software requirements such as the editor, simulator and the coding language used etc. Verilog language is used as the coding language for the dissertation work. Verify Logic (Verilog) is a Hardware Description Language a textual format for describing electronic circuits and systems. Applied to electronic design, Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis (testability analysis and fault grading) and for logic synthesis.

The Verilog HDL is an IEEE standard - number 1364. The first version of the IEEE standard for Verilog was published in 1995. A revised version was published in 2001; this is the version used by most Verilog users. The IEEE Verilog standard document is known as the Language Reference Manual, or LRM. This is the complete authoritative definition of the Verilog HDL.

A further revision of the Verilog standard was published in 2005, though it has little extra compared to the 2001 standard. System Verilog is a huge set of extensions to Verilog, and was first published as an IEEE standard in 2005. See the appropriate Knowhow section for more details about System Verilog.

IEEE Std 1364 also defines the Programming Language Interface, or PLI. This is a collection of software routines which permit a bidirectional interface between Verilog and other languages (usually C).Note that VHDL is not an abbreviation for Verilog HDL - Verilog and VHDL are two different HDLs. They have more similarities than differences, however.

Verilog descriptions can span multiple levels of abstraction i.e. levels of detail, and can be used for different purposes at various stages in the design process. At the highest level, Verilog contains stochastical functions (queues and random probability distributions) to support performance modeling. Verilog supports abstract behavioral modeling, so can be used to model the functionality of a system at a high level of abstraction. This is useful at the system analysis and partitioning stage.

Verilog supports Register Transfer Level descriptions, which are used for the detailed design of digital circuits. Synthesis tools transform RTL descriptions to gate level. Verilog supports gate and switch level descriptions, used for the verification of digital designs, including gate and switch level logic simulation, static and dynamic timing analysis, testability analysis and fault grading. Verilog can also be used to describe simulation environments; test vectors, expected results, results comparison and analysis. With some tools, Verilog can be used to control simulation e.g. setting breakpoints, taking checkpoints, restarting from time 0, and tracing waveforms.

Verilog is suitable for use in the digital hardware design process, from functional simulation, manual design and logic synthesis down to gate-level simulation. Verilog tools provide an integrated design environment in this area. Verilog is also suited for specialized implementation-level design verification

tools such as fault simulation, switch level simulation and worst case timing simulation. Verilog can be used to simulate gate level fanout loading effects and routing delays through the import of SDF files.

The RTL level of abstraction is used for functional simulation prior to synthesis. The gate level of abstraction exists post-synthesis but this level of abstraction is not often created by the designer, it is a level of abstraction adopted by the EDA tools (synthesis and timing analysis, for example).

The diagram below summarizes the high level design flow for an ASIC (i.e. gate array, standard cell) or FPGA. In a practical design situation, each step described in the following sections may be split into several smaller steps, and parts of the design flow will be iterated as errors are uncovered.

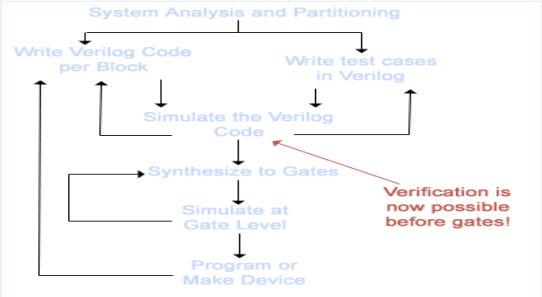

Figure 3 : Design Flow using Verilog

1) ***System-Level Verification***

As a first step, Verilog may be used to model and simulate aspects of the complete system containing one or more ASICs or FPGAs. This may be a fully functional description of the system allowing the specification to be validated prior to commencing detailed design. Alternatively, this may be a partial description that abstracts certain properties of the system, such as a performance model to detect system performance bottle-necks.

2) ***RTL Design and Test Bench Creation***

Once the overall system architecture and partitioning is stable, the detailed design of each ASIC or FPGA can commence. This starts by capturing the design in Verilog at the register transfer level, and capturing a set of test cases in Verilog. These two tasks are complementary, and are sometimes performed by different design teams in isolation to ensure that the specification is correctly interpreted. The RTL Verilog should be synthesizable if automatic logic synthesis is to be used. Test case generation is a major task that requires a disciplined approach and much engineering ingenuity: the quality of the final ASIC or FPGA depends on the coverage of these test cases.

3) ***RTL Verification***

The RTL Verilog is then simulated to validate the functionality against the specification. RTL simulation is usually one or two orders of magnitude faster than gate level simulation, and experience has shown that this speed-up is best exploited by doing more simulation, not spending less time on simulation. In practice it is common to spend 70-80% of the design cycle writing and simulating Verilog at and above the register transfer level, and 20-30% of the time synthesizing and verifying the gates.

4) ***Look-Ahead Synthesis***

Although some exploratory synthesis will be done early on in the design process, to provide accurate speed and area data to aid in the evaluation of architectural decisions and to check the engineer's understanding of how the Verilog will be synthesized, the main synthesis production run is deferred until functional simulation is complete. It is pointless to invest a lot of time and effort in synthesis until the functionality of the design is validated.

Figure 4 : Synthesis using Verilog

Synthesis is the procedure of loading the simulated and verified Verilog code in to a programmable logic structure such as an FPGA or an ASIC in order to verify and check the system created. It is not sufficient that the Verilog is functionally correct; it must be written in such a way that it directs the synthesis tool to generate good hardware. There are currently three kinds of synthesis which are possible such as behavioral synthesis, high level synthesis and RTL synthesis.

Xilinx integrated software environment (ISE) is a software tool developed and produced by Xilinx. This ISE is used for the simulation and analysis of hardware description language(HDL) designs. This ISE provides support for a variety of hardware description languages such as VHDL, Verilog etc. It provides RTL level diagrams of the designs so that even minute details of the design can be verified by the designer. It also allows the developer to synthesize the design onto an FPGA or ASIC. It also allows the designer to perform the timing analysis of the designs. The low-cost Spartan family of FPGAs is fully supported by this edition, as well as the family of CPLDs, meaning small

developers and educational institutions have no overheads from the cost of development software.

As Xilinx ISE is used for design development and implementation the OS requirements are …

Windows: Windows XP,Windows7, Windows 8, Windows 8.1
Linux: Red hat enterprise 4, 5, or 6 and Suse enterprise distributions.

Modelsim is a hardware simulation environment which provides accurate simulations of HDL designs. It also allows the developer to perform debugging easily. It equips the developer to easily change value of signals during testing and development phase. Modelsim is generally used along with Xilinx ISE as a simulator. Modelsim can also provide synthesize of HDL designs onto FPGA's and ASIC's.

VI. CONCLUSION

In the first phase of this project work some important literatures regarding MIMO systems and its implementation using FPGA kits have been studied .An objective for the work to be done has been framed and a block diagram of the proposed MIMO system has been realized. The software tools required for the work has been identified and installed. The hardware equipment's required for the work has also been decided. Xilinx ISE tool is being learned and the work of the convolution encoder has been started. In the future, the aim would be to develop software implementation of the encoder and the complete transmitter section.

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