Analysis of Low-Power and Area-Efficient Shift Registers using Pulsed Latch

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Abstract:
Flip-flops is perilous timing elements in digital circuits which have a huge influence on the circuit speed and power consumption. The performance of flip-flop is an significant element to regulate the efficiency of the entire synchronous circuit.This paper recommends a low-power and area-efficient shift register using pulsed latches. Therefore area and power consumption are reduced by substituting flip-flops with pulsed latches. This technique explains the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals as an alternative of the conventional single pulsed clock signal. Also the shift register uses a small number of the pulsed clock signals by grouping the latches to more than a few sub shifter registers and using supplementary temporary storage latches.

Keywords: *Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.*

I. INTRODUCTION

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size ofCMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers oftransistors onto the same die. The more transistors there will be more switching and more power dissipated in the form ofheat or radiation. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges oflow power design methodologies and practices. Another driver of low power research is the reliability of the integratedcircuit. More switching implies higher average current is expelled and therefore the probability of reliability issuesoccurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profoundtrend continuing and without a match trending in battery life expectancy, the more low power issues will have to beaddressed. The current trends will eventually mandate low power design automation on a very large scale to match thetrends of power consumption of today's and future integrated chips[3]. Power]consumption of Very Large ScaleIntegrated design is given by generalized relation, P = CV2f [1]. Since power is proportional to the square of the voltageas per the relation, voltage scaling is the most prominent way to reduce power dissipation. However, voltage scaling isresults in threshold voltage scaling which bows to the exponential increase in leakage power. Though severalcontributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design thatfurther improves the performance of single edge triggered flip-flops[2].patterns.

The architecture of a shift register is quite simple. An N-bitshift register is composed of series connected N data flip-flops.The speed of the flip-flop is less important than the area andpower consumption because there is no circuit between flip-flipsin the shift register. The smallest flip-flop is suitable for the shiftregister to reduce the area and power consumption. Recently,pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9].But the pulsed latch cannot be used in a shift register due to thetiming problem between pulsed latches

II. CONVENTIONAL EXPLICIT TYPE FLIPFLOPSYSTEMS:

Depending on the method of pulse generation, P-FFdesigns can be classified as implicit and explicit. an implicit-type P-FF, the pulse generator is a builtin logic of the latch design, and no explicit pulsesignals are generated. Generally implicit type PFFs are more power economical than the explicittype P-FFs. But it has a disadvantage of longerdischarging path which leads to inferior timecharacteristics. In an explicit-type P-FF, the designsof pulse generator and latch are separate. In thistype of flip-flops, one pulse generator is shared bygroup of flip-flops so that the circuit complexity isreduced and it has unique speed advantage. Someof the existing explicit type flip-flops are shownbelow.

A. ep-DCO(explicit pulsed data close to output):

It is the basic type of explicit pulse triggered flipflop. It contains a pulse generation circuit of threeinverters connected to the NAND gate and a semidynamic TSPC structure latch design. Back to backconnected inverters are used as keeper device.

Inverters I1 and I2 are used to hold the internalnode X and inverters I3 and I4 are used to latch thedata. It has two stages called static stage anddynamic stage. After the rising edge of the

clockpulse, N2 and N3 will turn on for a small period oftime. During this period, the flip-flop is transparent.

So the input data propagates to the output. Thekeeper logic at node Q is used to maintain theoutput at the same level till the next rising edge [4].

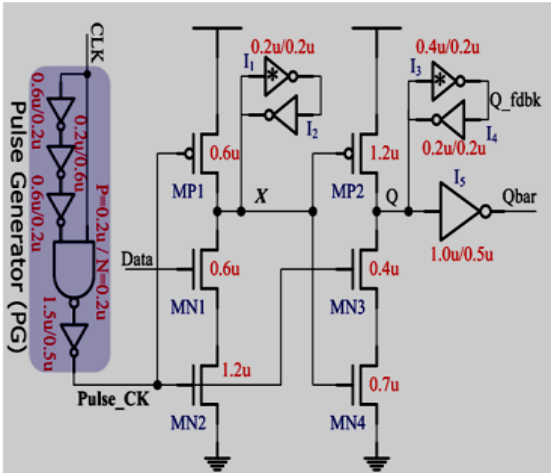


Fig.1: ep-DCO

This design suffers from a serious drawback, i.e.,the internal node X is discharged on every risingedge of the clock in spite of the presence of astatic input "1." This gives rise to large switchingpower dissipation.

B. Conditional Discharge Flip Flop(CDFF):

In order to reduce the redundant switch power, herewe employ a discharge controlled transistor MN3at the discharge path of the first stage [5]. It is usedto feedback the signal Q_fdbk to the input stage, sothat no discharge occurs at static input data „1". Thecircuit is further simplified by replacing the keeperlogic at the internal node X with an inverter and apull up PMOS transistor.

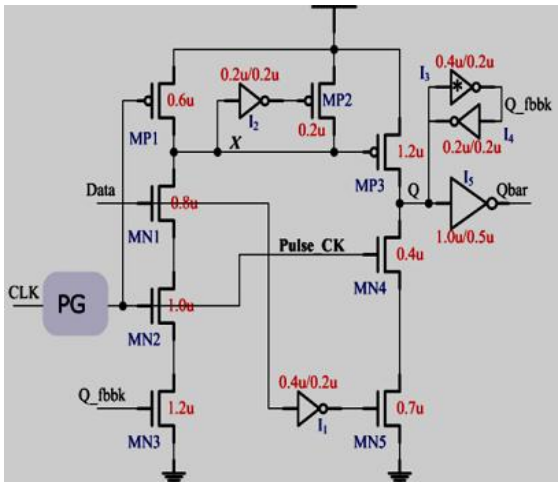


Fig. 2: CDFF

This paper put forward a low-power and area-efficient shift register using pulsed latches. The shift register resolves the timingproblem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. Theshift register uses a small number of the pulsed clock signals bygrouping the latches to several sub shifter registers and usingsupplementary temporary storage latches.

III. PROPOSED ARCHITECTURE:

A master-slave flip-flop using two latches in Fig. 3(a) can bereplaced by a pulsed latch consisting of a latch and a pulsedclock signal in Fig. 3(b)[6]. All pulsed latches share the pulsegeneration circuit for the pulsed clock signal. As a result, thearea and power consumption of the pulsed latch become almosthalf of those of the master-slave flip-flop. The pulsed latch is anattractive solution for small area and low power consumption.

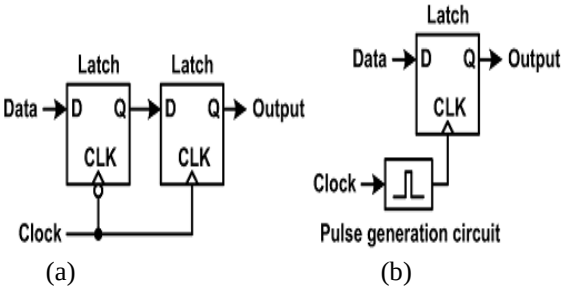


Fig. 3. (a) Master-Slave Flip-Flop. (b) Pulsed Latch.

The pulsed latch cannot be used in shift registers due tothe timing problem, as shown in Fig. 4. The shift register inFig. 4(a) consists of several latches and a pulsed clock signal(CLK_pulse). The operation waveforms in Fig. 4(b) show thetiming problem in the shifter register. The output signal of thefirst latch (Q1) changes correctly because the input signal ofthe first latch (IN) is constant during the clock pulse width (T_{PULSE}). But the second latch has an uncertain output signal(Q2) because its input signal (Q1) changes during the clockpulse width.

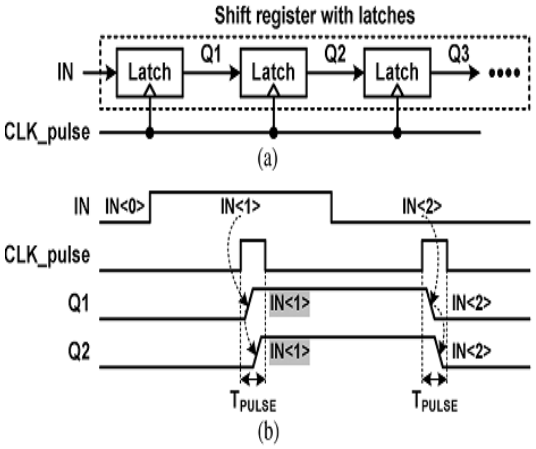


Fig. 4. Shift Register with Latches and a Pulsed Clock signal. (a) Schematic. (b)Waveforms

One solution for the timing problem is to add delay circuitsbetween latches, as shown in Fig. 5(a). The output signal of thelatch is delayed and reaches the next latch after theclock pulse. As shown in Fig. 5(b) the output signals of the firstand second latches (Q1 and Q2) change during the clock pulsewidth , but the input signals of the second and thirdlatches (D2 and D3) become the same as the output signals ofthe first and second latches (Q1 and Q2) after the clock pulse. Asa result, all latches have constant input signals during the clockpulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads.

Fig.6(a) shows an example the proposed shift register. Theproposed shift register is divided into sub shifter registersto reduce the number of delayed pulsed clock signals.

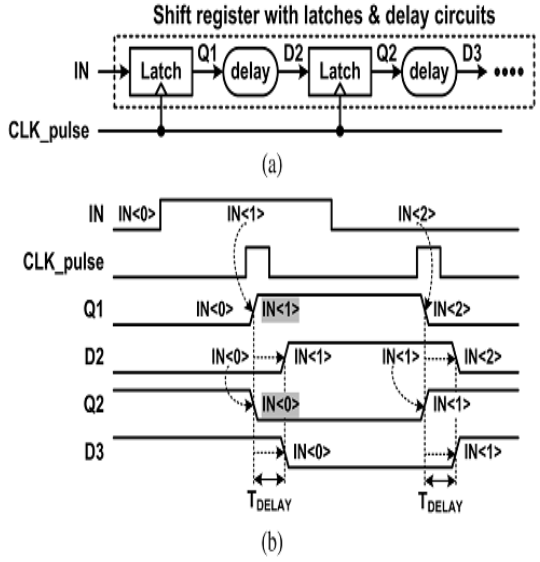
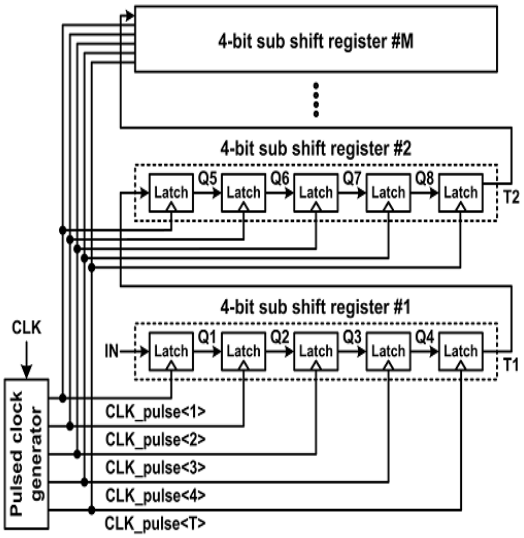
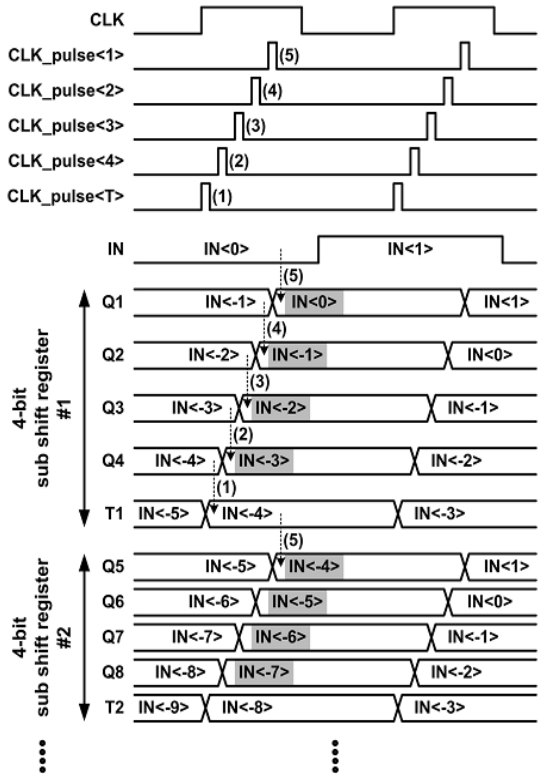


Fig. 5. Shift Register with Latches, Delay Circuits, and a Pulsed Clock Signal. (a)Schematic. (b) Waveforms.

A 4-bitsub shifter register consists of five latches and it performs shiftoperations with five non-overlap delayed pulsed clock signals(CLK_pulse<1:4>and CLK_pulse<T>). In the 4-bit sub shiftregister #1, four latches store 4-bit data (Q1-Q4) and the lastlatch stores 1-bit temporary data (T1) which will be stored inthe first latch (Q5) of the 4-bit sub shift register #2. Fig. 6(b)shows the operation waveforms in the proposed shift register.



(a)



(b)

Fig. 6. Proposed Shift Register. (a) Schematic. (b) Waveforms.

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register .isselected by considering the area, power consumption, speed.

A. *Area Optimization*

The area optimization can be performed as follows. Whenthe circuit areas are normalized with a latch, the areas of a latchand a clock-pulse circuit are 1 and , respectively. The total area becomes$(\alpha_A \times (K+1) + N\left(1+\frac{1}{K}\right)$. The optimal $K(=\sqrt{N/\alpha_A})$for the minimum area is obtained from the first-orderdifferential equation of the total area $(0=\alpha_A - N/K)$.An integer for the minimum area is selected as a divisor of, which is nearest to $\sqrt{N/\alpha_A}$.

B. *Power Optimization*

The power optimization is similar to the area optimization.The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clockloading. When the circuit powers are normalized with a latch,the power consumption of a latch and a clock-pulse circuit are1 and , respectively. The total power consumption is also$(\alpha_p \times (K+1) + N\left(1+\frac{1}{K}\right)$.An integer for the minimumpower is selected as a divisor of , which is nearest to$\sqrt{N/\alpha_p}$.

C. *Chip Implematation:*

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there isno delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting theflip-flop. The proposed shift register uses latches instead of flipflops to reduce the area and power consumption.

IV. CONCLUSION

This paper proposed a low-power and area-efficient shiftregister using pulsed latches. The shift register reduces area andpower consumption by substituting flip-flops with pulsed latches.The timing problem between pulsed latches is solved usingmultiple non-overlap delayed pulsed clock signals as an alternative of asingle pulsed clock signal.

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