Segmentation Based Matrix Code for Communication Channel

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Abstract

The problem of simultaneously broadcasting a common source to multiple receivers over a broadcast channel remains a challenging open problem in network information theory Each receiver is required to partially reconstruct the source sequence by decoding a certain fraction of the source symbols. Our scheme involves splitting the source sequence into multiple segments and applying a systematic erasure code to each such segment. In this project, novel decimal matrix code (DMC) based on divide-symbol is proposed to enhance data reliability with lower delay overhead. The proposed DMC utilizes decimal algorithm to obtain the maximum error detection capability of communication

I. INTRODUCTION

Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Summer is another name for error detection Error correction is the detection of errors and reconstruction of the original, error-free data The general idea for achieving error detection and correction is to add some redundancy (i.e., some extra data) to a message, which receivers can use to check consistency of the delivered message, and to recover data determined to be corrupted. Error-detection and correction schemes can be either systematic or non-systematic: In a systematic scheme, the transmitter sends the original data, and attaches a fixed number of check bits (or parity data), which are derived from the data bits by some deterministic algorithm. If only error detection is required, a receiver can simply apply the same algorithm to the received data bits and compare its output with the received check bits; if the values do not match, an error has occurred at some point during the transmission. In a system that uses a non-systematic code, the original message is transformed into an encoded message that has at least as many bits as the original message.

Related Works:

1) Punctured difference set (PDS) codes have been used to deal with MCUs in memories.
2) Interleaving technique has been used to restrain MCUs, which rearrange cells in the physical arrangement to separate the bits in the same logical word into different physical words.
3) Built-in current sensors (BICS) are proposed to assist with single-error correction and double-error detection codes to provide protection against MCUs
4) 2-D matrix codes (MCs) are proposed to efficiently correct MCUs per word with a low decoding delay, in which one word is divided into multiple rows and multiple columns in logical. The bits per row are protected by Hamming code, while parity code is added in each column.

Existing Drawbacks:

1) PDS codes require more area, power, and delay overheads since the encoding and decoding circuits are more complex in these complicated codes.

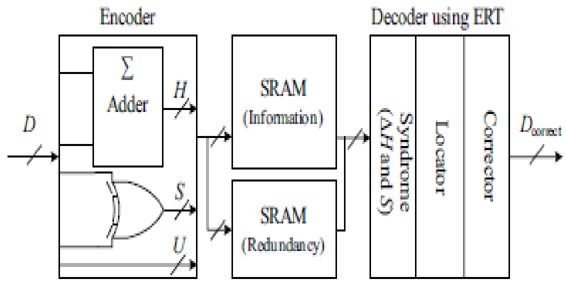
2) Interleaving technique may not be practically used in content-addressable memory (CAM), because of the tight coupling of hardware structures from both cells and comparison circuit structures
3) BICS technique can only correct two errors in a word.
4) 2D MC is capable of correcting only two errors in all cases.

Rateless codes are a popular class of codes that enable efficient communications over multiple unknown erasure channels at the packet level by simultaneously approaching the channel capacity at all erasure rates. Raptor codes, a special class of rateless codes, also have very low encoding and decoding complexity [3]. Because of these properties, Raptor codes have been standardized for Multimedia Broadcast/Multicast Service (MBMS) and are being deployed in applications such as LTE eMBMS. Raptor codes are essentially optimal for multicast over erasure channels where all receivers require identical content

II. PROPOSED SYSTEM

In this project, novel decimal matrix code (DMC) based on divide-symbol is proposed to provide enhanced memory reliability. The proposed DMC utilizes decimal algorithm (decimal integer addition and decimal integer subtraction) to detect errors. The advantage of using decimal algorithm is that the error detection capability is maximized so that the reliability of memory is enhanced. Besides, the encoder-reuse technique (ERT) is proposed to minimize the area overhead of extra circuits (encoder and decoder) without disturbing the whole encoding and decoding processes, because ERT uses DMC encoder itself to be part of the decoder.

Proposed architecture:



III. EXPERIMENTAL RESULTS

The proposed are simulated by using Xilinx ISE 12.1i and implemented in Virtex-5 FPGA processor. The experimental results are given in Table 1

S.NO	PARAMETER	USED
1	NUMBER OF SLICES	129
2	IOB'S	40
3	LUT'S	235

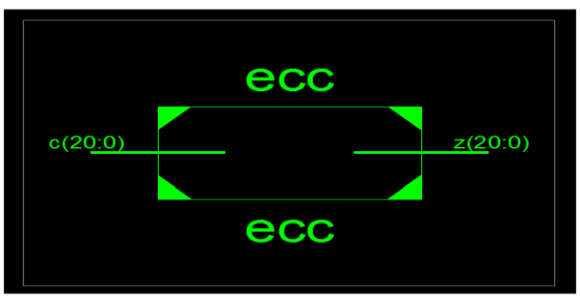


Fig. 2. Technology Schematic

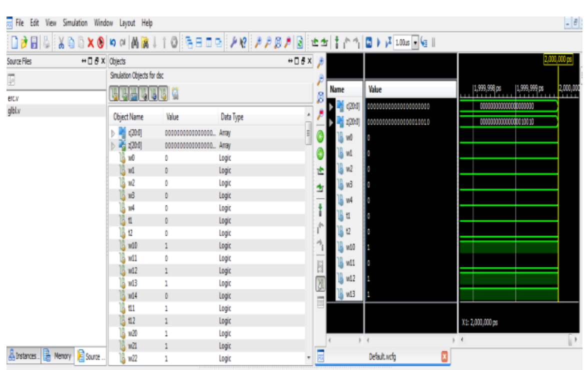


Fig. 3. Result without Error

IV. SIMULATION RESULTS

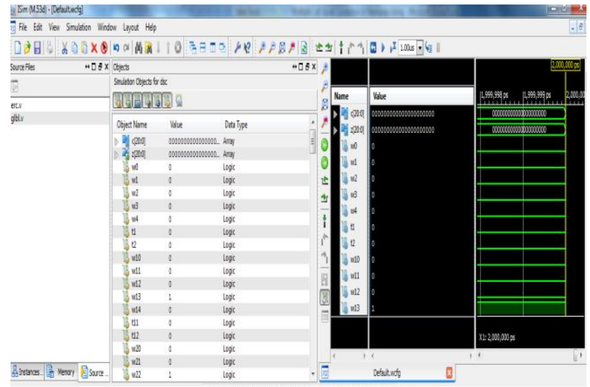


Fig. 4. Result with Error

Fig 3 and 4 shows the result of 21 bit decoder with more than and less than three errors The equation in which the errors are inserted is selected randomly. The bit positions on which the errors are inserted are then randomly selected These results indicate that the implementation of the proposed scheme is feasible at an acceptable cost and performance Conclusion In this paper, we proposed a successive segmentation-based matrix coding scheme for broadcasting a binary source over a multi receiver erasure broadcast channel. Each receiver has individual distortion constraints and experiences distinct channel erasure rates. The proposed scheme partitions the source sequence into multiple segments and applies a systematic erasure code to each segment. We provided optimal choices for segment sizes and code rates for each segment, which were based on the users' channel erasure rates, and distortion constraints. Not only does this proposed scheme outperform Raptor and network coding, it also has two other practical advantages, namely simplicity and scalability

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