QCA Design of Encoder for Low Power Memory Applications

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Abstract

A decoder is important component of memory, for address decoding and encoding. The size of Complementary Metal Oxide Semiconductor (CMOS) transistor keeps shrinking to increase the density on chip in accordance with Moore's Law. The scaling affects the device performance due to constraints like heat dissipation and power consumption. A Quantum dot Cellular Automata (QCA) is an alternative to CMOS.QCA offers higher speed, lower power consumption and higher density. In non reversible gates some amount of power loss is involved. Interest in reversible logic offers reduced heat dissipation and increases the speed. It is a new transistor-less computation in nanotechnology. In this project propose a reversible gate based decoder architecture. It provides reversibility and area minimization. QCA designer tool has been used to validate the performance of reversible decoders.

I. INTRODUCTION

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. Investigations of low-power logic styles reported in the literature so far, however, have mainly focused on particular logic cells, namely full-adders, used in some arithmetic circuits.

VLSI fabrication process keep on shrinking the physical sizes down to atomic scale dimensions and the operational frequencies of terahertz can be easily obtained if the devices can operate with less no. of electrons. However, there is a need for a trade-off to be made between increasing requirements of performance parameters and the feature size. The eventual saturation of CMOS technology is not due to inability to reduce its physical size further, but the detrimental effects of quantum mechanical effects on tiny transistors. for e.g., In nanoscale transistors, impermissible amounts of current leaks due to such highly narrow channels and ultra thin insulating layers.

Nanotechnology is one of the possible alternatives to the stated trade off problem. ITRS report summarized several possible solutions. The possible variants are i) Deltt (double–electron-layer tunneling transistor) developed by scholars at SN labs, ii) SET (single electron transistors) iii) rapid single quantum flux logic, iv0 quantum cellular automata. SET's are a promising technology for non volatile memory.

To the best of our knowledge, the concurrent testing of faults in QCA and QCA-based sequential circuits has not been addressed in the literature. In this paper, we propose novel designs for concurrently testable latches for molecular QCA using conservative reversible logic. Reversible computation in a system can be performed only when the system comprises reversible gates. Reversible circuits do not lose information, and can generate unique output vector from each input vector and *vice versa* (i.e., there is a one-to-one mapping between the input and the output vectors). Landauer has shown that for irreversible logic computations, each bit of information lost generates kT ln 2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed. Bennett showed that kT ln 2 energy dissipation would not occur if a computation is carried out in a reversible way.

In this paper an effective approach to analysis and design of priority encoder with reversible NAND gate using quantum dot cellular automata is explored in nanoscale. This paper we use the majority gates is the fundamental component of the QCA circuit implementation. The proposed encoder circuit is designed and simulated using quantum dot cellular automata designer tool and also this simulator tool is more useful for building a complex priority encoder input levels. The proposed structure of encoder required only less number of majority gate functions compared to previous structures.

II. RELATED WORKS

In previous, a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed, by using mixed-logic 2-4 predecoders combined with standard CMOS post-decoder. All proposed decoders have full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Adopting this design methodology, and with respect to the theory presented on section II, we implemented four 4-16 decoders by using the four new 2-4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are: 4-16LP (Fig. 1(a)), which combines two 2-4LPI predecoders with a NOR-based post-decoder, 4-16HP (Fig. 1(b)), which combines two 2-4HPI predecoders with a NOR-based post-decoder, 4-16LPI (Fig. 1(c)), which combines two 2-4LP predecoders with a NAND-based post-decoder and, finally, 4-16HPI (Fig. 1(d)), which combines two 2-4HP predecoders with a NAND-based post-decoder.

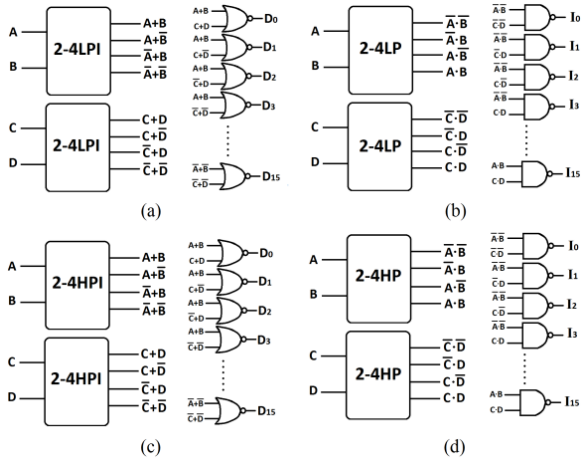

Fig.1. 4-16 Line Decoders

With continuous sub-micron scaling, especially at low voltage operation, leakage power consumption has become increasingly important as it dominates the dynamic one [12]. In our analysis, both leakage and active currents are considered. The total power dissipation (static+dynamic) is extracted from spice simulation and given in nanowatts (nW). Regarding the delay, we note the highest value that occurs among all transitions and outputs in each case, given in picoseconds (ps). The power-delay product (PDP) measures the energy per operation/switching event.

Here one of the main problems in CMOS is quantum tunnelling through insulators, causing leakage currents that increase power consumption. New technologies arising, have their working principles based on quantum effects, so these are no longer a problem, but a required feature instead. Therefore alternative technologies are under development. The design of current trend is strongly influenced by the fact that transistor and featured size have continuously influenced, while density and frequency have increased. If a new technology is to be created for devices of nanometer scale, new design principles are necessary. One promising approach is to move to a transistor-less cellular architecture based on interacting quantum dots named Quantum-dot Cellular Automata.

III. PROPOSED METHOD

Here an effective approach to analysis and design of priority encoder with reversible NAND gate using quantum dot cellular automata is explored in nanoscale. This paper we use the majority gates is the fundamental component of the QCA circuit implementation. The proposed circuit is designed and simulated using quantum dot cellular automata designer tool and also this simulator tool is more useful for building a complex input levels. The proposed structure required only less number of majority gate functions compared to previous structures.

The "loss of information" associated with an irreversible process is usually expressed in terms of a quantity called (information theoretic) entropy. Briefly, let p~ be the probability of state i in a given state distribution. Then the information-theoretic entropy of this distribution is -*E*i *pi* log *pi*. If the logarithm is taken in base 2, then the entropy is said to be measured in bits. For example, assuming equal probabilities for all possible values of the argument, the evaluation of the NAND function entails a decrease in entropy of approximately 1.189 bits, while the complete erasure of one binary argument (such as given by the function {O→O, l→O}) entails a decrease of exactly 1 bit. Note that information theoretic entropy is in general a much more richly endowed function than thermodynamic entropy (Baierlein, 1971); in the present situation, however, the two quantities can be identified-the conversion factor being given by the relation 1bit=*k* ln2.

IV. EXPERIMENTAL RESULTS

The proposed has been designed and simulated report can be obtained by using QCA Designer tool. The various parameters used for computing existing

and proposed systems are given in the table1 and also the schematic design for the proposed shown in fig.4

s.no	Parameter	Method In [5]	Proposed
1	No of cells	183	174

Table1: comparison Result of Existing and Proposed

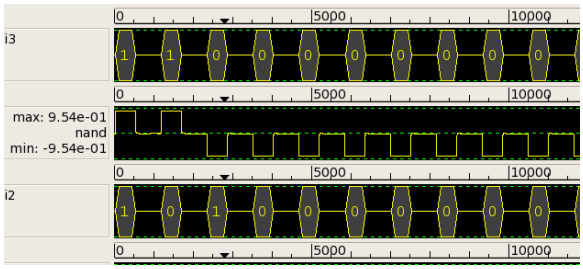

Fig.4 Simulation Results

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction in time and area based on the majority gates results which have been done by using QCA designer. The proposed algorithm significantly reduces area consumption when compared to the existing system(in fig.5).

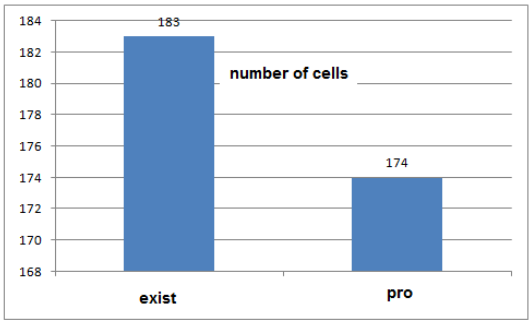

Fig.5 Comparison Chart

VI. CONCLUSION

The design under consideration, i,e reversible decoder is said to be an area effective when designed with QCA rather than CMOS. As there is an advantage of both low area and power at the same abstraction level, QCA can be seen as one of the promising technologies in near future. However there is still research going on in the inter disciplines of physical implementations and cost effective manufacturing process.High speed decoder is the essential components in fast SRAM. The work can be extended to design a SRAM which will be highly delay efficient design.

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