Review Paper on Reduced Power Consumption using Flip Flop

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Abstract:- In this review paper, we are discussing about the idea to minimize the power dissipation and area minimization using flip flops. The flip flop or latch in the circuit that has two stable states and can be used to store state information. A flip flop is a bi-stable multi vibrator. The circuit can be made to change state by signals applied to one or more control input and will have one or more output. As, the biggest challenge for Industry is to reduce power consumption and area minimization. So we have introduced the brief idea of using multi bit flip flop (using D flip flop) and dynamic D flip flop.

Keywords: - Flip flop, clock pulse trigger , power supply, multi bit flip flop, wire length.

I.INTRODUCTION

Over electronics, An flip-flop might be used to store state majority of the data. The circlet could a chance to be made with change state toward signs connected will particular case or more control inputs also will bring you quit offering on that one or two outputs. An flip flop may be an bi-stable multi-vibrator. It saves absolute bit from claiming information. Flip flop could be basic or clocked. It may be a parallel stockpiling contraption. It could store whichever 0 alternately 1 which is twofold spot. It meets expectations once two unfaltering states secondary and low i.e. 1 and 0. A flip-flop could control flags that includes an clock indicator which is typically regulated toward control flags. Those flip flop will be used to store data for odds. They include a chance to be used to stay with those rope or what estimation of variable (information, yield alternately white collar of the road). In those convenience of an propelled circlet i.e. Transform the operation of a circlet relying upon those state.

Different sorts from claiming flip-flop would there:-.

1. S-R flip-flop.

2. D flip flop.

3. J-K flip flop.

4. T flip flop.

The d flip-flop is broadly utilized. It may be otherwise called an information or delay flip-flop.

II .D FLIP FLOP

The D (delay) flip flop has only one input called the delay (D) input and two outputs 0 and 1. It can be constructed from an S-R flip flop by inserting an inverter between S and R and assigning the symbol D to the S input .The structure of D flip flop is shown in figure Basically, it consists of a NAND flip flop with a gating arrangement on its output.

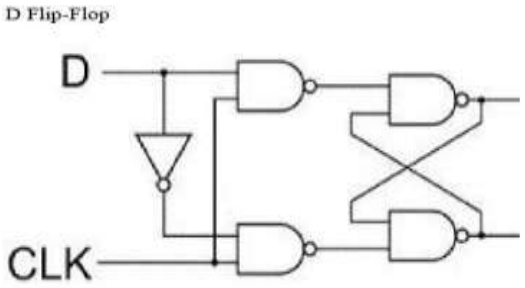

Figure 1: D Flip Flop

Those d flip-flop captures the quality of the D-input toward a positive part of the clock cycle

(such Concerning illustration those climbing edge of the clock). That caught quality turns into the Q yield. In other times, the yield Q doesn't progress. The d flip-flop can be seen as a memory cell, or a zero-order hold,

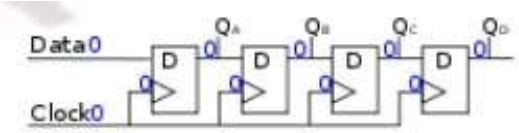

Figure 2: Shift register using D Flip Flop

The greater part D-type flip-flops to ICs bring those ability on a chance to be constrained of the set or reset state (which Disregards the d What's more clock inputs), a great deal like an S-R flip-flop. Usually, the illicit S=R = 1 state will be determined done D-type flip-flops. Toward setting S=R = 0, the flip-flop might be utilized Concerning illustration portrayed over.

III.MULTI BIT FLIP-FLOP

When a common clock is shared by the several flip-flops the k-bit flip-flop becomes k-bit multi bit flip-flop. The use of common clock may reduce the power consumption.

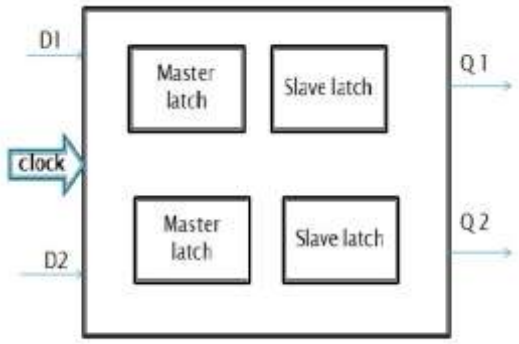

Figure 3: 2 bit flip flop[4]

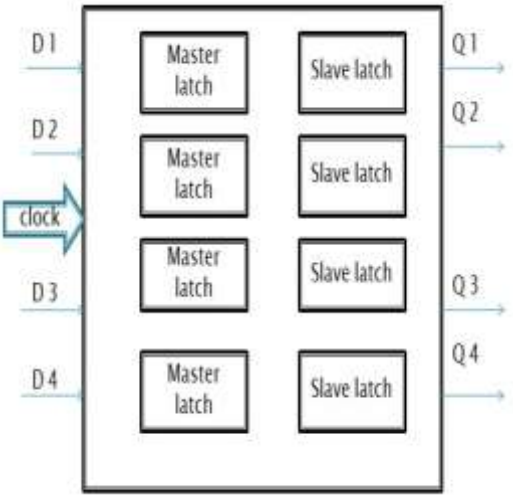

Figure 4: 4 bit flip flop[4]

A. Merge of flip-flop:

This plan stream could be harshly partitioned under three phases. In the beginning, we must identify an lawful placement district for each flip-flop .In those attainable placement areas of a flip-flop connected with diverse pins would discovered in view of those timing imperatives characterized on the pins. Afterward those lawful placement area of the flip-flop, a chance to be got toward those overlapped territory about these locales.

Therefore, the overlapped range might be recognized that's only the tip of the iceberg effortlessly whether we could convert those coordinate framework about phones on get rectangular locales. In the second stage, we might want will Fabricate an mix table, which characterizes constantly on could reasonably be expected combinations for flip-flops in place on get another multi-bit flip-flop Gave toward the library.

The flip-flops might be consolidated with those help of the table. Following those legitimate placement areas about flip-flops are found and the consolidation table will be built, we could use them with blend flip-flops. On accelerate our program, we will gap a chip under a few bins Also blend flip-flops over a neighbour hood receptacle. However, those flip-flops in distinctive bins might a chance to be mergeable.

Thus, we must consolidate a few bins under An bigger receptacle What's more repeatable this step until no flip-flop might be consolidated any longer

Table 1: Performance Comparison

Flip-flop	Power consumption using single bit flip-flop	Power consumption using multi bit flip-flop
1 bit flip flop	0.52	0.52
2 bit flip flop	1.04	0.52
4 bit flip flop	2.08	0.52
8 bit flip flop	4.16	0.52

B. Operation on flip flop:

1. Start
2. Identify the mergeable flip-flop
3. Build a combination table
4. Merge flip-flop
5. End

Conventional dynamic D Flip Flop:

Progressive or clocked rationale entryways are used to diminish circlet complexity, expanded working speed Furthermore easier control dispersal from claiming Different circlet strategies. A true single phase clock (TSPC) progressive CMOS circuits worked for particular case clock sign that is never altered. Therefore, no clock skew exits but to clock delay issues.

[2] By using the Transistor switching logic only we are designing this circuit so it will be consuming only less power when compared to all other circuits.
And in addition we are hosting best 8 transistors including those not entryways also. Something like that we will be hosting much diminished control So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also..

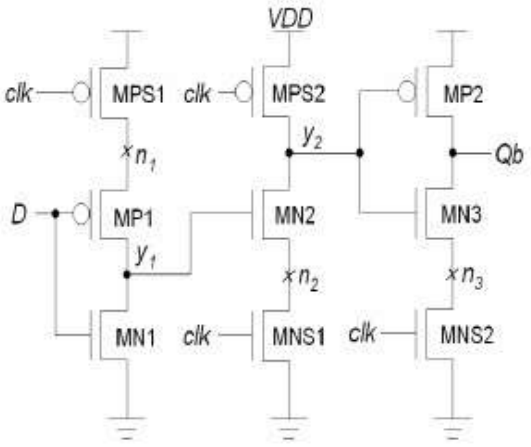

Figure 5: Operation of the conventional dynamic D Flip- Flop

Thus; we are reducing the overall switching delay and power

V.RESULTS AND DISCUSSIONS

[3]The point when clk =1. Assuming that D=0 What's more clk =0, MPS1, MP1 Also MPS2 are turned on and n1, y1 What's more y2 get secondary. If the single clk changes low to high , the node y2 is discharged to low through MN2 and MNS1,making MP2 be on and Qb high.

The case with clk change low to high and D=0 making MP2 be on and Qb high and .Figure 5 shows the case with clk changes low to high and D=1 making Qb be low.

The dissection is the robust lines when clk =1. In D=0 Also clk =0,MPS1,MP1 What's more MPS2 need aid turned on Furthermore n1,y1 What's more y2 turned on If those solitary clk transforms low with secondary ,the node y2 is released should low through MN2 What's more MNS1,making MP2 be on Also Qb helter skelter.

If the single clk changes low to high ,the node y2 is discharged to low through MN2 and MNS1,making MP2 be on and Qb high.

The case with clk change low to high and D=0 making MP2 be on and Qb high and The case with clk changes low to high and D=1 making Qb be low.

VI. APPLICATIONS OF FLIP FLOP

1.Data Storage:

[1] A flip flop store one bit at a time in digital circuit. In order to store more than one bit flip flop can be connected in series and parallel called registers. Register is simply a data storage device for a number of bits in which each flip flop store one bit of information (0 or 1). Thus a 4 bit register consists of 4 individual flip flops, each able to store one bit of information at a time.

2. Data Transfer:

Flip flops can also be used extensively to transfer the data. For this purpose shift register is used. A shift register is a register which is able to shift or transfer it. It may be designed to shift or transfer data either left or right. The shift register is used for multiplication and division where shifting is required. The shift register can be built using RS, JK or D flip flops.

VII. Conclusion

This whole research paper consumption by using multi bit flip-flop. It include the application of multi bit flip-flop in an 8 bit adder. The flip flop circuits can be changed its state by our convience. That the use of multi bit flip-flops can achieve power reduction. Power reduction reduces the chip area of the total power consumption. Its application is mostly oriented in power and delay. The future scope of flip flop is to reduce the leakage reduction using transistor. For the system which have high frequency performance have certain power consumption. And are designed for the semi dynamic ,hybrid interest.

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