Design of a 3-T Half Adder

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Abstract:

In this paper, we propose a new technique for implementing a half adder circuit consisting of minimum number of transistors (3-T). The W/L ratio is varied to get the required output. An adder is a digital circuit that performs addition of two numbers. In many computers and other kind of processors, adders are used not only in arithmetic logic unit but also in other parts of the processors where they are used to calculate addresses, table indices and similar operations. Simulated results indicate the performance of proposed half adder over the conventional half adders. Detailed comparison of the simulated results is presented here which is done in MultiSim software.

Keywords: *Pass Transistor Logic, 3-T XOR, Logical Effort and Transistor Sizing*

I. INTRODUCTION

Since the introduction of integrated circuits decades ago methods to speed up digital circuits and to reduce the area of their designs have great importance. The power dissipation per unit area grows as the number of transistors per chip increases which also increases the chip temperature. This excessive temperature reduces the reliability and lifetime of the circuit**.**

The CMOS technology has a great influence in the performance of microprocessors. Dynamic CMOS circuits are used in microprocessors to improve their timing performance. This method has many challenges like transistor sizing, charge sharing, noise-immunity, leakage current etc.

The growing world demands for circuits with ultra-low power dissipation. The presence of complementary transistors avoids contention. It ensures that if the inputs are not changing then there is no power dissipation. Here the output voltage level is connected to the power or ground line or both.

Various techniques have been implemented to reduce power dissipation at circuit, architectural and system level. The number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so power dissipation rises and heat removal becomes difficult and expensive. The proposed thesis is to develop a hybrid VLSI circuit that improves the circuit performance by reducing the number of transistors. The output of the gate can be improved by changing the W/L ratio of the transistor. The points to be noted while changing the W/L ratio:

1. As W/L ratio increases the drain-to source current increases.
2. As W/L ratio increases the response time increases.
3. W/L ratio is roughly proportional to the resistance.
4. The W/L ratio of PMOS should be larger than the NMOS.
5. Make the MOSFET in the output side the largest.

Logical effort is a method to make certain decisions:

1. Uses a simple model of delay.
2. Allows back of the envelope calculations.
3. Helps make rapid comparison between comparatives.
4. Emphasises remarkable symmetries.

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In modern computers adders reside in Arithmetic logic unit (ALU) where other operations are performed. Although adders can be constructed for many numerical representations, such as Binary coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or one's complement is being used to represent negative numbers, it is trivial to modify an adder into an adder-subtractor. Other signed number representations require a more complex adder.

In [1] the authors have designed a low power high speed multiplier using full adder consisting of minimum no. of transistors in which they modified the blocks AND gate and the XOR gate the idea behind this work is utilized here. Recently many techniques have been proposed with the objective of improving speed and power consumption [2], [3].

Paper is organized as follows. Section II describes the related work. Section III describes the proposed system. Section IV shows the simulation results.

II. RELATED WORK

Half adder is a combinational arithmetic circuit. A half adder adds two one-bit binary

numbers A and B. The input variables of a half adder are called the augend and addend bits. It has two outputs, S and C which is the sum and carry respectively. Carry is the output which is carried into the next stages. The simplest half adder design pictured incorporates an XOR gate for S and an AND gate for C. If A and B are the input bits, the sum bit(S) is the X-OR of A and B and the carry bit(C) will be the AND of A and B. Half adder is the simplest of all circuit. The inputs to the XOR gates are also inputs to the AND gate. The input "wires" to the XOR gate are tied to the input wires of AND gate. Thus, when voltage is applied to the A input of the XOR gate, the A input to the AND gate receives the same voltage. The Half adder can add only two bits so if input to a half adder have a carry then it will be neglected and adds only the A and B bits which means that the binary addition process is not complete and that's why it is called a Half adder.

0+0 = Sum 0 Carry 0
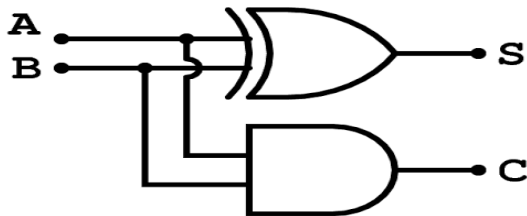0+1 = Sum 1 Carry 0
1+0 = Sum 1 Carry 0
1+1 = Sum 0 Carry 1

Figure 1: Block Diagram of Half Adder

Table 1: Truth Table of Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The previous work presents adder circuits using pass transistor logic based MUX & XOR gate, which contains lesser no. of transistors. The pass transistor logic reduces the count of transistors used to make different logic circuits, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit voltage[4]. This reduces the number of active devices, but has the disadvantage that output levels can be no higher than the input level. Each transistor in series has a lower voltage at its output than at its input [5]. For proper operation, design [6].
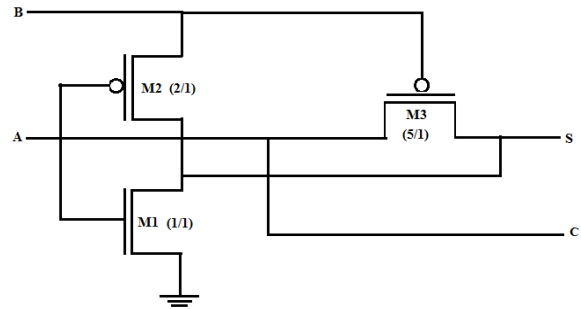

Figure 3:3-T XOR

Pass transistor logic has become important for the design of low-power high-performance digital circuits due to the smaller node capacitances and reduced transistors count it offers. The 5-T half adder was designed using this 3-T XOR and 2-T AND gate.
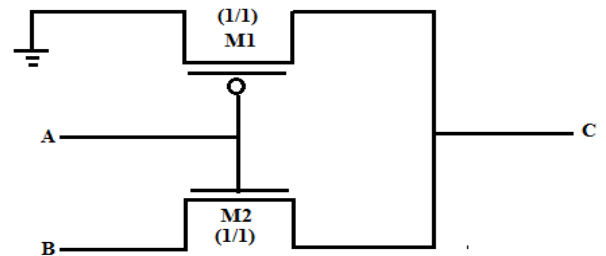

Figure 4:2-T MUX

A 2-T MUX is used as an AND gate. The input A is given to the select line. The output depends on the value given to A. When A=0 output is 0 since the MUX is off. When A=1 the value given to B is obtained as output. Hence the conditions for AND gate is satisfied.

Table 2: Truth Table of AND Gate

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

III. PROPOSED SYSTEM

The three major sources of power dissipation in a digital CMOS circuit are logic transition, short-circuit current and leakage current. The short-circuit current is the direct current passing through the supply and the ground, when both the NMOS and the PMOS transistors are simultaneously active. The proposed half adder is of 3Twhich is a variation from the existing half adder. The XOR gate itself can be used as a half adder. In the figure below the transistors M1 and M2 forms an inverter circuit.The CMOS inverter output is at high impedance when input B is at logic low and when B

is at logic high the inverter acts like a normal inverter .when input B is at logic low the pass transistor M3 is enabled and the output S gets the same logic value as input A. Now when A=1 and B=0, due to threshold drop voltage degradation occurs across transistor M3 and consequently the output S is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3. The desired output is obtained by varying the W/L ratio. The sum is obtained from the M3 transistor and Carry is obtained across its drain and source.

Since the proposed circuit has only 3 transistors it reduces the chip area and thereby reduces power consumption.
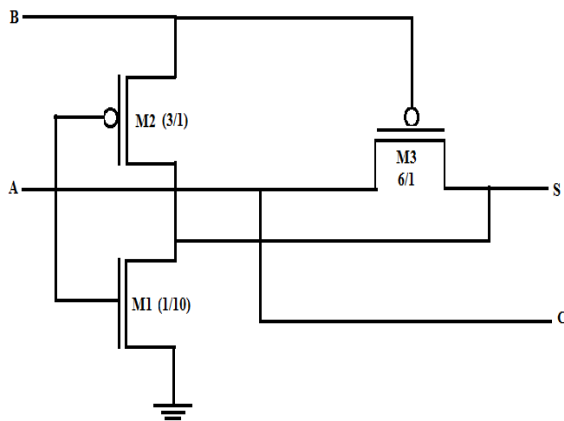

Figure 5:3-T Half Adder

IV. EXPERIMENTAL RESULTS

Figures show the simulation results of the proposed half adder. Simulation is done in Multisim software. The connections are made as in the circuit. A 5V represents logic 1 and a 0V represents logic 0.The two inputs are A: (S1), B:(S2).The output of the half adder the sum(S) and the carry(C) is connected to the oscilloscope. The red line represents the sum and pink line represents the carry in the graph. Figure 6, figure 7, figure 8, figure 9 shows the graph for various input combinations 00,01,10,11 respectively and Table 2 shows the output values of these input combinations. From the table it is clear that the proposed half adder shows a result which is more feasible compared to a conventional half adder.
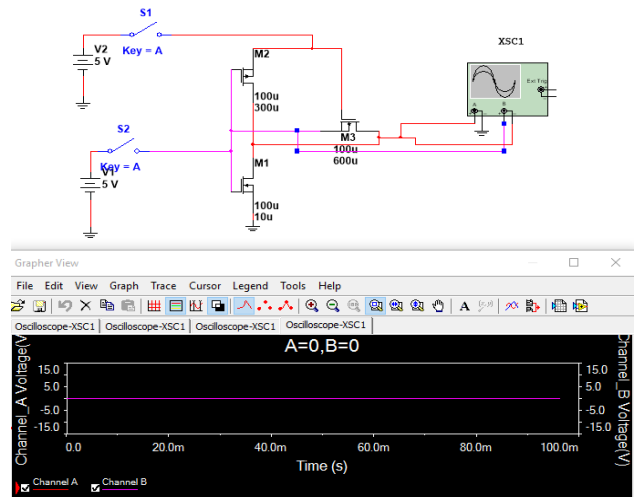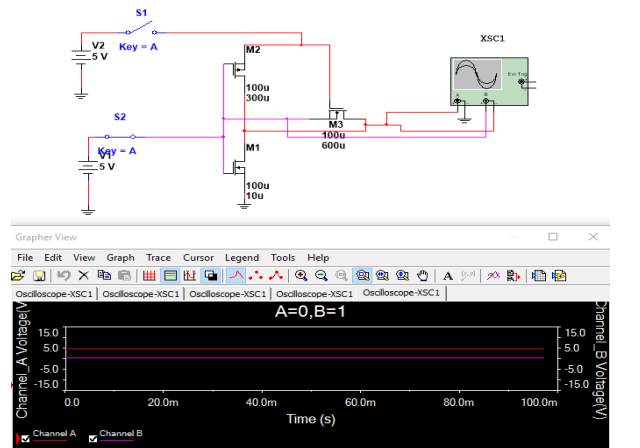

Figure 6: 3-T Half Adder (A=0,B=0V)

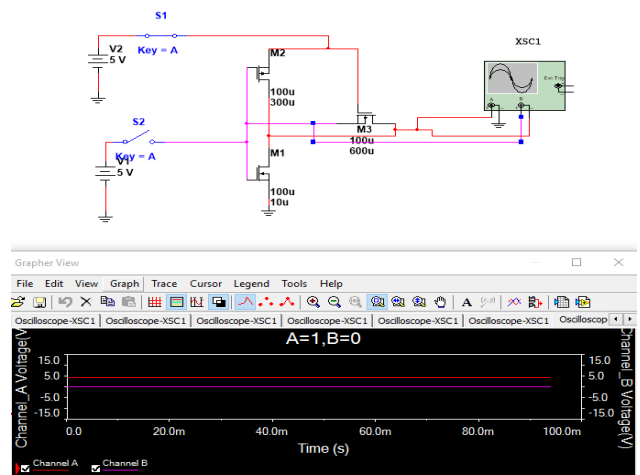**Figure 7: 3-T Half Adder (A=0,B=5V)**

Figure 8: 3-T Half Adder (A=5,B=0V)

Figure 9:3-T Half Adder (A=5,B=5V)

Table 3: Output of Conventional and Proposed Half Adder

Combinations	5-T Half Adder		3-T Half Adder	
	Sum	Carry	Sum	Carry
00	0V	0 V	0 V	0 V
01	3.07 V	1.366 V	4.49 V	504.73mV
10	3.09 V	-174.82mV	4.37 V	-155.41mV
11	100 nV	4.99 V	1.0uV	4.96 V

V. CONCLUSION

A 3-T half adder by varying the W/L ratio to obtain the desired output has been implemented. The proposed circuit can be used where low power consumption is an essential requirement like in design of high-speed embedded processors. A reduction in power consumption provides several benefits. As a future scope of the work, Power of circuit can be further reduced by sizing the transistor keeping logical effort in mind.

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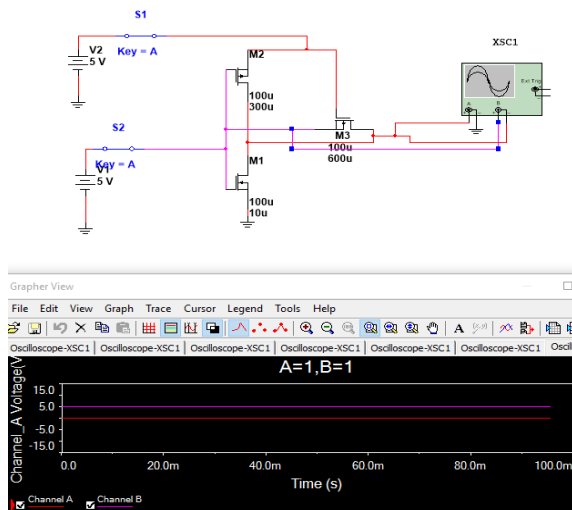
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