An Analysis of Device Characteristics of Strained N-Channel MOSFET

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Abstract *– Large effects of strain on the electrical resistance of silicon were exposed not long after the recognition of silicon as the material for the growth of solid state electronics. As we are approaching to Nano scale, the CMOS applications, device dimensions are getting their scaling limit and it is affecting the gate leakage current, drain induced barrier lowering (DIBL) etc. to a rise. It also worsening the required characteristics and performance of the devices. To overcome this some significant changes in device structures and materials will be needed for continued transistor miniaturization and equivalent performance improvements. This paper is a comparison of performances of unstrained MOSFET with performances of n-channel planer MOSFET with introduction of strain into it, for different channel lengths and its simulation with ATLAS, a 2D device simulator from Silvaco Inc.*

Keywords *– Nano scale strained-Si/SiGe MOSFET, short channeleffects, simulation, threshold voltage, DIBL, CMOS etc.*

I. INTRODUCTION

Strained-silicon devices have been receiving enormous attention owing to their potential for achieving higher channel mobility and drive current enhancement and compatibility with conventional silicon processing. Strain improves MOSFET drive currents by fundamentally altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths. Here, the variation in device characteristics of n-channel strained MOSFET is provided, while changing the parameter like channel length and Ge content. The results of the simulation verifies the enhanced drain current after introducing strain and by decreasing channel length. The presence of strain is due to presence of silicon-germanium layer placed just below the channel region of MOSFET. With this underlying layer of silicon germanium in a strained n-channel MOSFET, its comparison is done with unstrained MOSFET, with the I_d-V_g curves. Along with comparison of curves, comparative analysis of strained planner MOSFET with varying channel length is also done. Effect of strain is analysed by varying the mole fraction of Ge in relaxed $Si_{1-x}Ge_x$ layer from 0.0 to 0.4, with respective change in material property like mobility, energy gap, density of states, changes in I_d-V_g curve and the shift in threshold voltage from the curve is calculated.

II. STRAIN

To maintain a lower junction electric field in horizontal path between drain and source in the channel region, and non-overlap of the source and drain depletion in the channel need of high doping develops authoritative. But a serious effect of mobility deprivation due to the impurity scattering arises in picture with higher amount of channel doping. The mobility of the charge carriers is enhanced through a concept known as the strain technology.

A. Physics of Strain

When a layer of a crystal is grown over another layer, a strain is settled in the upper layer due to the mismatch of the lattice constants of the two layers. This is used to accomplish the high speeds without scaling down the devices. In order to achieve the biaxial strain in the Si channel a $Si_{1-x}Ge_x$ virtual substrate is castoff. Here is germanium is elected because of its compatibility with the Si technology

and its somewhat larger lattice constant. The lattice constant of both material is given below:

Silicon = 5.431 Å

Germanium = 5.657 Å

Epitaxial growth of Si on relaxed SiGe substrate fallouts in strained-Si layers due to the larger lattice constants of Ge. When a layer of $Si_{1-x}Ge_x$ is placed by epitaxial growth on top of a bulk Si wafer. The atoms of Si Ge substrate will firstly line up with the Si wafer and be under compressive strain and as the depth of the $Si_{1-x}Ge_x$ layer increases it will begin to relax.

B. Effect of Strain

A silicon thin film developed pseudo-morphically over a calm $Si_{1-x}Ge_x$substrate understandings biaxial tension foremost to changes in band structure [9], [13]. Owed to strain, the electron fellow feeling (affinity) of silicon rises and the band gap drops. Also, the effective mass of carriers drops. The effect of strain on Si band structure can be displayed as [9], [11], [13]

$$(\Delta E_C)_{s-Si} = 0.57x, \left(\Delta E_g\right)_{s-Si} = 0.4x$$

$$V_T ln\left(\frac{N_{V,Si}}{N_{v,s-Si}}\right) = V_T ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{3/2} \approx 0.075x \quad (1)$$

Where x is the Ge mole part in $Si_{1-x}Ge_x$substrate, $(\Delta E_C)_{s-Si}$ is the rise in electron fellow feeling of silicon due to strain, $(\Delta E_g)_{s-Si}$ is the reduction in band gap of silicon due to strain, V_T is the thermal voltage, $N_{V,Si}$ and $N_{V,s-Si}$ are the density of states (DOS) in the valence band in normal and strained silicon, singly, $m^*_{h,Si}$and $m^*_{h,s-Si}$are the hole DOS effective masses in normal and strained silicon, respectively. The band structure parameters for relaxed $Si_{1-x}Ge_x$ substrate can also be estimated as [9],[11] ,[14]

$$\left(\Delta E_g\right)_{SiGe} = 0.467x$$

$$N_{V,SiGe} = \left(0.6x + 1.04(1-x)\right)X10^{19}cm^{-3}$$

$$\varepsilon_{SiGe} = 11.8 + 4.2x \quad (2)$$

Where $(\Delta E_g)_{SiGe}$is the fall in band gap of $Si_{1-x}Ge_x$from that of Si, $N_{V,SiGe}$ is the DOS in the valence band in relaxed $Si_{1-x}Ge_x$, and ε_{SiGe} is the permittivity of $Si_{1-x}Ge_x$. The flatband voltage of a MOSFET is thus altered due to strain as [9]

$$\left(V_{FB,f}\right)_{s-Si} = \left(V_{FB,f}\right)_{Si} + \Delta V_{FB,f} \quad (3)$$

Where

$$\left(V_{FB,f}\right)_{Si} = \emptyset_M - \emptyset_{Si}$$

$$\Delta V_{Fb,f} = \frac{-(\Delta E_C)_{s-Si}}{q} + \frac{\left(\Delta E_g\right)_{s-Si}}{q} - V_T ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \quad (4)$$

$$\emptyset_{Si} = \frac{x_{Si}}{q} + \frac{E_{g,Si}}{2q} + \emptyset_{F,Si}$$

$$\emptyset_{F,Si} = V_T ln\left(\frac{N_A}{n_{i,Si}}\right) \quad (5)$$

In the beyond dealings, $\varphi_M$is the gate work function, φ_{Si} is the unstrained Si work function, $\varphi_{F,Si}$ is the Fermi potential in unstrained Si, χ_{Si} is the electron fellow feeling in unstrained Si, $E_{g,Si}$ is the band gap in unstrained Si, q is the electronic charge, N_A is the body doping concentration and $n_{i,Si}$ is the intrinsic carrier concentration in unstrained Si. The built-in voltage across the source-body and drain-body junctions in the strained-Si thin film is also exaggerated by strain as

$$V_{bi,s-Si} = V_{bi,Si} + (\Delta V_{bi})_{s-Si} \quad (6)$$

Where,

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \emptyset_{F,Si}$$

$$(\Delta V_{bi})_{s-Si} = \frac{-\left(\Delta E_g\right)_{s-Si}}{q} + V_T ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \quad (7)$$

The built-in voltage across the source-body and drain-body junctions in the relaxed $Si_{1-x}Ge_x$substrate can be inscribed as

$$V_{bi,SiGe} = V_{bi,Si} + (\Delta V_{bi})_{SiGe} \quad (8)$$

Where,

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \emptyset_{F,Si}$$

$$(\Delta V_{bi})_{SiGe} = \frac{-\left(\Delta E_g\right)_{SiGe}}{q} + V_T ln\left(\frac{N_{V,Si}}{N_{V,SiGe}}\right) \quad (9)$$

III. MODEL FOR THE OUTPUT CURRENT-VOLTAGE CHARACTERISTICS

Current at any point x along the channel is given by eqn.

$$I_D = WQ_{inv}(x)v(x) = WC_{ox}\left(V_{GS} - V_{th} - V(x)\right)v(x) \quad (10)$$

Where W is device width. So,

$$v(x) = \frac{I_D}{WC_{ox}(V_{GS} - V_{th} - V(x))} \quad (11)$$

By using, Analytical expression of drain current and (11) and$E_x = \frac{dV(x)}{dx}$, we get:

$$I_D\left(1+\frac{\mu_{eff}}{2v_{sat}}\frac{dV(x)}{dx}\right) = \mu_{eff}WC_{ox}\left(V_{GS}-V_{th}-V(x)\right)\left(\frac{dV(x)}{dx}-k\frac{V_{DS}}{L^2}\right) \qquad (12)$$

For $V_{DS} \leq V_{DS,sat}$

$$I_D = \frac{\mu_{eff}WC_{ox}}{L\left(1+\frac{\mu_{eff}V_{DS}}{2v_{sat}L}\right)}\left[\left((V_{GS}-V_{th})V_{DS}-\frac{V_{DS}^2}{2}\right)\left(1+\frac{k}{L}\right)+\frac{Ka}{12}\frac{V_{DS}^2}{L}\right] (13)$$

Where, $V_{DS.sat} = \frac{V_{GS}-V_{th}}{1+\frac{V_{GS}-V_{th}}{E_{sat}L}}$is the drain voltage for the carriers at the drain gets velocity saturation [8]. When V_{DS} is greater than $V_{DS,sat,}$ the velocity saturation or pinch off point moves toward the source of MOSFET, by a distance l_d.

$$l_d = l_c \sinh^{-1}\left(\frac{V_{DS}-V_{DS,sat}}{l_cE_{sat}}\right) (14)$$

Where,$l_c = \sqrt{\frac{\varepsilon_{av}x_{dv}}{2(C_{ox}+C_d)}}$,$\varepsilon_{av} = \frac{\varepsilon_{Si}+\varepsilon_{SiGe}}{2}$, $C_d = \frac{\varepsilon_{av}}{x_{dv}}$, and $x_{dv}$is the vertical depletion region depth due to gate bias, is given as,

$$x_{dv} = \sqrt{\frac{2\varepsilon_{SiGe}(\varphi_{th}-V_{sub})}{qN_A}}, \varphi_{th} = 2\varphi_{F,Si} + \Delta\varphi_{s-Si} \text{ and,}$$

$$\Delta\varphi_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} + V_T ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

Where φ_{th} is the minimum surface potential required for inversion [7].

IV. RESULTS

The device characteristics of strained n-channel MOSFET can be explained by Watt surface mobility model, the model is used to model the traverse-field dependent low field mobility [10],[12]. The device parameters used in our simulation are given in Table 1.

Parameter	Value
Ge mole fraction of SiGe substrate, x	0 – 0.4 (0 – 40%)
Source/Drain doping	$2x10^{20}$ cm^{-3}
Body Doping, N_A	10^{18} cm^{-3}
Gate Length, L	50 nm
ate Oxide Thickness, t_f	2.0 nm – 6.0 nm
Work function of gate material, φ_M	4.35 eV (n+ poly Si)
Strained-Silicon film thickness, t_{s-Si}	15 nm
Source/Drain junction depth, r_j	50 nm
Substrate bias, V_{sub}	0 Volts (Gnd)
Drain bias, V_{DS}	0.0 – 1.0 Volts
Gate bias, V_{GS}	0.4 – 1.0 Volts (V_{th}~ 0.25 V)

Table 1: Device parameters used in the simulation for the output characteristics of s-Si/SiGe MOSFET [14]

Fig. 1 shows the drain current variation w.r.t. drain voltage for various values of gate voltages V_{gs}(red),= 0.2 V, V_{gs}(green) = 0.4 V, V_{gs}(blue) = 0.6 V, V_{gs}(Indigo) = 0.8 V, V_{gs}(yellow) = 1.0 V; simulated on ATLAS simulator and accurately matched with modelled data [14].

Fig. 2 describes the drastic changes in drain current w.r.t. gate voltage (Input characteristics) of MOSFET without strain in normal conditions for different channel length condition. Where the threshold voltage is found to be changed each time and as the plot shows for different channel length of 60, 50 & 40 nm that threshold voltage is decreasing drastically at reduced channel length.

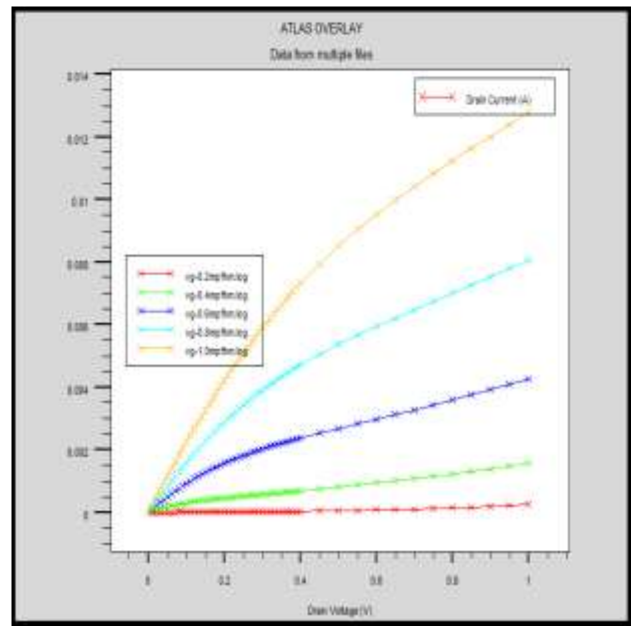

Fig. 1: Output characteristics (drain current (μA) v/s drain voltage (V)) for a unstrained MOSFET (x=0) at different values of gate voltages simulated with ALAS simulator.

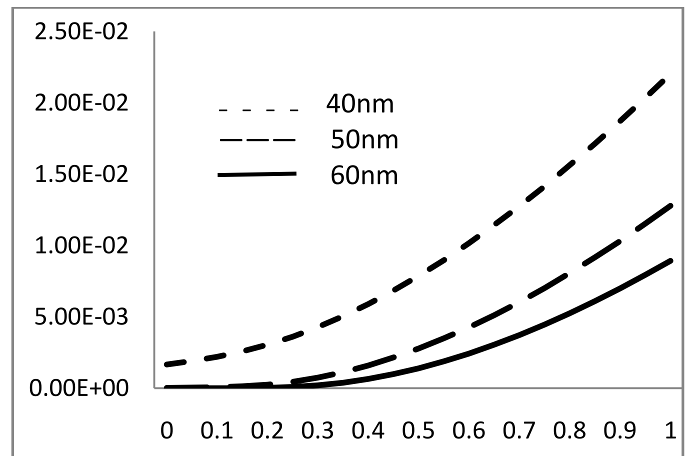

Fig. 2: Input characteristics of MOSFET for different channel lengthwithout strain in normal conditions, at metal work function 4.35 eV. Simulated with ALAS simulator. (y axis drain current in μA and X axis gate voltage in volt)

Fig. 3 describes the change in drain current w.r.t. gate voltage (Input characteristics) of MOSFET with a metal work function of 4.71 eV. It shows that drain current is reduced and threshold voltage increases by increasing work function.

Fig. 4 describes the drastic changes in drain current w.r.t. gate voltage (Input characteristics) of MOSFET with varying the levels of strain (Ge mole fraction in$Si_{1-x}Ge_x$) x=0 to x=0.4 where the threshold voltage is decreasing but the value of threshold voltage is positive even for 40 nm channel length. It can be easily seen here that by increasing the level of strain the changes in drain current occurs, as the drain current is increasing sharply.

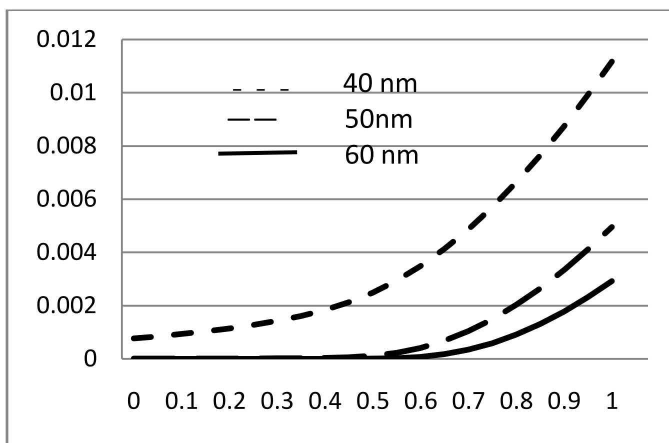

Fig. 3: Input characteristics of MOSFET for different channel length at metal work function 4.71 eV.Simulated with ALAS simulator(y axis drain current in µA and X axis gate voltage in volt)

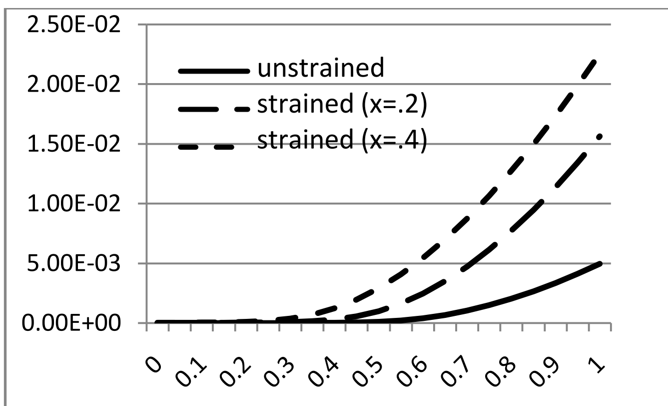

Fig.4: Input characteristics of MOSFET with various strain levels, as strain level increased the drain current curve variation increased at work function 4.71 eV.(Y axis drain current in µA and X axis gate voltage in volt).

V. CONCLUSION

Strain in the Si channel is evolving as an influential skill of growing MOSFET routine. In this paper, we have established a simple methodical model for the current-voltage characteristics of strained-Si/SiGe MOSFET. Our model has been verified for its accuracy using two-dimensional simulation under different bias conditions and technology parameters. Our results display that strain-induced enhancements will continue even for extremely short channel length devices. It also displays the variation in threshold voltage and drain current with changes in thickness of SiGe layer. Developments in n-MOSFET recital can be obtained in a wide range of operating conditions with modest strain.

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