Design of Optimized High Speed FIR Filter

V.N. Mahawadiwar[1], S. S. Shriramwar[2]

[1]*Asst.Professor, K.D.K. College of Engineering, Nagpur*

[2]*Asst. Professor, Priyadarshini College of Engg., Nagpurr*

[1, 2]*Maharashtra, India.* .

Abstract

For high performance and portable applications, Energy efficiency is one of the most required features for modern electronics systems design. This article proposes the implementation of FIR Filter using low power adder and multipliers. The ever increasing market segment of portable electronics devices demands the availability of low power building blocks. With the explosive growth in Laptops, portable personal communication systems and evaluation of the shrinking technology and flexible circuits, the efforts in low power micro electronics has been identified. In this scheme the function of adder is minimized by a technique called scaling and rounding-off Filter coefficient and truncation of unnecessary bits in order to reduce the power consumption of FIR Filter. Evaluation of power, area and speed for different types of adders and multipliers is carried out and the FIR filter is designed with optimized combination of adders and multipliers for low power and high speed application. The Full Adder designed with multiplexers do not exhibit any leakage problems and short circuits problems. The current trend towards low-power design is mainly driven by two forces, the growing demand for long-life autonomous portable equipment and the technological limitations of high- performance VLSI systems. The proposed Design of High Speed FIR Filter for DSP Application with Optimized Adder & Multiplier is simulated using Active HDL and implemented using Tanner tool.

Keywords: *FIR filter, Tanner Tool Adder, Multiplier, MAC.*

I. INTRODUCTION

Energy efficiency is one of the most required features for modern electronics systems designed for high performance and/ or portable applications. In one hand, the ever increasing market segment of portable electronics devices demands the availability of low power building blocks. We propose the implementation of FIR Filter using low power adder and multipliers. With the explosive growth in Laptops, portable personal communication systems and evaluation of the shrinking technology and flexible circuits, the efforts in low power micro electronics has been identified. To reduce the power Consumption of FIR Filter, function of adder is minimized by a technique called scaling and rounding-off Filter coefficient and truncation of unnecessary bits [1]. Evaluation of power, area and speed for different types of adders and multipliers will be carried out and the FIR filter will be design with optimized combination of adders and multipliers for low power and high speed application.

High speed and low power Full Adder cells designed with an alternative internal logic structure that lead to have a reduce power delay product (PDP) [2]. The logic approach uses only Ex-OR gate and multiplexer to implement the carry and sum. Ex-OR gate is the most power hungry component of the Full Adder Cells, therefore the new logic approach will reduce the power consumption. Multiplexers are used to design adder. The Full Adder designed with multiplexers may not have the leakage problems and short circuits problems.

The current trend towards low-power design is mainly driven by two forces, the growing demand for long-life autonomous portable equipment and the technological limitations of high-performance VLSI systems. For the first category of products, low-power is the major goal for which speed and dynamic range might have to be sacrificed. High speed and high integration density are the objectives for the second application category, which has experienced a dramatic increase of heat dissipation that is now reaching a fundamental limit. These two forces are now merging as portable equipment grows to encompass high Throughput computationally intensive products such as portable computers and cellular phones.

Signal processing applications typically exhibit high degrees of parallelism and are dominated by a few regular kernels of computation such as multiplication, that are responsible for a large fraction of execution time and energy. In such systems, multiplier is a fundamental arithmetic unit shrinking feature sizes are responsible for increasing thermal related problems as well [10].

II. LITERATURE REVIEW

M. Kathirvelu[1] in describes about low power high speed FIR Filter. Mariano Aguirre-Hernandez et al in [2], describes about An alternative internal logic structure for designing full adder cells in CMOS Full-Adders for Energy-Efficient Arithmetic Applications.

Hosseinghadiry.M et al [3], describes about Two New low power High Performance Full adders with minimum gates. Yingtao Jiang, Abdulkarim AI – Sheraidah, Yuke Wang, Edwin Sha,and Jin-Gyun Chung, [4], Introduces a novel multiplexer based low power full adder.

Zaid Al-bayati in [5] describes about Low power Wallace multiplier design. Weste N. and Eshraghian [6] describes about Principles of CMOS VLSI Design.

Senthilpari .S [7] describes about A Low-power and High-performance Radix-4 Multiplier Design Using a Modified Pass- transistor Logic Technique.

There are generally two methods through which we can increases the throughput of system.

A. Parallelism of system

It increases the sampling rate by replicating hardware ,so that several input can be process in parallel and several output can be produced at the same time.

B. Technology Enhancement

Table 1. Technological Comparison

ARCHITRCTURE TYPE	VOLTAGE	AREA	POWER
SIMPLE DATA PATH	5V	1	1
PIPELINING DATA PATH	2.9V	1.3	0.39
PARALLELE DATA PATH	2.9V	3.4	0.36
PIPELINING PARALLELE	2V	3.7	0.2

A FIR filter scheme suitable for unsigned and signed computations is presented in this paper. Low power designs for 6 Tap FIR filter using latch based and pipelining techniques are implemented. It can be seen that dynamic power consumption is decreased through the use of two techniques; latch based clock gating and pipelining of original 5 tap FIR filter.

III. FIR FILTER

A finite impulse response (FIR) filter is a type of a digital filter. The impulse response of an Nth-order FIR filter lasts for N+1samples, and then dies to zero. The most efficient way to reduce the power consumption of digital circuits is to reduce the supply voltage, since the average power consumption of CMOS digital circuits is proportional to the square of the supply voltage. The resulting performance loss can be overcome for standard CMOS technologies by introducing more parallelism and to modify the process and optimize it for low supply voltage operation. The major elements required in FIR Filter are: a) Delay Element. b) Multiplier. c) Adder as shown in Fig.1.
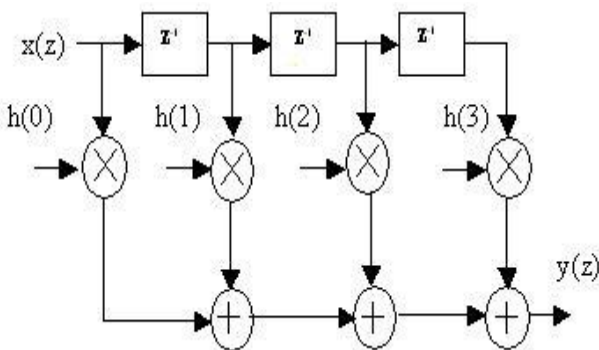

Fig. 1: Basic Structure of FIR Filter [1].

IV. PROPOSED IMPLEMENTATION

The implementation of n - tap FIR filter design using the low power adder and multiplier. Low power adder is designed with novel transistor level circuit design approach. Filters can be built in different technologies. The same transfer function can be realized in several different ways, that is the mathematical properties of the filter are the same but the physical properties are quite different. Often the components in different technologies are directly analogous to each other and fulfill the same role in their respective filters. We will calculate area and power used by FIR. Simple Data Path with Corresponding Layout is shown in Fig. 2 and Fig. 3 shows Parallel implementation of Simple Data Path.
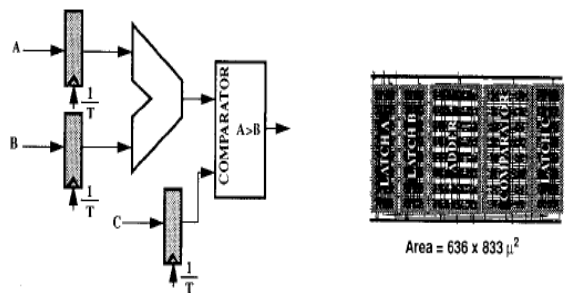

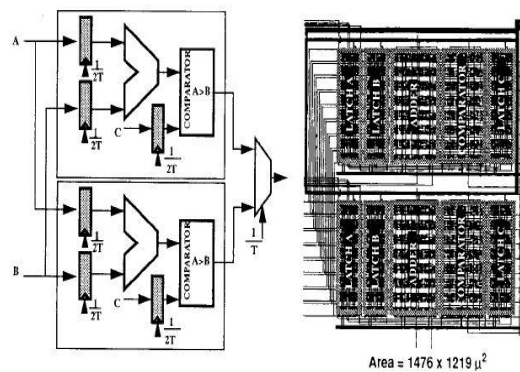**Fig. 2 Simple Data Path Showing Corresponding Layout.**

Fig. 3 Parallel Implementation of Simple Data Path.

We present two high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). Fig. 4 shows Full Adder cell formed by Three main logic blocks and an alternative logic scheme for designing Full Adder.
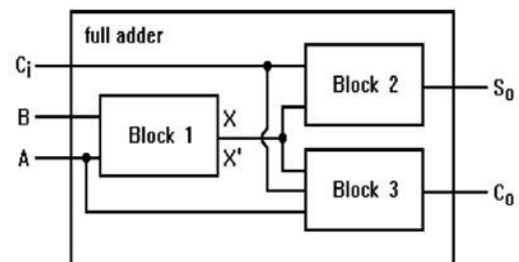

Fig.4. Full Adder Cell formed by 3 Main Logical Block [2].

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2.Truth Table for a 1-bit Full Adder

The multiply accumulate (MAC) operation is used as the kernel of various digital signal Processing algorithms. A variety of approaches to the implementation of the multiplication and addition portions of the MAC function are possible.
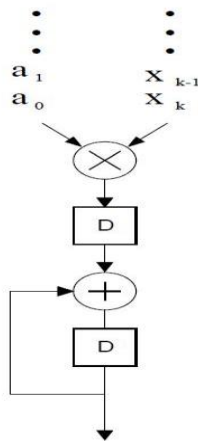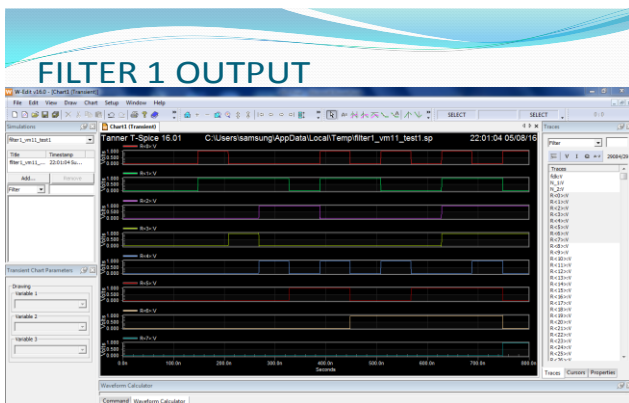

Fig. 5 MAC Unit.

V. RESULT

Comparison of Filter 0 &Filter 1

Table 3. Comparison of Filter 0 & Filter 1

DESIGN	AREA	POWER	CRITICAL PATH	DEALY
FILTER 0	16554 MOSFET	501.99 micro watt	65	4 TO 6n sec.
FILTER 1	6322 MOSFETS	414.44 micro watt	08	0.1to0.5 n sec

VI. APPLICATIONS

- Multiple optimization methods for low power FIR Filter takes into account, the various techniques that will be use to reduce power. Reduction in power will help in implementation of this research for DSP Application.
- Increased speed of FIR Filter can be used in FFT algorithm.
- Proposed FIR Filter can be used in DWT Algorithm.
- Optimized adder and multiplier can cope-up with MAC (Multiply Accumulate Operations).
- Proposed system will help in filter designing.
- Low power high speed FIR filter can be used for convolution.

VII.CONCLUSION

VLSI architecture for low power MAC has been presented in this research work. The basic building blocks for the MAC unit are identified and each of the blocks is analyzed for its performance. Power is calculated for the blocks. 1-bit MAC unit is designed. using this block, the N-bit MAC unit is constructed and the total power consumption is calculated for the MAC unit. The dynamic power which is determined by the equation

$$D_{ynamics} = \alpha\ CV^2_{dd}f$$

Where **α** is the switching activity factor, C is the capacitance, V is the supply voltage, and f is the clock frequency. To achieve low power in circuits one or more of the parameters must be minimized. The MAC unit designed in this work can be used in filter realizations for High speed DSP applications. The logic approach uses only Ex-OR gate and multiplexer to implement the carry and sum. Ex-OR gate is the most power hungry component of the Full Adder Cells, therefore the new logic approach is implemented to reduce the power consumption. Multiplexers are used to design adder. The Full Adder designed with multiplexers may not have the leakage problems and short circuits problems. The proposed Design of High Speed FIR Filter for DSP Application is with Optimized Adder & Multiplier. The proposed Design of High Speed FIR Filter for DSP Application with Optimized Adder & Multiplier is simulated using the Tanner tool. The performances parameter [power, area and latency] are calculated.

The average power consumed for Filter 1 is 414.44 µWatt. Low power utilization is the most important criteria for the high performance DSP system. This research implements a better performance FIR filter using low power adder and multiplier. On the basis of power consumption results of proposed and existing FIR filters. The conclusion come out that projected FIR filter consume lesser power than existing FIR filter. So according to the result proposed FIR filter is the best for DSP system.

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