Des IGN of Inexact Circuits using Gate-Level Pruning

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Abstract

Inexact and approximate circuit design is a promising approach to improve performance and energy efficiency . Such strategy is suitable for error-tolerant applications involving perceptive or statistical outputs. The gate-level pruning (GLP) is first demonstrated on adders and then Probabilistic pruning technique has been proposed for an efficient approximate tangent function. The approximation is based on a mathematical analysis considering the maximum allowable Significance-Activity Product (SAP) and unessential nodes. This significant saving is achieved by the pruned arithmetic circuits, which sets some nodes to constant values. The proposed approximation scheme is presented, which shows that the proposed structure compares favorably with previous architectures in terms of area, power and delay.

Key Terms: *GLP, SAP, Pruned Arithmetic Circuits, DCT, Hyperbolic tangent, Neural Network, Activation Function.*

I. INTRODUCTION

Neural networks are complex non-linear models, built from components that individually behave similarly to a regression model. They can be represented as graph and some sub-graphs may exist similar to that of logic gates. Although the structure of a neural network is explicitly designed beforehand, the processing that the network does in order to produce a hypothesis evolves during the learning process. This allows a neural network to be used as a solver that "programs itself", in contrast to typical algorithms that must be designed and coded explicitly. Evaluating the hypothesis defined by a neural network may be achieved via feed-forward, which amounts to setting the input nodes, then propagating the values through the connections in the network until all output nodes have been calculated completely. The learning can be accomplished by using gradient descent, where the error in the output nodes is pushed back through the network via back-propagation, in order to estimate the error in the hidden nodes, which allows calculation of the gradient of the cost-function.

The building blocks needed for neural networks are multiplier [6], adder [8], and nonlinear activation function. Many research has been done in multipliers and adders [9][10].

Hyperbolic tangent are used with back propagation algorithm. Activation functions have an s-shaped curve while their output range varies. Exponentiation and division terms present in hyperbolic tangent activation function, it is hard to represent.

To solve this problem, approximation schemes are applied.

II. RELATED WORKS

A technique for accuracy in area, power and delay. A CAD tool is used for conventional design. This method is first applied on adders and then on (DCT) Discrete Cosine Transform for achieving energy-delay-area and mean relative error. Pruning is removing the unessential nodes from the circuit. Significance Activity Product used for ranking the nodes.GLP is demonstrated by pruned arithmetic circuits, which sets some nodes at constant values and simplifies the circuit.

III. PROPOSED SYSTEM

In this paper, an efficient approximation scheme for hyperbolic tangent function is proposed. The approximation is based on a mathematical analysis. Activation Function is performed on multipliers. The proposed scheme reduces the area, delay time and power.

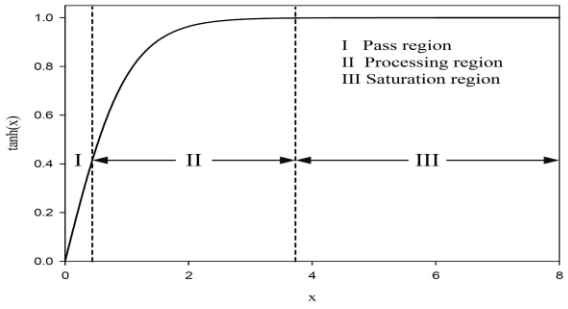


Figure 2: Different Regions of Hyperbolic Tangent Function

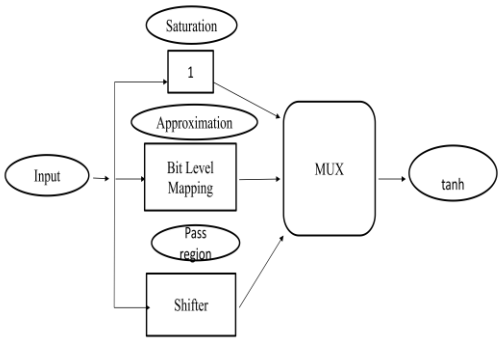


Figure 3: Block Diagram of The Proposed Structure

The above diagram has three main blocks to approximate the hyperbolic tangent function in three regions, Saturation, processing, pass region.

1) Pass Region *:*In this area, input is passed to the output and absolute value is processed.
2) Processing Region*:* For inputs bit-level input mapping is required. The approximation value should be less than the maximum allowable error.
3) Saturation Region Approximation*:* Hyperbolic tangent function is approximated by the maximum value by output bits, and determined by setting all output bits to 1.

IV. RESULTS AND DISCUSSIONS

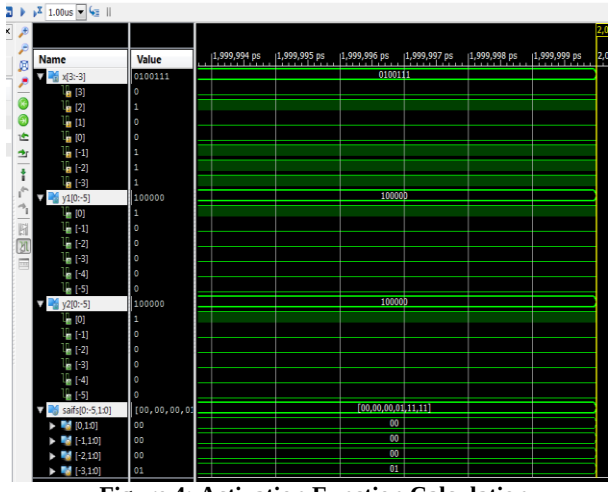
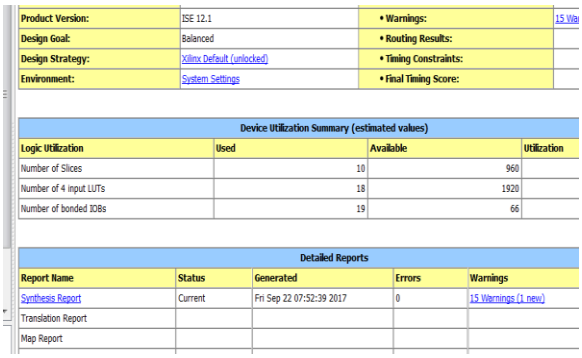


Figure 4: Activation Function Calculation

The activity of each wire is extracted from SAIF file. The nodes with the lowest SAP are pruned first and the hyperbolic tangent function is performed for the approximation.



Product Version:	ISE 12.1	• Warnings:	15 Wa
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	10	960	
Number of 4 input LUTs	18	1920	
Number of bonded IOBs	19	66	

Detailed Reports

Report Name	Status	Generated	Errors	Warnings
Synthesis Report	Current	Fri Sep 22 07:52:39 2017	0	15 Warnings (1 new)
Translation Report				
Map Report				

Figure 5: Synthesis Result

This synthesis report of proposed approach shows the slice, LUTs and bonded IOBs.

The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1i. The various parameters used for computing existing and proposed systems with Spartan-3 processor are given in the table.

Table 1-Comparison

S.No	Parameter	Existing	Proposed
1.	Area	19	10
2.	Delay Time	19.436ns	5.27ns
3.	Power	0.185	0.123

The synthesis report of existing and proposed approach has been tabulated thus the area, delay time, power has been reduced when compared to existing method.

Power Estimation

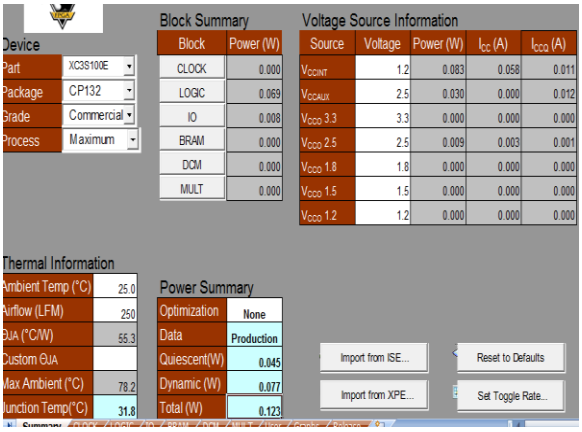


Figure 7: Power Calculation

Power is calculated by XPower Estimator-11.1 by using Xilinx with Spartan-3E Processor. The Quiescent power 0.045, Dynamic power 0.077, Total

power 0.123. The power is reduced compared to the previous methods.

After performing the synthesize process, the RTL schematic has been created automatically based on the functionality. The routing between the different cells can be viewed clearly by this schematic.

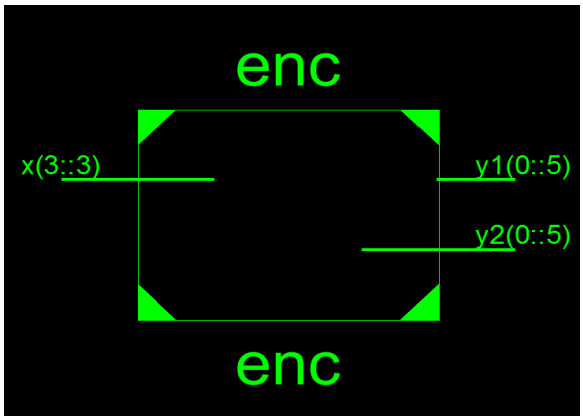


Figure 8: RTL Schematic

In digital circuit design, register-transfer level (RTL) is a abstraction which models a synchronous digital circuit in terms of the flow of digital signals between hardware registers and logic operations performed on those signals. A encoder is a device, circuit, software, algorithm that converts information from one format or code to other.

Performance Analysis

Figure 9: Performance Graph

In this section, the proposed hyperbolic tangent function is presented. Figure 9.shows the comparison of number of slice, LUT has reduced.

V. CONCLUSION

A new approximation scheme for hyperbolic tangent function was proposed in this project. The proposed approximation scheme is based on three regions. In this project gate-level pruning is applied on circuit and it determines the area, delay, and power. The proposed structure required less output bits.

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