Null Convention Logic (NCL) Design of Efficient Sorting Unit

E. Juhi Gladies[1], E. Thanga selvi[2]
1 PG Scholar, Dept. of ECE, PSNA CET
2 Assistant Professor, Dept. of ECE, PSNA CET., Dindigul, India.

Abstract:

Sorting is a method through which the data is assembled in ascending or descending order. To construct a sorting unit of N values from M inputs. The basic OR, AND gate are used to construct a sorting unit. NCL threshold gates are a specialized case of the logical operands or gates. Self-timed logic design process are developed using Threshold Combinational Reduction (TCR) in the Null Convention Logic (NCL) paradigm. NCL logic functions are constructed using 27 distinct transistor built-up networks. To implement partial sorting using NCL and max-set-selection units with low delay units. But, higher-speed estimation usually raises power consumption extremely. To reduce that problem, a low-power, high-throughput, and modular design of partial sorting network is presented. This paper presents the NCL threshold logic has been used in sorting techniques. The proposed technique is used for lower power consumption and high operating speed. All the circuits in null conventional logic is developed using Threshold Combinational Reduction (TCR) method. Overall NCL logic techniques are meant for reduced area and delay of sorted output.

Keywords: *Null convention logic (NCL), Threshold combinational reduction (TCR),delay insensitive, sorting network, Multi threshold complementary metal oxide semiconductor (MTCMOS) ,Threshold gates.*

I. INTRODUCTION

NULL CONVENTIONAL LOGIC is a new method designed for asynchronous circuits NCL is not based on DI circuit method called as quasi delay insensitive (QDI). The latency in the fanout is likely to be same as NCL which is symbolically complete and completely free from time dependencies. Thus the Implements NULL CONVENTIONAL LOGIC in economically available FPGA's. This document describes the basic understanding on NCL. NCL logic design is implemented using threshold gates with hysteresis. These gates have many inputs and one output.

The ASCEnD [1], flow to design NCL gates which enable design advancement opportunities for some asynchronous pattern. A set of 14 different NCL gates was designed at the layout level through the ASCEnD flow. NCL gates can be created through the ASCEnD flow, these gates can be used to improve an asynchronous design in terms of power consumption and operating speed.

The design methodology [2] that links multi-threshold CMOS (MTCMOS) into delay insensitive asynchronous circuits in order to solve the drawbacks of the synchronous correlative circuit. Due to the handshaking protocol and delay-insensitive nature, drawbacks in the MTCMOS synchronous complementary circuit can be eliminated. Thus ultra-low power consumption is achieved.

Various CMOS implementations [3] of asynchronous NULL Convention Logic (NCL) gates have been analyzed at various terms. This use a new way to design semi-static NCL gates. Several CMOS implementation schemes have been introduced for NCL gates include dynamic, static, semi static and differential. It can be carry out under moderately low supply voltage and consuming lower energy.

A process algebraic framework known as PAFSV [4] is implemented to the directed arrangement. The definition of PAFSV is defined by means of deduction rules that associate a time transition system with a PAFSV process. PAFSV is useful for the directed arrangement and analysis of System Verilog designs. Thus PAFSV to model and analyse classical circuits such as the Null Convention Logic (NCL) circuit.

Multi-Threshold CMOS (MTCMOS) to delay insensitive self- timed [5] NCL so called Multi-Threshold NULL Convention Logic (MTNCL) that can comparatively reduce leakage power and improve performance. This is used to reduce the delay requirements as compared to the CMOS logic designs and to reduce the generation of issues to improve the system performance.

Fine-grain power gating NCL [6] with early sleep (FPG-NCL- ES) and optimization (FPG-NCL-ES-OPT), which engage both fine-grain power gating and early sleep to achieve lower power consumption. The MTCMOS threshold gates in the FPG-NCL-ES pipeline have higher possibility of staying in the sleep mode. Thus higher maximum sustainable throughput rate is achieved.

A new methodology for mapping [7] multi-rail logic expressions to NULL convention logic (NCL) gate library is designed. Both mapping approaches were implemented in the Perl programming language and tested on some multi-rail logic expressions and circuit components. Thus the new mapping algorithm performs mapping in one pass requiring less

computation in the main loop.

Self-timed logic design [8] procedure is established using Threshold Combinational Reduction (TCR) within the NULL Convention Logic (NCL) criterion. TCR optimizations are estimated by comparing levels of gate delays, gate counts, transistor counts, and power consumption designs. This method has been used to design various delay-insensitive MACs, multipliers and ALUs. This method is used to maximize output of combinational circuits.

Fault attack [9] in pipelined NCL the generation characteristics was analyzed and a new structure called the synchronization self-feedback random tower (SFRT) is designed. The register design consists of a two-level and three-cycle ring layout and efficient obstacle against the fault injection.

In ternary circuits for null convention logic [10] using an offset ternary logic system which consists of the logic set {t, N, O} maps to voltage levels {+V DO' V 00/2, OV}.This has the ternary detector and register block and thus multi-rail binary counterparts has been exchanged.

II. NCL OVERVIEW

Null convention logic uses delay insensitive code for data communication between set and reset phase. This combines data and null in mixed path. NULL mean NODATA or spacer between DATA. It indicates no input or output is present. Basically, in set phase data changes from spacer (NULL) to proper code (DATA).The NCL which uses delay insensitive circuit is which operate with positive bounded and robust. NCL circuits are constituted of 27 major gates, which constitute the set of all functions composed of small number of variables. Every NCL systems must satisfy the following two benchmarks to be delay-insensitive

1. Input-Completeness
- Outputs of the circuits changes from NULL to DATA only after all inputs transition from NULL to DATA
- Outputs of the circuits changes from DATA to NULL only after all inputs transition from DATA to NULL

2. Observability
- All gate transitions must be observed at the output (the gate which is described must contain atleast one output to be asserted).

The fundamental type of threshold gate, is the THmn gate, where $1 \leq m \leq n$. THmn gates have n inputs and m as threshold.

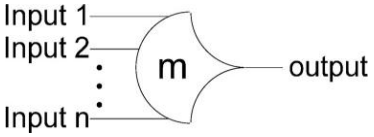


Fig.1 THmn Threshold Gate

Null convention logic is Asynchronous Circuits is the main advantage. Synchronous circuits are generally Time dependent

i.e. clock signal. In an asynchronous circuit the clock signal is replaced with handshake signals for synchronization, communication between their components. The benefits of asynchronous circuits are:

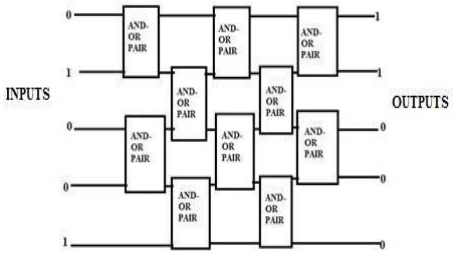
- Due to absence of clock signal, there is Low power consumption between the components
- Absence of clock distribution, so that clock routing can be overcome
- The operating speed is high, as it does not depends on the global latency
- There is no clock signal so the circuit noise is less

Classical Boolean logic is not symbolically complete in expression. They are dependent on control logic called time. The time dependence expression will depend on propagation of delay to determine correctness of data and control dependent factor. To eliminate both the dependencies from the Boolean logic and make it symbolical complete. The DI circuits are circuits which operate correctly with positive bounded but unknown delay in wires as well as gates. Thus these circuits are extremely robust and expensive to design.

NCL systems contain two DI registers, one at both the input and at output. Two interrelated register stages communicate by request and responds signals, to prevent the current DATA wave front from overwriting by conforming that the two DATA wavefronts are always separated by a NULL. NCL registration is realized through cascaded arrangements of single-bit dual-rail registers. These registers consist of TH22 gates that pass a DATA value at the input only when Ki is request for data (rfd) (i.e. logic 1) and send NULL only when Ki is demand for null (rfn) (i.e. logic 0).They also contain a NOR gate to generate K0, which is rfn when the register output is DATA and rfd when the register output is NULL.

The registers are reset to NULL, since all TH22 gates are reset to logic 0. Either register could be instead reset to a DATA value by replacing exactly one of the TH22n gates with a TH22d gate.

III DESIGN OF NULL CONVENTION THRESHOLD SORTING UNIT



Sorting is the process of readjusting a

sequence of objects to align in logical order. Sorting plays a major role in commercial data processing and in modern scientific analysis. Applications abound in transaction processing, combinatorial optimization, nuclear physics, molecular dynamics, etymology, genomics, weather analysis, sort a name list and computer graphics. There are different types of sorting are available. Bubble sort compares every adjacent pair swap their position at right order. Merge sort is a comparison based algorithm that uses divide and conquer approach to sort an array in O(n log n) time.

Merge sort is a stable sort, it preserves the order of same array elements after sorting. Algorithm for Merge sort is Divide the array into 2 halves recursively and Merge the divided parts in sorted order. A parallel sorting network is a collection of correlated compare-and-exchange (CAE) blocks that leads a parallel set of inputs to a parallel set of outputs in sorted order. Each CAE block has two inputs and two outputs. The input values are directed to the corresponding output or else it will be get swapped. There are increasing and decreasing CAE block.

Comparator networks are abstract devices built up of a fixed number of "wires", carrying values, and comparator modules that connect pairs of wires, swapping the values on the wires if they are not in a desired order. Such networks are typically designed to perform sorting on fixed numbers of values, in which case they are called sorting networks.

A sorting network consists of two types of items: comparators and wires. The wires are thought of as running from left to right, carrying values (one per wire) that traverse the network all at the same time. Each comparator connects two wires. When a pair of values, traveling through a pair of wires, encounter a comparator, the comparator swaps the values if and only if the top wire's value is greater than the bottom wire's value. Binary sorting is a process through which the data is arranged in ascending or descending order.

The basic OR,AND gate are used to design a sorting unit. Partial sorting with minimum costs will be more beneficial than the complete sorting method.

Because total sorting is the problem of returning a list of items such that its elements all appear in order, while partial sorting is returning a list of the *k* smallest (or *k* largest) elements in order.

The other elements (above the *k* smallest ones) may also be stored, as in an in-place partial sort, or may be discarded, which is common in streaming partial sorts.

Fig.2 Sorter unit

By this implementation of sorter unit there are many advantage and applications. But this sorter unit has few disadvantages like more power and area utilization. So we move for Null convention sorter using threshold gate. THmn gate is the primary type of threshold NCL gate with n-inputs and single output, Z where the inputs are combined to the logic gate.

The threshold, m is written in the gate, where $1 \leq m \leq n$ (Fig.1). THmnWw1w2…wR is another type of threshold gate, called weighted NCL threshold gate . Weighted NCL threshold gates contain an integer value, $m \geq wR > 1$, given to input R. The design process of any circuits in NULL conventional logic is implemented using *threshold combinational Reduction (TCR) method*. The above expression of the circuit is defined in Boolean logic.

Library of 27 special gates. It is on the basis of sorting N values from M inputs. NCL gates have hysteresis the output remains maintained until all inputs are get allotted. This hysteresis action ensure a full transition of input back to NULL before output associated with next input is allotted. The hysteresis behaviour is achieved by keeping the output as in the same state as previous till all the input goes to NODATA.

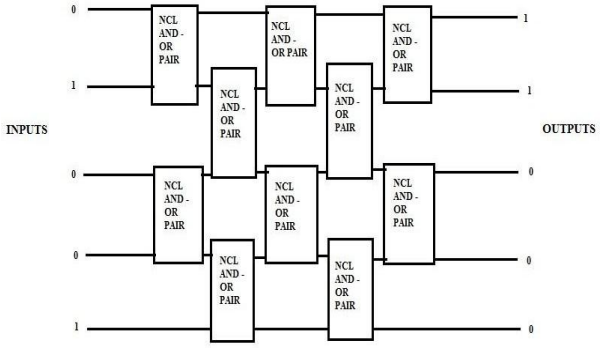


Fig.3 Sorting Unit using NCL Threshold Gate

NCL gates has 4 transistor network consisting of set, reset, hold0, hold1. The set function become true only when output is get allotted. The set function of each gate will be designed differently. Thus by implementing Null convention threshold gates overall power, area and time is reduced.

IV SIMULATION AND RESULTS

Finally, the 8-bit sorting unit using NCL threshold gate was designed. The proposed system has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1i. The various parameters used for computing existing and proposed systems with Spartan-3 processor.

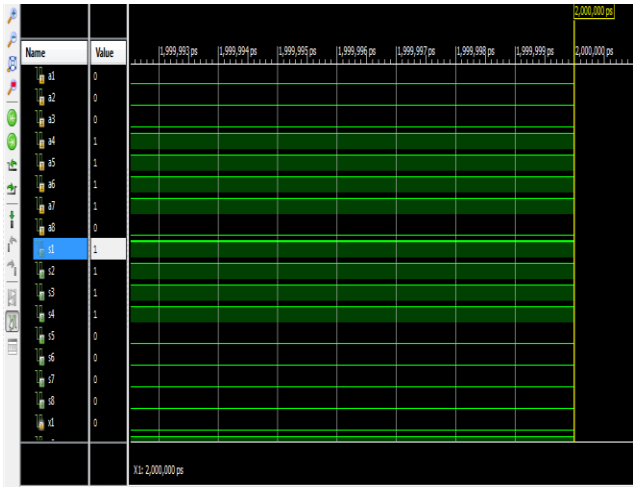


Fig.4 Sorted output

The simulation output for sorting unit is shown in the figure 4.

The power parameter provides the power consumption of the NCL through the Xilinx Power analyzer software. The total power consumption of the device must be sufficiently low for low power application.

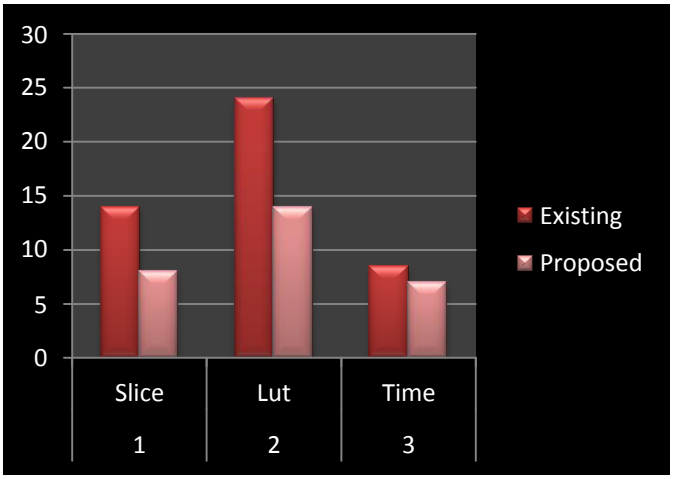


Fig.5 Power Report for 8bit NCL Sorter

The below table shows how the proposed method helps to reduce LUT count, time delay and power.

Table.1 Comparison Results of Existing System and Proposed System

S. No	Parameter	Existing	Proposed
1	**Slice**	14	8
2	**LUT**	24	14
3	**Time**	8.421	6.991
4	**Power**	0.220	0.151

V CONCLUSION

Sorting is an important operation in a wide range of applications including data mining, digital signal processing, network processing, scientific computing, and high-energy Physics. The NCL 8bit sorting has presented the design and implementation of flexible, low-latency, minimum consumed area of NULL convention logic (RL-NCL) based N-to-M sorter. The 8bit NCL low-power architecture provides an alternative solution for users. The NCL based sorter drastically reduces power consumption up to 31% and area up to 43%, it is much more feasible for applications such as wearable and implantable devices, which are required to provide long usage times between battery replacements.

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