Usage of Gain Cell Embedded Dram in Low Power Applications

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Abstract:

Gain - Cell embedded DRAM (GC-DRAM) has latterly been confessed as conceivably replaced to conventional SRAM. While GC- e DRAM potentially allow for high -balance , low- outflow, low- voltage, and 2 - focussed verdict, its modest priority time permit occasional, power - hungry renew cycles. The disadvantages are further strengthen at ascend inventions, where expanding sub threshold leakage currents and decreased in - cell storage capacitances results in faster data deterioration. In this project, we present a novel 4T GC- e DRAM bit cell that utilizes an internal feedback contraption to remarkably increase the data retention time in scaled CMOS technologies. A 2 kb memory macro was implemented in a low power 65nm CMOS technology, displaying an over 3× improvement in retention time over the best previous publication at this node.

Indexterms: *Gain-cell Embedded dynamic Random Access Memory (GC-e DRAM), Single Event Upset (SEU), Error Correction Codes (ECC), Data Retention Time, Low Power Applications.*

I. INTRODUCTION

Dynamic Random Access Memories (DRAM) is widely used in processor design. Distinct units have been proposed in the last to over- whelmed responsibility correlated with low retention time, degradation in performance due to process deviations and sensitivity to soft errors. This paper proposes two novel DRAM cells (referred to as 4TI and 4T1D) that utilize the techniques of gated diode and forward body-biasing to overcome the above controversies. The designs of these cells are evaluated by HSPICE simulation; different figures of merits (such as Read delay, Write delay, retention time, power dissipation, critical charge and layout area) are estimated and a comparative analysis of the proposed cells with existing cells is pursued. The 4TI cell achieves the best power distraction, while the 4T1D achieves the best retention time, the highest detracting charge and the least average Read delay. An thorough simulation based evaluation of system variations is also presented to confirm that using static and Monte Carlo based analysis, the proposed cells are probably to be less afflicted by process variations (in verge voltage and persuasive channel length) than the other cells found in the technical literature.

Types OF DRAM:

There are two types of DRAM. They are

- Asynchronous DRAM
- Synchronous DRAM

Every bit of data in a DRAM is stored as a positive or negative electrical charge in a capacitive form. The structure supporting the capacitance, as well as the transistors that control access to it, is generally indicated to as a *DRAM cell*. They are the constitutional building block in DRAM arrays. Multiple DRAM memory cell's modification exist, but the most commonly used derived form in modern DRAMs is the one-transistor, one-capacitor (1T1C) cell. The transistor is used to admit current into the capacitor during writes, and to discharge the capacitor during reads. The access transistor is designed to maximize drive strength and minimize transistor-transistor leakage. The capacitor has two final cells, one of which is related to its access transistor, and the other to either ground or $V_{CC}/2$. In modern DRAMs, the concluding case is more common, since it allows faster operation. In newfangled DRAMs, a voltage of $+V_{CC}/2$ side to side the capacitor is unavoidable to reserve a logic one; and a voltage of $-V_{CC}/2$ across the capacitor is required to supply a logic zero. The electrical charge stored in the capacitor is determined in coulombs. pursuing the retention time of a gain-cell-embedded dynamic-random-access-memory massive cell approved to system variations and manipulating data, thereby reducing the data retention power of the array. Gain cells have recently been shown to be a feasibly substitute to static random access memory in low-power applications due to their less emission currents and high density. The primary integral part of power utilization in these arrays is the dynamic power consumed at the same time as sporadic simulation. Exhilaration set up is consistently set according to a least-case appraisal of retention time under intense procedure variations, and bad-case access data, prominent to repeated power-desirous refresh cycles[1].method for a permissive sub-0.9 V logic-appropriate embedded DRAM (e DRAM) are bestowed. A boosted 3Tgain cell utilizes Read Word-line (RWL) preferential boosting to increase read margin and improve data retention time. Read speed is embellished with a composite current/voltage sense amplifier that allows the Read Bit-line (RBL) to endure close to VDD. A controlled bit-line write

pattern for forceful the Write Bit-line (WBL) is outfitted with a steady-state storage node voltage oversees to overcome the data '1' write commotive complication of the PMOS gain cell without recommending another boosted supply for the Write Word line (WWL)over-drive. An flexible and die-to-die alterable read citation bias generator is proposed to cope with PVT variations. Monte Carlo simulations compare the 6-sigma read and write performance of proposed e DRAM against conventional design [2].Circuit techniques for enhancing the retention time and random cycle of logic-compatible embedded DRAMs (e DRAMs). An asymmetric 2T gain cell handles the gate and junction leakages of a PMOS write device to maintain a high data '1' voltage level which enables fast read access using an NMOS read device. A current-mode sense amplifier(C-S/A) high lighting a cross-coupled PMOS latch and pseudo-PMOS diode pairs is proposed to overcome the inherited problem of small read bit-line (RBL) voltage swing in 2T e DRAMs with improved voltage headroom and better impedance matching under process–voltage–temperature (PVT) variations. A half-swing write bit-line (WBL) scheme is adopted to improve the WBL speed and reduce its power dissipation during write-back operation with no effect on retention time[3].With an area-efficient single inverter sensing scheme designed for R/W speed compatibility with ultralow power processors, array efficiency is maintained for memories as small as 2kb and for as few as 32 bits per bit line[1].The forward data-in pipeline splits the clock for the master and slave stages of the flop. The circuit shown forces the slave stage to enable only after the succeeding master stage has locked out thus preventing a race in the forward path[10].

II. SEU MITIGATION METHODS

A single event upset (SEU), is an unintentional change of state caused by ionizing radiation in any integrated circuit, including ASIC, ASSP, FPGA, memory, logic, and mixed-signal devices. Despite of SEUs are extremely exceptional and fully recoverable in Xilinx devices, Xilinx figure out the need for the utmost in system authentication and opportunity, and that managing SEUs requires far more than simply estimating SEU Failures-In-Time (FIT). To that end, Xilinx provides system designers a inclusive solution for SEU mitigation. The first SEU mitigation solution that has been used for many years in spacecraft was shielding, which reduces the particle state of constant change to very low levels, but it does not completely eliminate it. This solution was adequate to avoid failure caused by radiation effects for many years in the past. However, due to the continuous evolution of the fabrication technology process, as explained in last chapter, electronic circuits are becoming more and more sensitive to radiation particles and the charged particles that once were insignificant are now able to cause errors in the electronic layout. Consequently, extra techniques must be applied to avoid radiation effects[10].Several SEU mitigation techniques have been proposed in the last few years in order to prevent defects in digital circuits, containing those enforced in programmable logic. They can be top secreted as:

- Fabrication method-based approach, such as: • Epitaxial CMOS processes • Advanced process such as silicon-on-insulator (SOI). - Also there are Design-based techniques, such as: Detection techniques: Hardware redundancy Time redundancy EDC (error detection coding) Self-checker techniques

Mitigation Techniques:

- Triple Modular Redundancy (TMR)
- Multiple redundancies with voting
- EDAC (Error detection and correction coding)

Seasoned memory cell level - And Rehabilitated Techniques (applied to programmable logic only), such as:

- Reconfiguration
- Partial configuration
- Rerouting design

The Deceit process-based techniques, also called specialized techniques, such as epitaxial CMOS process and silicon-on-insulator (IBM, 2000; Colinge, 2001; Musseau and Ferlet-Cavrois, 2001), can reduce to adequate levels some of the disseminated possession, such as Total Ionization quantity (TID) effects and single event latch-up (SEL), however, they do not completely ignore upset effects, such as single event upsets (SEUs) and single transient effect (SET).[9][10] The fabrication process-based solution is extravagant and therefore very few designs have adopted this technique, particularly for less capacity of management. In (Irom et al., 2002), SEU effects from heavy ions and protons are delibrated for Motorola and IBM silicon-on- insulator microprocessors, and compared with results from similar devices with bulk substrates[12][13]. Results show that the threshold LET values of the SOI processors are nearly the same as those of bulk/epi processors from the same manufactures, indicating that little improvement in SEU sensitivity has resulted from the move to SOI technology[7][8].

III. PROPOSED 4T GC-e DRAM MEMORY

Gain-Cell embedded DRAM (GC-e DRAM) has recently been recognized as a possible alternative to traditional SRAM. While GC-e DRAM inherently provides high-density, low-leakage, low-voltage, and 2-ported operation, its limited -retention time requires

periodic, power-hungry refresh cycles. This drawback is further enhanced at scaled technologies, where increased sub-threshold leakage currents and decreased in-cell storage capacitances result in faster data deterioration. In this project, we present a novel 4T GC-e DRAM bit cell that utilizes an internal feedback mechanism to significantly increase the data retention time in scaled CMOS technologies. A 2 kb memory macro was implemented in a low power 65nm CMOS technology, displaying an over 3× improvement in retention time over the best previous publication at this node.

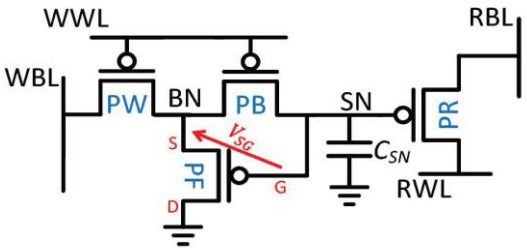

Fig 2: Structure Of 4T GC-e DRAM

The immediate conclusion from the phenomena presented above is that the data '0'state is the bottleneck that needs to be resolved in order to increase the retention time of this bit cell. The proposed cell addresses this by adding a buffer node (BN) and a feedback device to the basic configuration, as show in Fig. SN is connected in a feedback loop to the feedback device (PF), which conditionally discharges the BN according to the stored data state. An additional buffer device (PB) separates the stored data level from the BN to ensure extended retention time. The resulting 4T bit cell is built exclusively with standard threshold-voltage (*VT*) transistors and is fully compatible with standard CMOS processes. PMOS devices are selected over NMOS due to their lower sub-*VT* and gate leakages to provide longer retention times while maintaining a small cell area. Detailed cell operation is explained hereafter.

Cell access is achieved in a similar fashion as with a standard 2T cell. During writes, the write word line (WWL),which is connected to the gates of both PW and PB, is pulsed to a negative voltage in order to enable a full discharge of SN(when writing a '0'). Readout is performed by pre-discharging the read bit line (RBL) to ground and subsequently charging the read word line (RWL) to *V*DD. RBL is then provisionally charged if the storage node is low, and in another way remains dismissed. To save area and power, a simple sense inverter is used on the readout path; however, other conventional sense amplifiers can be used for improved read performance.

IV. ERROR DETECTION AND CORRECTION

Electrical or magnetic impedance inside a computer system can cause a single bit of DRAM to instinctively flip to the opposite state. The majority of one-off ("soft") errors in DRAM chips appear as a result of circumstances radiation, chiefly neutrons from cosmic ray secondaries, which may change the elements of larger objects of one or more memory cells or intervene with the circuitry used to read/write them. Recent studies contribute broadly varying error rates for single event upsets with over seven orders of importance dissimilarity, ranging from about one bit error, per hour, per gigabyte of memory to one bit error, per century, per gigabyte of memory.

The problem can be diminished by using repetitious memory bits and supplementary circuitry that use these bits to detect and correct soft errors. In most cases, the detection and correction logic is accomplished by the memory controller constantly, the unavoidable logic is apparently enforced inside DRAM chips or modules, enabling the ECC memory range of capabilities for otherwise ECC-incapable systems. The extra memory bits are used to note parity and to enable missing data to be build up by error-correcting code (ECC). Parity acknowledges the detection of all single-bit errors (actually, any odd number of wrong bits). The best common error-correcting code, a SECDED Hamming code, acknowledge a single-bit error to be corrected and, in the usual arrangement, with an extra parity bit, double-bit errors to be detected.latter analysis give widely varying error rates with over seven orders of magnitude difference, ranging from 10^{-10}–10^{-17} error/bit·h, roughly one bit error, per hour, per gigabyte of memory to one bit error, per century, per gigabyte of memory. The Schroeder et al. A study reported a 32% chance that a given computer in their study would suffer from at least one correctable error per year, and provided proof that most such errors are sporadic hard rather than soft errors. Another study at the University of Rochester also gave evidence that a substantial fraction of memory errors are intermittent hard errors. Large scale studies on non-ECC main memory in PCs and laptops suggest that undetected memory errors account for a substantial number of system failures: the study reported a 1-in-1700 chance per 1.5% of memory tested (extrapolating to an approximately 26% chance for total memory) that a computer would have a memory error every eight minutes.

V. SEQUENTIAL DIAGRAM DEPICTION

A Sequential diagram professing the error detection and correction design is shown in Fig. early, an *N*-bit word (DI) and its reciprocal (DIB) are written to the input write address. In aligned, the parity of DI is calculated and stored in the memory array. Following some period of retention, the desired word in the array is read, outputting the data (DO)

and its reciprocal value (DOB). These two values are bitwise distinguished, and if any of the bits are proportionate, an error has occurred, and a device checks the parity of the DO vector against the stored parity bit.

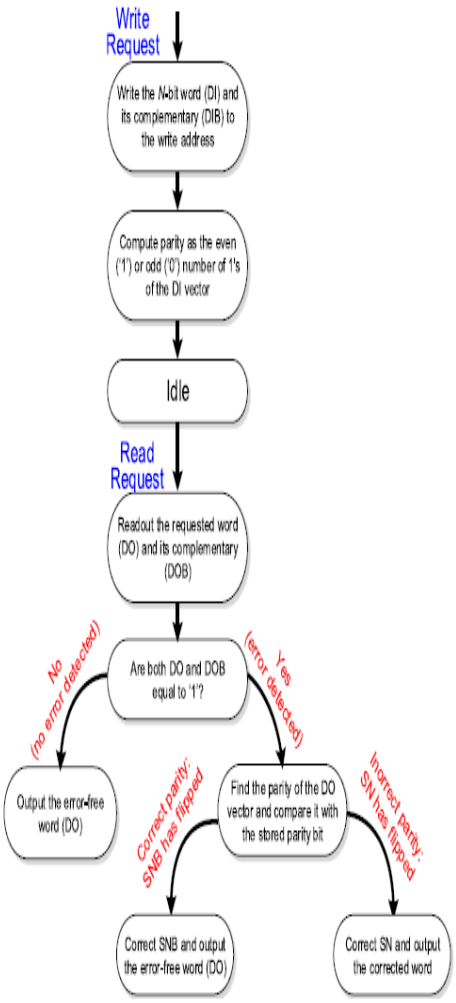

Fig 3: Sequential Diagram for Error Correction and Detection Using Seu Algorithm

If the parity is construct to be correct, the SNB of the erroneous bit has flipped, while if the parity is correct, the SN value is incorrect.

The erroneous data are then corrected to provide an error-free output. Note that the recommended error correction scheme with a single parity bit for an *N*-bit word does not handle to multiple bit upsets, which can be persuaded through highly forceful cosmic ray particles developing in a parasitic bipolar conduction, conceivably flipping numerous bits in a single well. To account for more than one error per every set of bits that includes parity, bit interleaving techniques can be used. However, for single-ended readout storage architectures, half-select susceptibility is a problem that must be addressed, if column multiplexing or byte masking is required. This can easily be solved by either writing entire words at a time, or by performing a read-modify-write operation, when byte masking is required. In addition, parity can be applied to every $k < N$ bits for additional protection.

VI. SIMULATION RESULT

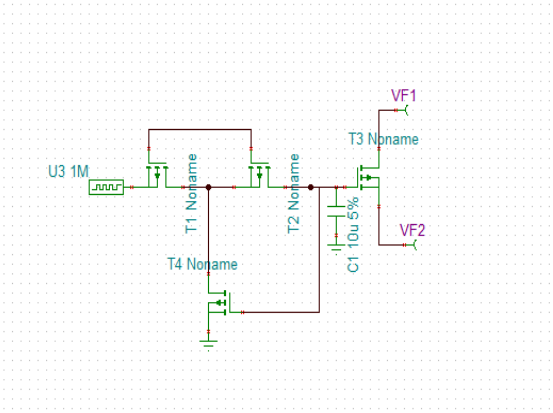

Fig 4: Layout Design OF 4T GC-E DRAM

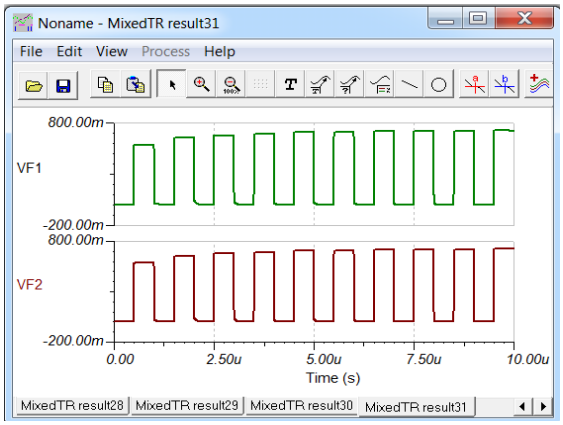

Fig 5: Simulation Result For 4t GC-E Dram

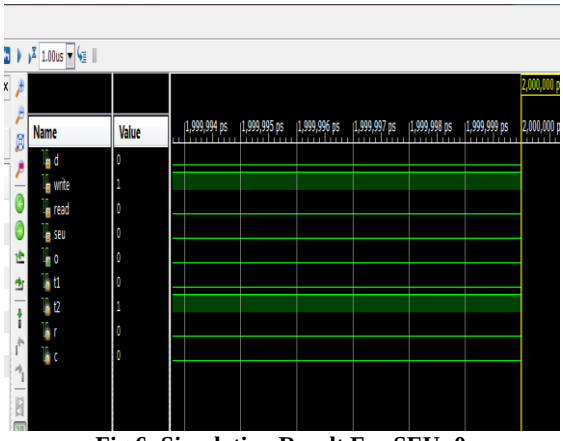

Fig 6: Simulation Result For SEU=0

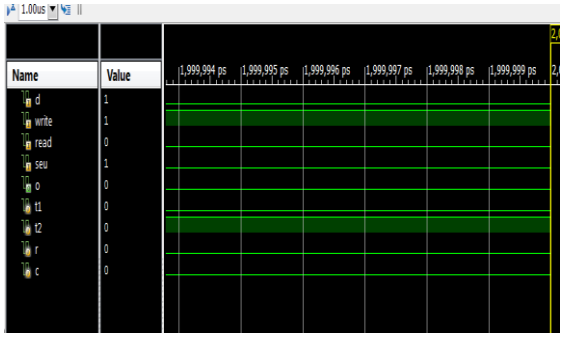

Fig 7: Simulation Result For SEU=1

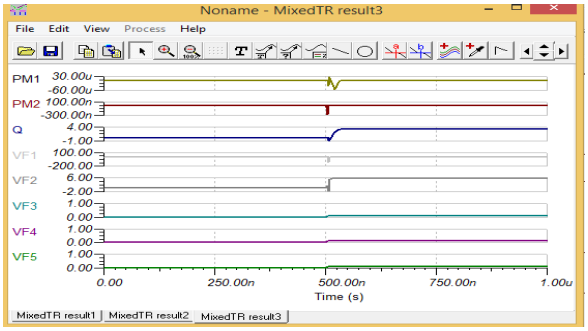

Fig 8: Comparison Result

Table I: Comparison of Various Parameters

S.NO	PARAMETER	PROPOSED
01.	POWER	100ns
02.	SLICE	2
03.	LUT	4

Performance Analysis

The Figure given below is shown that there is a considerable reduction in time and area based on the implementation results which have been done by using TINA. The proposed algorithm significantly reduces area consumption when compared to the existing system.

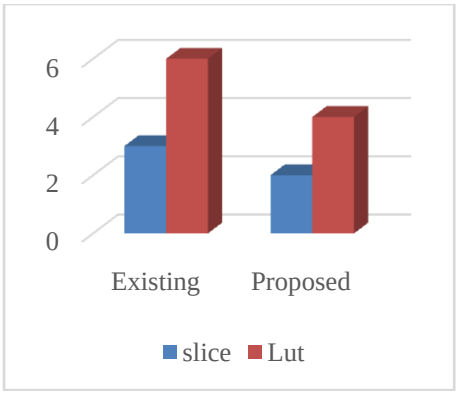

Fig 9: Performance Analysis

VI.CONCLUSION

In view of device scaling issues, embedded DRAM (e DRAM) technology is being considered as a strong replaced to conventional SRAM for use in on-chip memories. Memory cells designed using e DRAM technology in addition to being logic-compatible, are variation tolerant and immune to noise present at low supply voltages. This paper proposes a novel 4T GC-e DRAM for use in scaled CMOS nodes characterized by high leakage currents. The bit cell design protects the weak data level (‘0’) by a conditional unit-internal feedback path, while the feedback is disabled for the strong data level (‘1’). The proposed cell is shown to enable low power when compare with existing one, making it an appealing high-density, low-leakage alternative.

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