

An Efficient Bandwidth Utilized FFT Computation using Highly Accelerated Advanced Multiplier

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Abstract:

During last decades demand for integrated circuits design increases in order to meet the requirement of High speed, High throughput and area efficient. In Digital Signal Processing systems Fast Multipliers are essential. The speed of the multiplication is important not only in digital signal processing but also in general purpose processors. Here a Fast Fourier transform is implement using twin precision technique. By adapting efficient multipliers to the bit widths of the operands reduce the dissipation of power. Computational throughput is increased by performing narrow-width operation in parallel. Efficient bandwidth utilization can be achieved by using twin-precision technique with Baugh-Wooley algorithm.

Keywords: Fast Fourier Transform, Baugh-Wooley Algorithm, Twin precision

I. INTRODUCTION

In the Field of Digital Signal Processing such as Spectral Analysis, linear filtering, correction analysis etc., Fast Fourier transform (FFT) is widely using algorithm to compute Discrete Fourier transform and its inverse. It is used in many applications such as speech, image, Radar processing [1][2][6].In digital systems selecting a Power efficient multiplier plays a major role in Very Large Scale Integration (VLSI)

system. Among these multiplier, the basic multiplication is implemented using booth [5] or Baugh-Wooley algorithm[3].The bit width of the multiplier to be as wide as possible for largest operand that run on digital system.

To measure and compare the efficiency of algorithm depends on complexity of multiplication, since among all operation multiplications are complicate to design [4].In the Field of VLSI, Multiplication consumes more time and power for entire process, resulting large size and Expensive.

II. FAST FOURIER TRANSFORM

To compute Discrete Fourier transform, Fast Fourier transform is an efficient algorithm. The Basic Butterfly structure of FFT algorithm is shown in Fig.1.

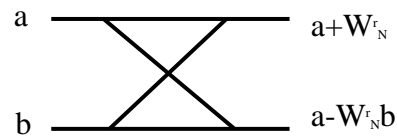


Fig 1: Basic Butterfly Computation Decimation in time FFT Algorithm

A sequence of values are decomposes in to different frequency components by using Discrete Fourier transform. It is using in many applications even

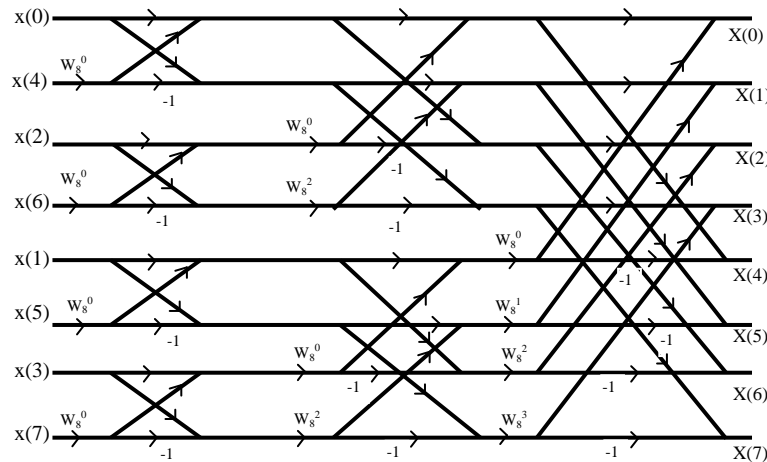


Fig 2: Eight Point Decimation in time FFT Algorithm

The DFT is defined by the formula

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N} \quad k=0, 1, 2, \dots, N-1$$

Evaluating this operation directly requires N^2 complex multiplications and $N(N-1)$ complex addition operations. To illustrate the savings FFT requires $N/2 \log_2 N$ complex multiplications and $\log_2 N$ complex addition operations.

In order to decompose Discrete Fourier transform, FFT algorithm requires $\log_2 N$ stages; each stage consists of $N/2$ butterfly computations. The structure of 8-point FFT Butterfly computation is shown in Fig. 2.

Twin-Precision

The Basic technique used for unsigned binary multiplication is twin precision[7]. In an unsigned Binary multiplication each bit of first operand called binary multiplier, is multiplied with each bit of second operand, called multiplicand generates a row of Partial products. An unsigned 8-bit multiplier is shown in Figure 3 depending upon position of Multiplier bit, each row of partial product is shifted

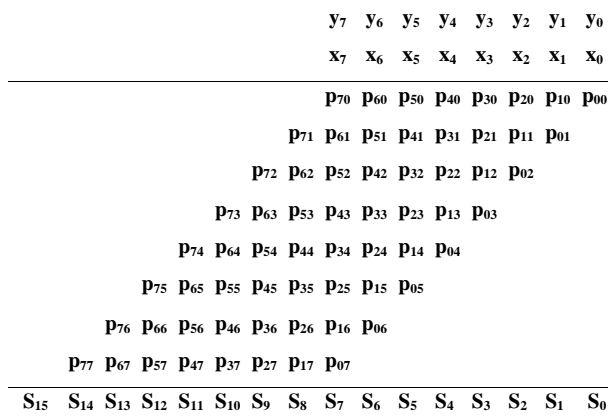


Fig 3: Illustration of an Unsigned 8-bit Multiplication

III. PROPOSED WORK

A signed multiplication is implemented with twin-precision using Baugh-Wooley algorithm. In many applications Signed multiplication is using rather than unsigned multiplication. The efficient algorithm used for signed multiplication is Baugh-Wooley [4].

It is possible to perform two multiplications without changing the way of summation using same partial product array by making unwanted partial products shown in gray to zero. Then it is possible to partition the multiplier in to two small bit multipliers to compute two multiplications in parallel. A signed 8-bit multiplication, using the Baugh-Wooley algorithm is shown in Fig.4.

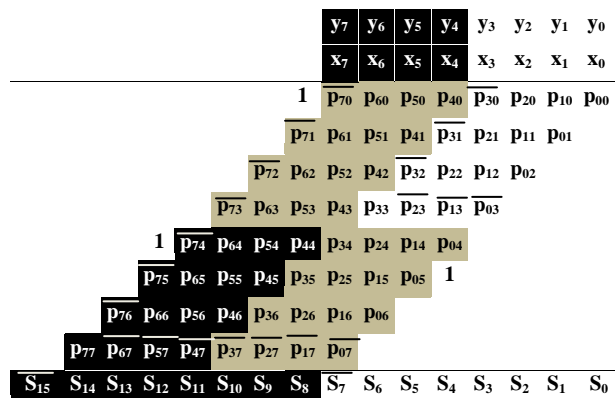


Fig 4: Illustration of a Signed 8-bit Multiplication, using the Baugh-Wooley Algorithm

Implementation of twin precision Baugh-Wooley algorithm for 8-bits signed multiplier is shown in Fig. 5. Three important things that differentiates unsigned multiplier with signed multiplier is

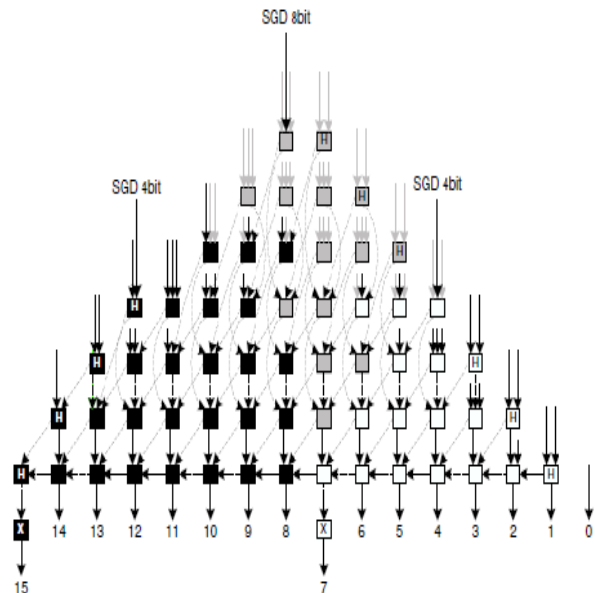


Fig 5: Block Diagram of a Signed 8-bit or Two 4-bit Multiplication, using the Baugh-Wooley Algorithm

(i) In order to fit extra sign bit needed the half adder in column 4 and 8 is replaced with Fulladders. (ii) There is no half adder for sign bit of 4-bit multiplication that can be changed in column 12, Hence added an Extra Half adder (iii) At the output of column 7 and 15 finally XOR gate had been added for inversion. it is easy to compute unsigned multiplication due to the simplicity of bandwidth implementation. While using control signals none of the partial products are negated and sign bits are set to zero.

In this Paper Fast Fourier transform is implemented using twin precision technique along with Baugh-Wooley algorithm because it has efficient Bandwidth utilization and low power consumption

compared with Booth algorithm and Modified Booth Algorithm.

IV. SIMULATION RESULTS

Here the simulation results of Multiplier using Baugh-Wooley algorithm with twin precision technique is shown in Fig 6.

The main aim of the technique is to utilize bandwidth efficiently and to increase the speed of operation. Depending upon the input operands the high order bits of the multiplier reduces the speed of operation. For large operand values by making the control signal (cntrl=0) multiplier acts as a single 8-bit multiplier and its simulation result of 8-bit multiplier is shown in Fig 6.

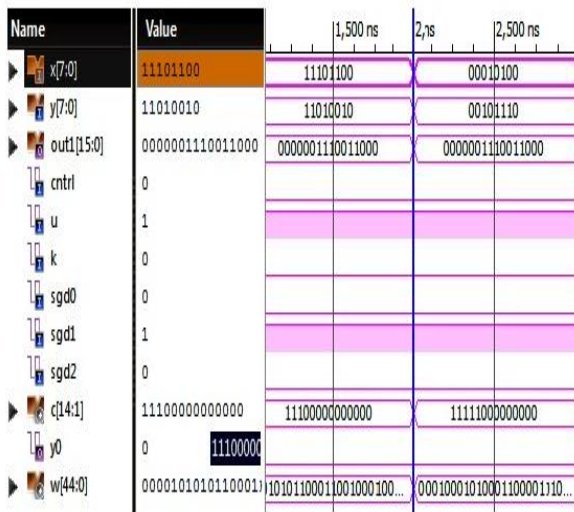


Fig 6: Simulation Results of 8-bit Multiplier

The Higher order bits of the multiplier is not using for small operand multiplication by making control signal (cntrl=1) multiplier splits into two parts at a time two 4-bit multipliers can perform and the simulation result of two 4-bit multiplier is shown in Fig. 7.

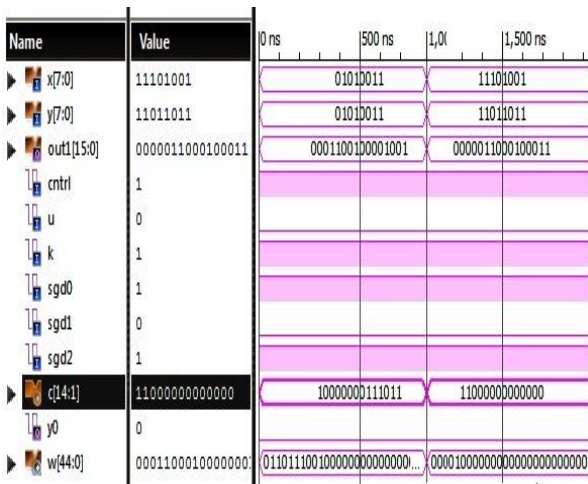


Fig 7: Simulation Results of two 4-bit multiplier.

If multiplicand = 01010011, multiplier=01010011 and cntrl=0 it acts like a single 8-bit multiplier and generates 16-bit output as 0001101011101001 as shown in Table 1. If cntrl=1 it splits into two 4-bit multiplier and generates output as 0001100100001001.

**TABLE I
BANDWIDTH MULTIPLIER OUTPUT USING CNTRL BIT**

S.No	8-Bit Input data		Cntrl	16-bit output data
1	Multiplicand	01010011	1	0001100100001001
	Multiplier	01010011		
2	Multiplicand	01010011	0	0001101011101001
	Multiplier	01010011		

Here the simulation result of Fast Fourier transform using Baugh-Wooley Algorithm with Twin Precision technique is shown in Fig. 8. The utilization of bandwidth and speed of operation is efficient by using this technique when compared with booth multiplier and modified booth multiplier.



Fig 8: Simulation Results of Fast Fourier Transform using Baugh-Wooley Algorithm and Twin Precision technique.

V. CONCLUSION

Flexible architectural solutions were obtained by twin-precision technique and variations in bit width of operand decreases power dissipation and increases throughput of FFT. Here twin precision technique with Baugh-Wooley algorithm is used to implement

FFT. Minor modifications are needed in computation of twin-precision technique due to simplicity of this algorithm. Finally efficient signed and unsigned multiplications are utilized for the computation of FFT.

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