Design and Comparison of Various Low Power n-T SRAM Cells

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Abstract—

Modern ICs are enormously complicated due to decrease in device size and increase in chip density involving several millions of transistors per chip. The rules for what can and cannot be manufactured leads to a tremendous increase in complexity due to the amount of power dissipation are increased. For high-speed memory applications such as cache, a SRAM is often used. Power consumption is the key parameter for an SRAM memory design (SRAM). In this paper an effort is made to design 6T, 7T, 8T, 9T, 10T, 11T SRAM cells using Cadence 180nm technology. The average power consumption of these SRAM cells are calculated and compared.

Keywords - *Modern IC, Cache, SRAM cells, average power consumption, cadence 180nm technology.*

I. INTRODUCTION

As increase of VLSI industries, the demand for portable device size and battery operated embedded system are increasing with greater scale. Cache memory is the basic memory part which play vital role in executing of data, cache occupies 60%-70% of chip area. Due to rapid integration power consumption of the chip increases, hence degrade the speed of microprocessors. As million of transistor is fabricating on single chip failure rate also increase and degradation of performance take place so industry is working to create the circuit consume low power and high speed memory to keep up with the advancement of VLSI circuit .A new SRAM with n-T structure have been proposed to full fill the demand of low power and high speed.

More than half of the transistors in today's high performance microprocessors are devoted to cache memories and this ratio are expected to increase in the foreseeable future. Typically, SRAM (Static Random Access Memory) is the choice for embedded memories as SRAM is robust to the noisy environment in such chips. As a result, considerable attention has been paid to the design of low-power, high-performance SRAMs since they are a critical component in both hand-held devices and high-performance processors. By incorporating an SRAM that is the correct size for the system requirements, the system can avoid using unnecessary memory cells. This leads to improvements in area, speed, and power. Therefore, depending on the application's need, an appropriate SRAM size should be used. In this paper we compare the different structure of SRAM cell and calculated the average power consumption of each SRAM cell to enhance the performance of SRAM cell and increase the speed of the microprocessor.

II. VARIOUS STRUCTURES OF SRAM CELLS

SRAM cell design depend upon the speed and size of the cell, SRAM cell should be sized as small as possible so large No of transistor can be fabricated on single chip, and we achieve high density in memory design.

A. 6T SRAM

The 6T SRAM cell as shown in Figure1, consist of six transistors. That includes two back to back cascaded inverters, and two NMOS pass transistor for access. A 6T SRAM cell has high speed, better noise immunity, and lesser area than other SRAM cell.

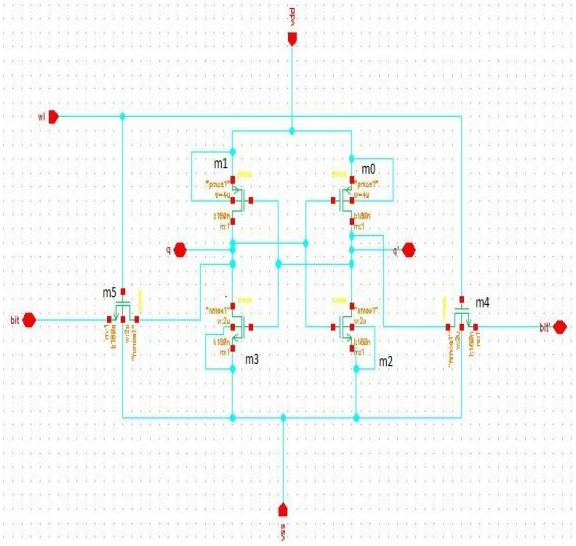

Figure 1:Schematic of 6T SRAM cell

Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**.[3] Two additional access transistors m5 and m4 serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (wl) which controls the two access transistors m5 and m4 which in turn, control whether the cell should be connected to the bit lines: bl and bl'. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, but both the

signal and its inverse are typically provided in order to improve noise margins. The disadvantages of 6T SRAM cell is ,as the transistor size shrinks, the leakage power increases which in turn increases the power dissipation of the memory cell .

SRAM Cell Operation - Operation of the SRAM Cell can be categorised into three different state: Standby Mode in which circuit is in ideal mode, Read Mode when data has to be extracted, Write Mode when mode data has to be updated. The working of different mode can be explained:

Standby: If the word line is not asserted, the access transistors M4 and M5 disconnect the cell from the bit lines. The two cross coupled inverters formed by M0 – M3 will continue to reinforce each other as long as they are connected to the supply.

Reading: Assume that the value of memory cell is 1 stored at "q". The read operation is started when the word line wl is asserted enabling both access transistors m4 and m5. Values stored in q and q' are transferred to the bit lines bl and bl'. By leaving bl at its precharged value the bl' is discharged through m2 and m4 to logical 0. On bl side the transistors m1 and m5 pulls the bit line bl towards Vdd to logical 1.

Now assume that the value present in memory cell is 0 stored at q. When wl is asserted enabling both the access transistors m4 and m5. The value stored at q and q' are transferred to bit lines bl and bl'. The sense amplifiers are used to read the values from bit lines bl and bl'.

Writing: The write operation begins by applying the value to be written to the bit lines bl and bl'. If we wish to write a 0 value, we would apply a 0 to the bit lines, i.e. setting bl' to 1 and bl to 0. A 1 is written by inverting the values of the bit lines. wl is then asserted and the value that is to be stored is latched in.

B. 7T SRAM

7T SRAM cell as shown in figure 2 consists of 7 transistors. [3][4] It also consists two back to back cascaded inverter, and two NMOS pass transistor for access to the cell. This 7T SRAM cell design is similar to 6T SRAM cell, in place of vdd of the cross coupled inverter one nmos transistor is placed. This extra nmos is placed to pull the bit lines to high i.e., vdd such that the read and write operation and average power consumption are improved compared to 6T SRAM cell.

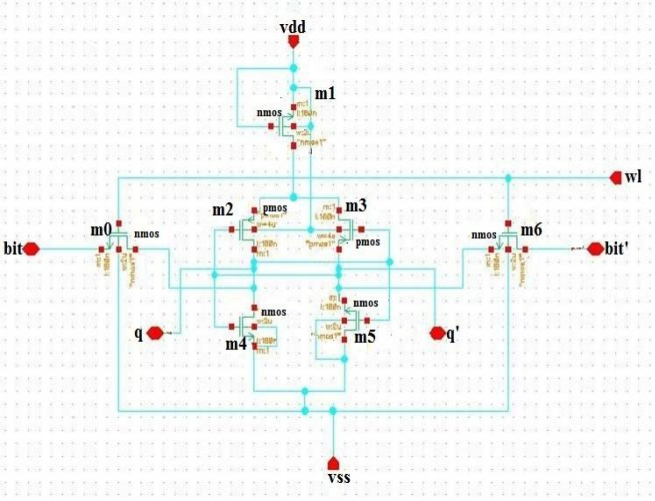

Figure 2: Schematic of 7T SRAM Cell

C. 8T SRAM

The 8T SRAM cell as shown in figure 3 consists of 8 transistors. It consists of two cross-coupled inverters made up of transistors m1, m5 and m2, m4. The transistors m0, m3 are access transistors. The two additional NMOS transistors m6 and m7, one each in pull down path of cross coupled inverters are used to achieve leakage power reduction. The access transistors are connected to the word line "wl" at their respective gate terminals, and the bit-lines bl and bl' at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. Internally, the cell holds the stored value on one node and its complement on the other node. The node q holds the stored value while other node q' holds its complement. The two complementary bit lines are used to improve speed of write and read operations. Though the number of transistors are increased in the design compared to conventional 6T SRAM, power consumption is reduced considerably.[11]

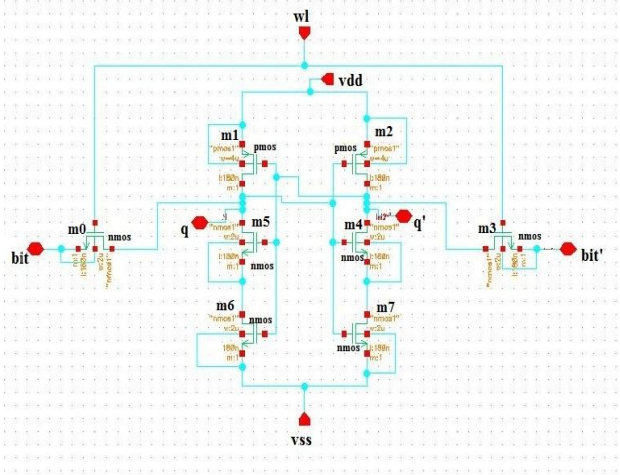

Figure 3: Schematic of 8T SRAM cell.

D. 9T SRAM

9T SRAM cell enhances the data stability and reduces leakage power consumption. The

schematic of the 9T SRAM cell is shown in Figure 4. The upper sub-circuit of the 9T memory cell is essentially a 6T SRAM cell composed of m0, m1, m2, m3, m4, m5. The two write access transistors m4 and m5 are controlled by a write signal (WL). The data is stored within this upper memory sub-circuit at q and q' nodes. The lower sub-circuit of the new cell is composed of the bit-line access transistors m6 and m7 and the read access transistor m8.[7]

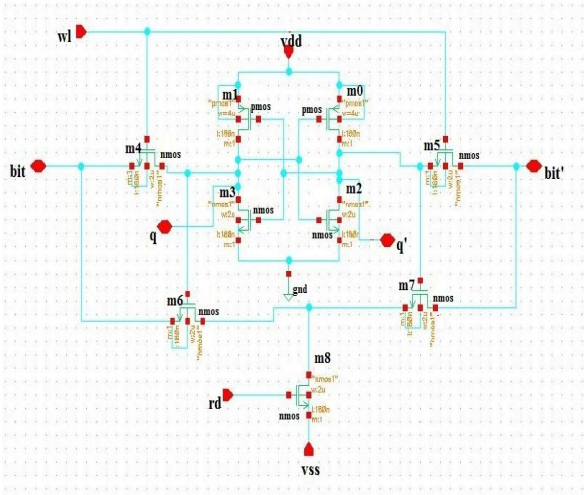

Figure 4: Schematic of 9T SRAM cell

E. 10 T SRAM

In the conventional 6T SRAM cell, read and write operations take place through same access transistors, and hence both read and write failure cannot be avoided simultaneously due to conflicting requirements of transistor sizing. Figure.5 shows schematic of 10T SRAM cell. It consists of separate path for read and write operations and allows independent tuning of read and write stability. [13]

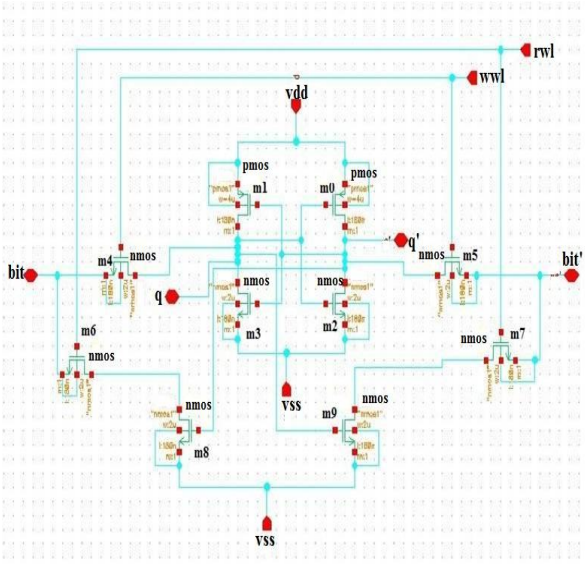

Figure 5: Schematic of 10T SRAMcell

This 10T circuit utilizes the cross-coupled inverters composed of m0, m1, m2, m3 similar to conventional 6T SRAM cell for write operation. The two write access transistors m4 and m5 are controlled by write word line (WWL). Whereas, the additional transistors m8 and m9 are controlled by the data stored in the cell and the two read access transistors m6 and m7 are controlled by a separate read signal (RWL). In the hold mode, WWL and RWL both are kept at ground that reduces the circuit to simple cross-coupled inverters.

F. 11T SRAM

The architecture of 11-T SRAM cell is shown in Figure 6. The upper part of the circuit is essentially 6T SRAM cell and is used to perform write operation. Transistors M8, M9 and M11 are used for reading the content of the storage nodes q and q'. Read access is single ended and occurs on the separate bitline "rbl". The read wordline "rwl" is distinct from the write wordline "wl". To store the data at the storage nodes "q" and q', the read wordline "rwl" is set to be low.[10]

Transistors M7 and M10 are used to decouple the storage nodes q and q' from read bitline "rbl" during write operation and standby mode so that proposed cell has distinct write and read ports. Due to separate read and write circuits, the previously stored data remains intact in the cell during next write operation as long as rwl=0. The switching behaviour of the transistors M8 and M9 is decided by the voltage at the storage nodes.

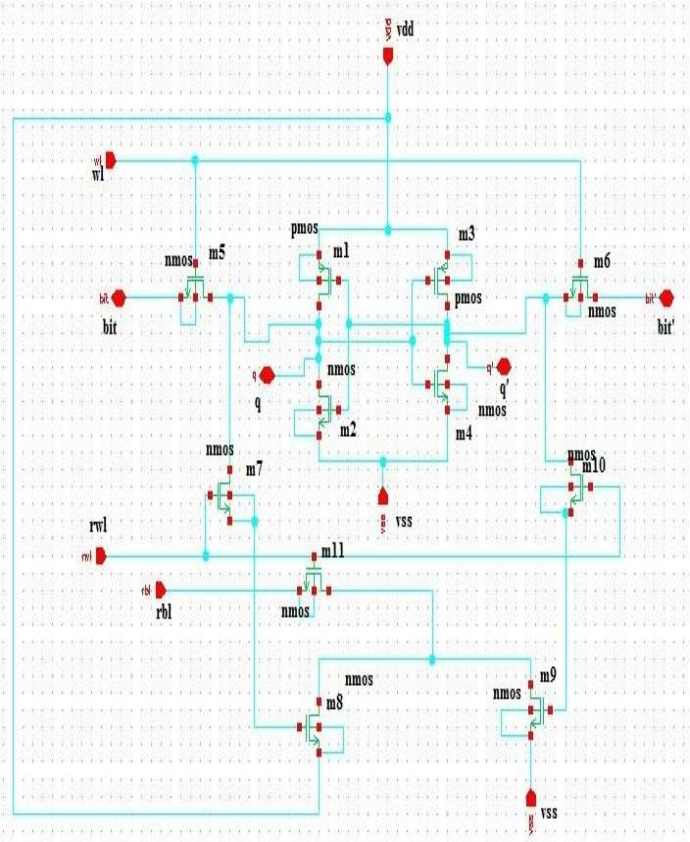

Figure 6: Schematic of 11T SRAM cell

III.PERIPHERAL CIRCUITS

Peripheral circuits are used to charge both bit lines(bl) and bit line bar(bl') to vdd and to discharge the bit line and bit line bar to ground. They are also used to sense and amplify the output. A peripheral circuit consists of pre-charge circuit, write circuit and sense amplifier which are shown below.

A. Precharge Circuit

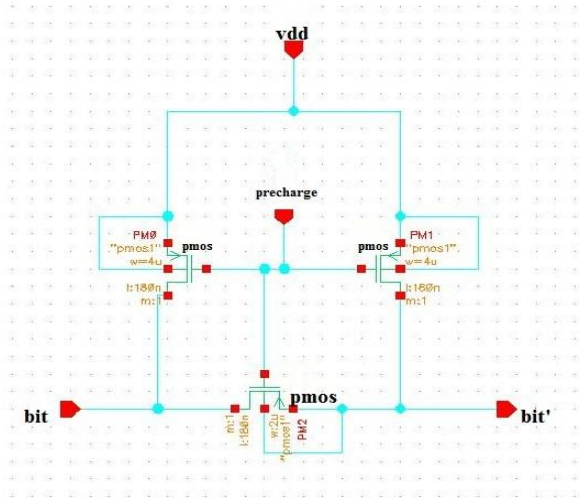

Figure 7: Schematic of Precharge Circuit

When pre_ch is logic 0,then both Bit and Bit' are charged to VDD, whenever the SRAM cell is in inactive state. In active a state, pre_ch is disabled by making it high. The schematic of pre-charge circuit is shown in figure 6.

B. Write Circuit

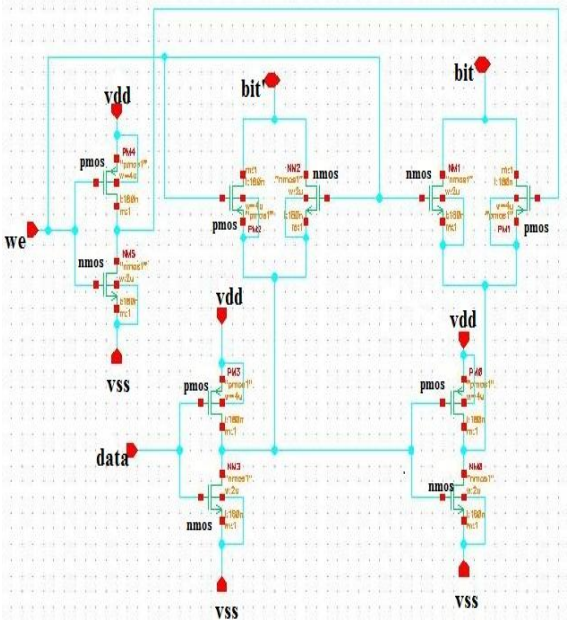

Figure 7:Schematic of Write Circuit

Whenever "WE" is enabled, data is written into the SRAM memory cell. If it is deactivated, then memory cell retains the previously stored data. The figure.7 shows the schematic of write circuit.

C. Sense Amplifier

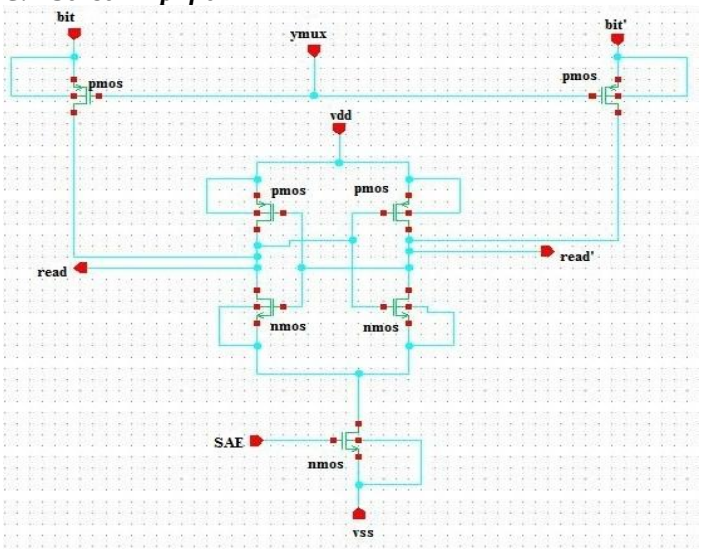

Figure 8: Schematic of Sense Amplifier Circuit

Sense amplifiers are used to sense which line is being pulled down and perform the read operation of the stored data. Read and Read' indicate the data stored and its complement during the read operation. The figure 8 shows the schematic of sense amplifier circuit.

IV. SRAM MEMORY SYSTEM FOR WRITING AND READING A SINGLE BIT OF DATA:

The whole memory system of 6T SRAM is shown in figure 9.To access the SRAM cell, extra circuitry is needed. They are,

- Precharge circuit
- Write circuit
- Sense amplifier circuit

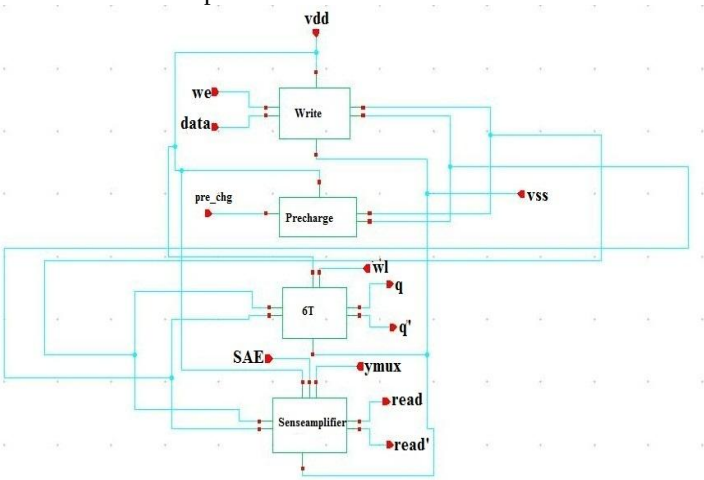

Figure 9: Schematic of 6T SRAM with Peripherals

Figure 9 shows the 6T SRAM connected to other peripherals such as pre-charge, write circuit and sense amplifier.

When data to be written into the SRAM cell, pre-charge and Word line enable are made high. SAE(sense amplifier Enable) is made low. Data to be written is given at data line which is stored into SRAM cell and can be seen at output "Q". Whenever the data to be need to read from the SRAM cell, SAE is enabled and output is read at read and read'.

V. SIMULATION AND RESULTS

Cadence Virtuoso Schematic Editor is used for circuit design and the circuit is analysed and verified for functionality through simulations using Cadence Virtuoso Spectre tool. The total power measurement is done using Cadence Virtuoso ADE Visualization and Analysis XL Browser and XL Calculator.

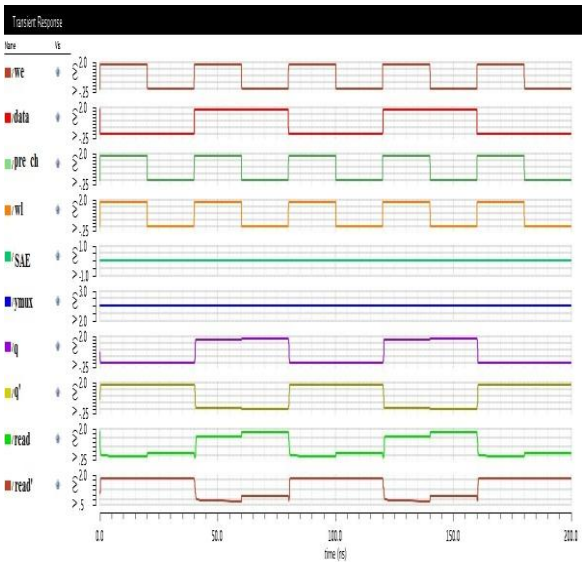

Figure 10: Simulation of 6T SRAMcell

Figure 10 shows the transient analysis of 6T SRAM cell. The run time for simulation is given as 200nm When 'we' is enable and when 'pre_ch' is enable then data is written in to the cell i.e., q and q'. If data =0 then q=0 and q'=1. If data=1 then q=1 and q'=0.

The data written into q and q'can be read with the help of sense amplifier. When SAE is enabled and ymux is disabled, the data in q and q' are read from read and read' lines. When q=0 and q'=1 then read=0 and read'=1.When q=1 and q'=0 then read=1 and read'=0.

Sl.no	1-bit SRAM cell	Average power consumption(u watt)
1	6T	$33.87e^{-6}$
2	7T	$34.76e^{-6}$
3	8T	$9.127e^{-6}$
4	9T	$6.538e^{-3}$
5	10T	$15.64e^{-6}$
6	11T	$4.229e^{-6}$

VI. CONCLUSION

The design of SRAM memory cells to be a challenging and valuable learning experience. It gave us the opportunity to learn Cadence Virtuoso tools used in designing of different SRAM cells using 180nm technology. The static RAM is very widely used in CMOS systems. In this paper we have simulated and analysed the performance of 6T SRAM cell at 180nm technology. Same as 6T SRAM we can design other SRAM topologies like 7T, 8T,9T, 10T, 11T with peripherals and simulated. The average power consumption of these SRAM can be calculated and analysed.

The comparative results are given in table 1. Which shows that the average power consumption of different SRAM cells. From the table.1 we can analyse that 8T, 10T, 11T SRAM cells has lower average power consumption compared to 6T, 7T, 9T SRAM cells. For power constrained projects like space exploration and satellites the SRAM cell which consumes minimum power must be used.

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