Schematic Design and Layout of Flipflop using CMOS Technology

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Abstract-

In this paper the work is done on low power and high speed design of flipflop using CMOS technology on different nanoscale technologies i.e. 90 nm, 65nm and 45 nm. The transistor used small area and low power consumption. By decreasing the geometrical feature size of the transistors we can achieve the low power consumption and high speed of integrated circuit in VLSI design. When the technology size decreases in the result of this the leakage power increases which is reduced by type of CMOS technology. The comparisons are held TSPC D-Flipflop and Multi threshold CMOS technology and among the power consumption propagation delay and power dissipation product. The work is carried out with the help of tanner EDA tool.

Keywords- *CMOS technology, Nanoscale technology, VLSI design, Tanner EDA tool.*

I. INTRODUCTION

For designing IC chip the circuit consist of many numbers of logic gates which are integrated inside. The minimization of power dissipation in any circuit has always been a big challenge for any circuit designer. There are many related works which are already carried out by different groups with different techniques like bipolar junction transistor, CMOS technology, BiCMOS technology etc. Designers are able to work on more transistors onto the same die because of the shorter size of the CMOS as per Moore's law.

Latches and Flipflops are the sequential circuits that stores 1 and 0 state called logic states. Latches works on level triggered while flip flops works on edge triggred. A Flipflop is a bistable circuit which give the output in response to a reference pulse. The data stored in flip flops on the rising and falling edge of the clock signal is applied as the inputs to other sequential circuits. Those flip flops which stores data on both the rising and falling of the clock signal are termed as double edge triggered flipflops and those flip flops that stores data either on the rising or falling edge are known single edge triggered flipflops.

II. DESIGN ANALYSIS

Basically there are three source of power dissipation in CMOS digital circuits. The first one is due to signal transistor, the second one is due to the leakage current and the last one is from short circuit current which flows directly from supply (Vdd) terminal to the ground. High leakage current plays the most significant role of contributor in the power dissipation of CMOS circuit as the threshold voltage, gate oxide thickness and channel length are reduced.

In this paper the work is done on Multithreshold CMOS technology. There are many technique proposed for flip flop and latches. In figure1 shows 11 transistor TSPC D flipflop with positive edge triggered which later on reduces to 8 transistors and further reduced to 6 transistors in which 4 NMOS and 2 PMOS were used. The schematic design of TSPC filp flop is shown in figure 1 in which 5 transistors where 3 NMOS and 2 PMOS are used.

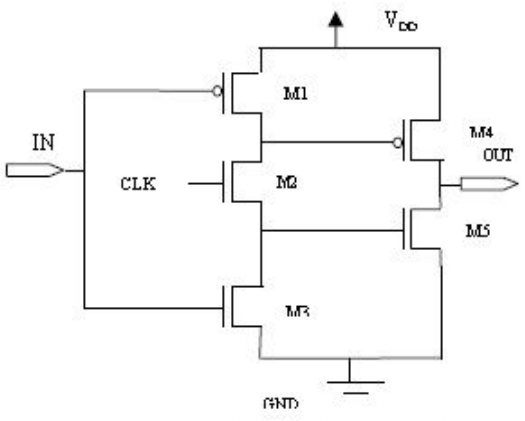

Figure 1: TSPC D Flipflop with 5 Transistor

CLK	INP	M1	M2	M3	M4	M5	OUT
↑	0	ON	ON	OFF	OFF	ON	0
↑	1	OFF	ON	ON	ON	OFF	1
↓	0	ON	OFF	OFF	OFF	OFF	0
↓	1	OFF	OFF	ON	OFF	OFF	0

Table 1: Truth Table of D Flipflop

TSPC D Flipflop turns into a Multithreshold CMOS technology when 1 PMOS transistor and 1NMOS transistor are connected to the circuit of TSPC D Flipflop which is shown in Figure2.The Multi Threshold CMOS Technique is very important Low Power Technique which reduces the Leakage Power effectively. This technique works in two modes, Mode 1 and Mode 1: High Threshold Mode and Mode 2: Low Threshold Mode.. Mode 1 reduces the leakage power and Mode 2 improves the speed of the system.

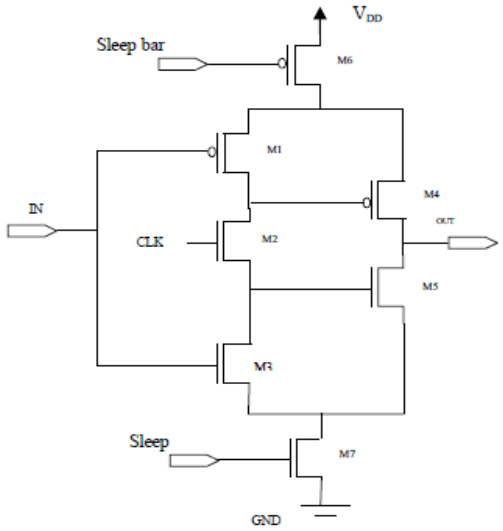

Figure 2: Multi Threshold CMOS

CLK	IN	Sleep	Sleep bar	M1	M2	M3	M4	M5	M6	M7	OUT
↑	0	0	1	ON	ON	OFF	OFF	ON	ON	OFF	0
↑	0	1	0	ON	ON	OFF	OFF	OFF	OFF	ON	0
↑	1	0	1	OFF	ON	ON	ON	OFF	ON	OFF	1
↑	1	1	0	OFF	ON	ON	ON	OFF	OFF	ON	1
↓	0	0	1	ON	OFF	OFF	OFF	OFF	ON	OFF	0
↓	0	1	0	ON	OFF	OFF	OFF	OFF	OFF	ON	0
↓	1	0	1	OFF	OFF	ON	OFF	OFF	ON	OFF	0
↓	1	1	0	OFF	OFF	ON	ON	OFF	OFF	ON	0

Table 2:Truth Table of Multi Threshold CMOS

III. RESULT

The performance analysis of the D Flipflop and latches are presented there. T Spice and S-Edit are used to carryout the work for different technologies like 90nm, 65nm and 45nm technologies.

Parameter	90 nm		65 nm		45 nm	
	0.5V	1V	0.5 V	1V	0.5V	1V
Power Dissipation(µW)	0.2435	1.2847	0.2293	1.3122	0.1377	1.9015
Delay(nS)	2.9316	0.2365	0.1963	0.02867	0.6414	0.0282
Power Delay Product(fJ)	0.7138	0.0304	0.0450 2	0.03762	0.8831	0.0537

Table 1: Power Delay Comparison for TSPC Based D Flipflop

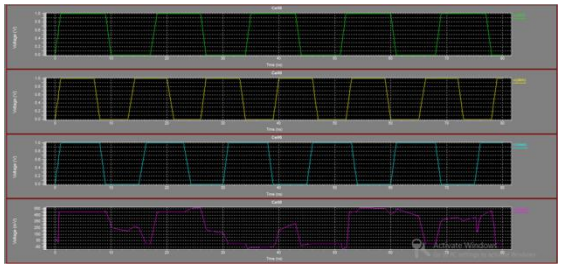

Figure 3 :Multithreshold CMOS Based D Flipflop on 90 nm Technology at 1V

The figure 3, 4 & 5 shows the output results of our proposed designed Multithreshold CMOS baesd D flip flop on 90nm, 65nm and 45 nm respectively. All the figures contain the Clk, sleep, Vin, Sleep bar and Vout waveforms. The voltage range for the Vin had been checked and verified by providing pulse waveform whose amplitude is 1v, or 0.5v. The clock pulse is designated by clk pulse whose amplitude is also varied from 1v or 0.5v (depends on the voltage range of the entire circuit.)There are two additional signal has been provided to reduce the power dissipation of the circuit. These pulse trains are named as sleep and sleep bar. The vin signal is shown by the green color, the yellow color depicts the clk signal, the blue color shows the waveforms for the sleep signal and at last the generated output pulse i.e. Vout has been shown by purple color.

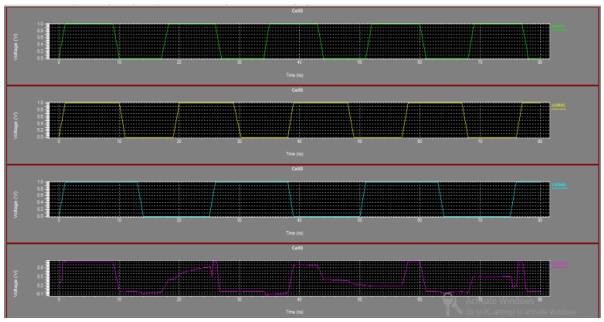

Figure 4: Multithreshold CMOS based D Flip flop on 65 nm Technology at 1V

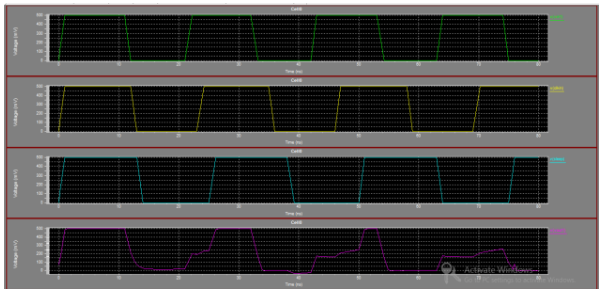

Figure 5: Multithreshold CMOS Based D Flip Flop on 45 nm Technology at 1V

The comparison between different technologies and different scaled supply voltages is shown in Table 1 for TSPC D Flipflop and Table 2 for Multithreshold CMOS D Flipflop respectively.

Parameter	90 nm		65 nm		45 nm	
	0.5V	1V	0.5V	1V	0.5V	1V
Power Dissipation(µW)	0.1900	1.3322	0.2147	1.3380	0.1587	0.83474
Delay(nS)	0.2359	0.1045	0.2471	1.1564	0.2675	0.1065
Power Delay Product(fJ)	0.0448	0.1392	0.0537	1.5472	0.0425	0.0892

Table 2: Power Delay Comparison for MTCMOS Based D Flipflop

The table 1 & 2 shows the various parameters e.g. Power dissipation, Delay and power delay product for TSPC and MTCMOS on various nanometer technology scales. As the table shows the variation in the delay and power dissipation while we are changing the technology file(s) at different various voltage levels.

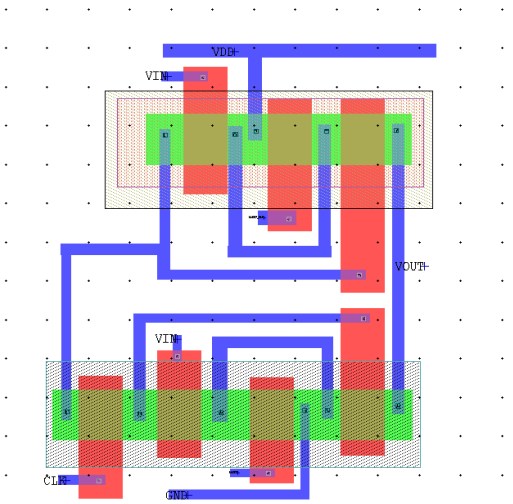

Figure 6: Layout of Multi Threshold based D Flipflop

The figure 6 shows the layout diagram of the Multi threshold D flip flop by using in which all metal lines are drawn in Blue colors, all active layers are by green color and the polysilicon layers are drawn by the Red color for active region. The complete layout has been carried out on Tanner L-Edit tool.

IV. CONCLUSION

We had successfully designed and simulated our CMOS based D flip flop using TANNER EDA tool. In our design we had obtained the power dissipation lesser than we referred. From the tables 1 & 2 listed above, it is clear that the power dissipation decreases and propagation delay increases as the technology is scaled down. Also as the supply voltage is scaled down, both the power dissipation and propagation delay decrease. When compared with TSPC based D Flip-Flop, the Multi threshold CMOS based D Flip-Flop has advantage of low power delay product which is well suited for high performance applications.

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