Minimization of Power for the Design of an Optimal Flip Flop

Kahkashan Ali[#1], Tarana Afrin Chandel[#2]
[#1]M.TECH Student, [#2]Associate Professor, [1,2]Department of ECE, Integral University, Lucknow, INDIA

Abstract—

The power consumption is critically the most important factor in the modern VLSI circuits especially for those circuits which work on low-power applications. This designing aims in achieving optimum speed performance for low power and low noise simultaneously. In this paper basically we are dealing with the power minimization factor. In modern VLSI circuits power saving plays the vital role especially for the applications which runs on low power such as latches, flip-flops and also some logic components which plays a vital role in the functioning of digital system. The main factor is to reduce the power loss in both the flip-flops and clock distribution networks. In this paper we have made a comparison in terms of power loss, parasitic values and no. of transistors in some of the existing classes of the flip-flop. Each flip-flop have been analysed and the output is simulated using Tanner EDA tool in 180nm technology. The comparison made shows the best result between the working design of the flip-flop and the existing flip-flop designs.

Keywords:*Tanner EDA, clock distribution networks, Flip flops and Power minimization, pulse triggered.*

I. INTRODUCTION

Earlier in the designing of VLSI circuits the main concern for the VLSI designers were area, reliability, performance and cost. Power was given the secondary priority. But now-a-days power is given an equal preference with area and speed. Flip-flop is one of the most power consuming digital circuits used in many devices such as register file and many more. It consists of clock distribution networks and storage network which consumes more power almost 50% of total power consumed. Power dissipation in flip-flop and clock distribution networks must be reduced. Due to clock networks power consumption in highly synchronous system such as microprocessor is high. It is important to minimize power..This designing aims in achieving optimum speed performance for low power and low noise simultaneously. In this paperbasically we are dealing with the power minimization factor. In modern VLSI circuits power saving plays the vital role especially for the applications which runs on low power such as latches, flip-flops and also some logic components which plays a vital role in the functioning of digital system.

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II. EXISTING DESIGN

The basic elements for storing information or data are flip-flops and latches. The performance of flip-flop plays an important role in determining the synchronous circuit performance. Flip-flop is a bistablemultivibrator. It stores data in the form of binary digits (bit) of which one state represents “one” and other “zero”. Flip-flop can be either simple or clocked. Simple ones are called as latches while clocked one are termed as flip-flops. Flip-flops can be designed by the use of two NOR gates and NAND gates.These type of flip-flops are known to be SR flip-flop or SR latch. A Latch is an asynchronous circuit which means the output of latch depends on its input. The main difference between these two is that, for latches, output constantly gets change by the change in input (level triggered). Flip-flop on the other hand have their output change on the rising or falling edge of the clock pulse (edge triggered).

A P-FF consists of a pulse generator for generation of strobe signal and a latch for storing data. The pulse width of the triggering pulse generated on the transition edge of the clock signal is very narrow so latch acts as edge triggered flip-flop. The three existing pulse triggered flip-flop which are known are implicit data close to output, master hybrid latch level triggered flip-flop (MHLLTF), single ended conditional capture energy recovery (SECCER).

A. Implicit Pulse Triggered DCO Flip Flop

The figure[1] P-FF design is named as ip-DCO[9]. It consists of two bodies one is pulse generator and another one is semi dynamic latch design. It works on single phase clocking and alsooccupies small area. Inverter I5 and I6 are used to hold the latch whereas inverter I7 and I8 are used to hold the data. To generate a transparent window equal in the size to the delay by the inverters I1-I3 the pulse generator takes the complimentary and delayed skewed clock signal. In this flip flop a narrow pulse of short pulse width is generated by the clock signal and its complement clock signal during which the output follows the input.

In this design two practical problems arises. The one is during the rising edge where NMOS transistors N1 and N2 are turned on. Node x will discharged on every rising edge of the clock only if the data remains high which leads to large switching power. While the other problem is that node x controls two larger MOS transistors N5 and P2. Due to large

capacitive load to node x leads to the degradation of speed and power performance.

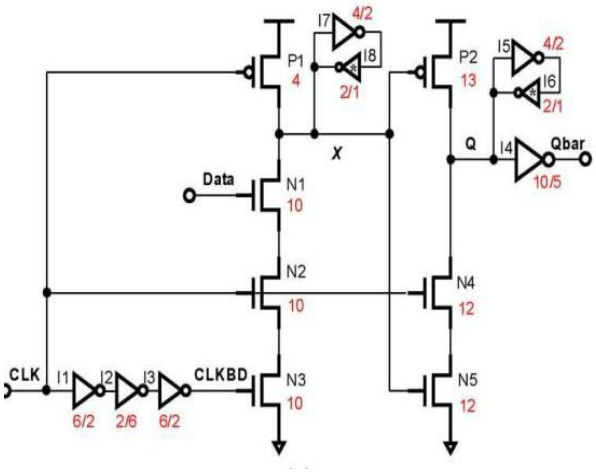


Figure 1: Implicit Data Close to Output flip flop

B. Master Hybrid Latch Level Triggered Flip Flop

Figure [2] shows an improved P-FF design named Master Hybrid Latch Level Triggered Flip Flop by employing a static latch structure [4], [8] and have less numbers of transistors and also consumes less power as compared to ip-DCO.

Node X is no longer pre-charged periodically by the clock signal. To maintain the node X level at high when Q is zero a weak pull-up transistor P1 which is controlled by the FF output signal Q is used. In this design unnecessary discharging problem at node X is eliminated. As node X is not pre-discharged the flip flop encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions. Another drawback of this MHLLTF design is that the node X become floating when the output and the input data both equal to "1" i,e., both Q and data are 1. If node X is drifted from 1 extra DC power starts emerging.

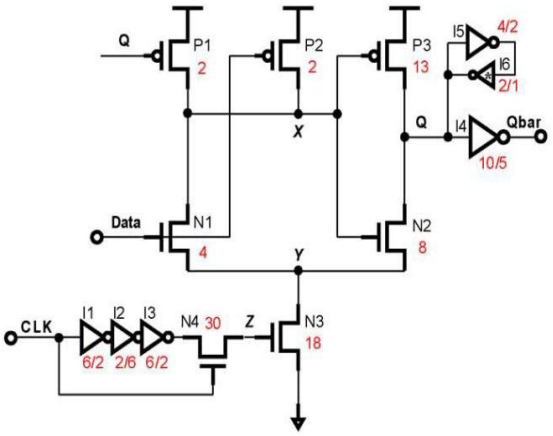


Figure 2. Master Hybrid Latch Level Triggered Flip Flop

C. Single Ended Conditional Capture Energy Recovery FF

It is the modified form of ip-DCO design which uses conditional discharged technique where the discharging path is controlled by eliminating the switching activity when the input stays in the stable high[4],[12]. In this design, I7 and I8 back to back inverters of the ip-DCO are replaced by a weak pull-up transistor P1 in addition with an inverter I2 to reduce the load capacitance of node X. Transistors N1 and N2 are connected in series which forms the discharging path. An extra NMOS transistor N3 is employed in order to eliminate the superfluous switching at node X. If the input data remains high no discharge occurs as N3 is controlled by Q_fdbk. The main limitation of this design occurs when the input data is "1" and node X discharged through four transistors in series, i.e., N1 through N4 while combating with P1 pull up transistor.

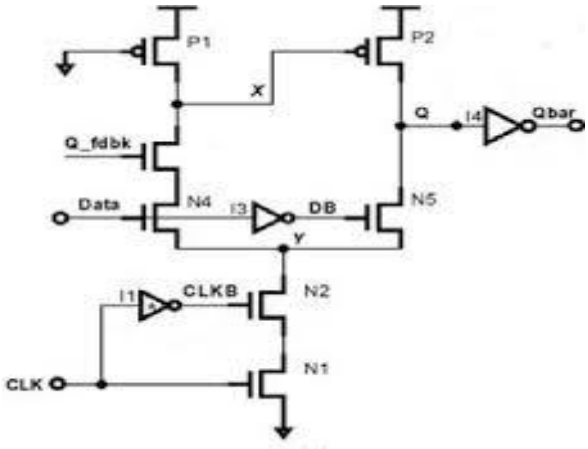


Figure 3:Single Ended Conditional Capture Energy Recovery FF

III. PROPOSED DESIGN

Figure [4] shows a refined low power P-FF with pulse control scheme adopts two steps to overcome the problem associated with existing P-FF designs. The first one is reducing the number of NMOS transistors which are stacked in the discharging path. And second one is to support the mechanism to conditionally enhance the strength of pull down when the input data is "1". The upper part of the latch design in fig.4 is similar to the output of the one employed in SCCER design fig.3[13].In this proposed design transistors N2 and N3 are in additionand forms a two input pass transistor logic (PTL) based on AND gate to control the discharge of N1 transistor. As the two inputs to the AND logic are mostly compliment except during the transition edge of the clock, the output node Z is kept at zero all most all the time.But when both the input signal are "0" which is during the falling edge of the clock temporary floating at the node Z is not harmed.

At the rising edge of the clock both transistor N2 and N3 are on and combine together to pass a weak logic at node Z which results in the turning on of N1 transistor by a time span which is defined by the inverter I1. Unlike the MHLLF design where the discharge control signal is control by a single transistor, conduction between two NMOS transistors (N2 and N3) leads to the speeding up the operation of pulse generation.

In this design number of stacked transistors along with the discharging path and the size of transistors N1-N5 is reduced. The longest discharging path in this design occurs when the input data is "1" while the Qbar output is "1".Transistor P3 is added to enhance the discharging. When node X is high transistor P3 is turned off. After the rising edge of the clock the delay inverter I1 drives node Z back to zero through N3 transistor to close the discharging path.

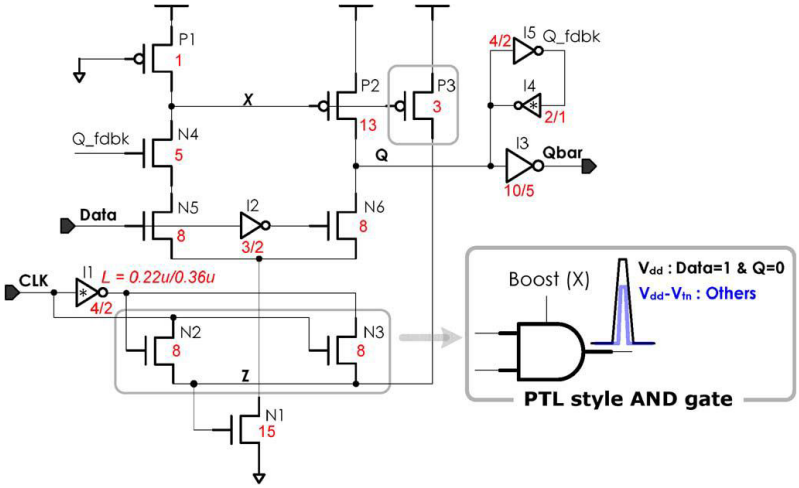
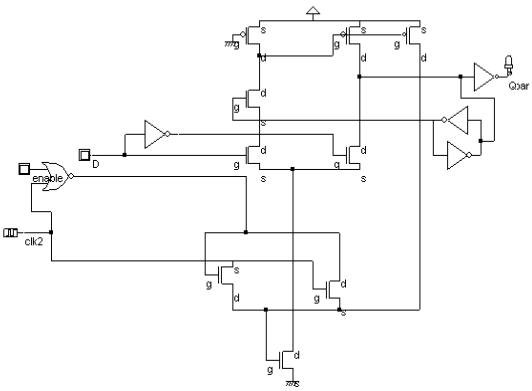


Figure 4. Schematic of Proposed P-FF

Clock gating technique is employed to reduce the power consumption to a minimum level which shown in fig.5. Instead of NOT gate NOR gate is used in the pulse generating part. The circuit works normally when the enable input is given O. When enable is 1 then the circuit is in clock gating mode which leads in the reduction of total power.

Figure 5. Schematic of Modified P-FF



IV. SIMULATION RESULT

The power consumption result is summarized in Table 1. The power consumption of enhanced pulse triggered flip flop is lowest due to shorter discharging path in compared to other existing flip flop[11]. The output of the flip flop is loaded with a capacitor having capacitance of 20pf. An extra capacitor of 3pf capacitance is also connected after the clock buffer.

The simulation result of all the existing and proposed flip flop mentioned above were obtained from Tanner EDA in 180 nm technology at room temperature. Simulation result of all the flip flops are shown below. Implicit pulse triggered data close to output (ip-DCO) consumed more power[10].

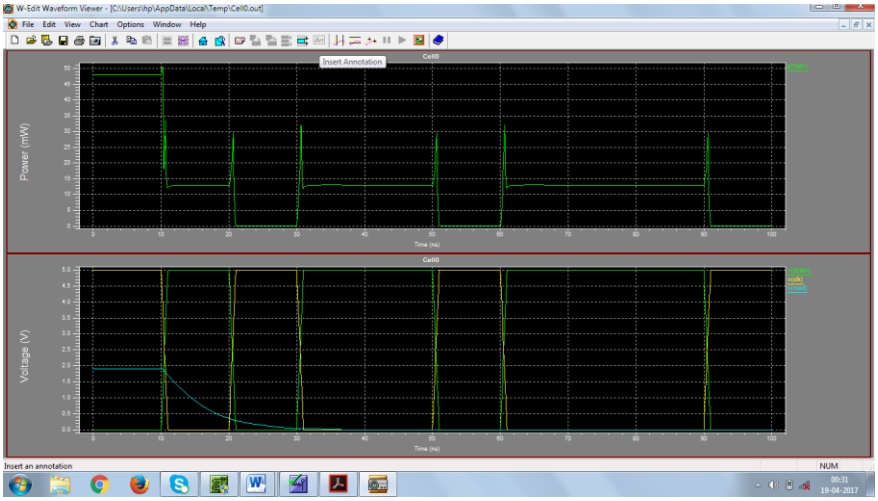


Figure 6. Simulation result for ip-DCO Design

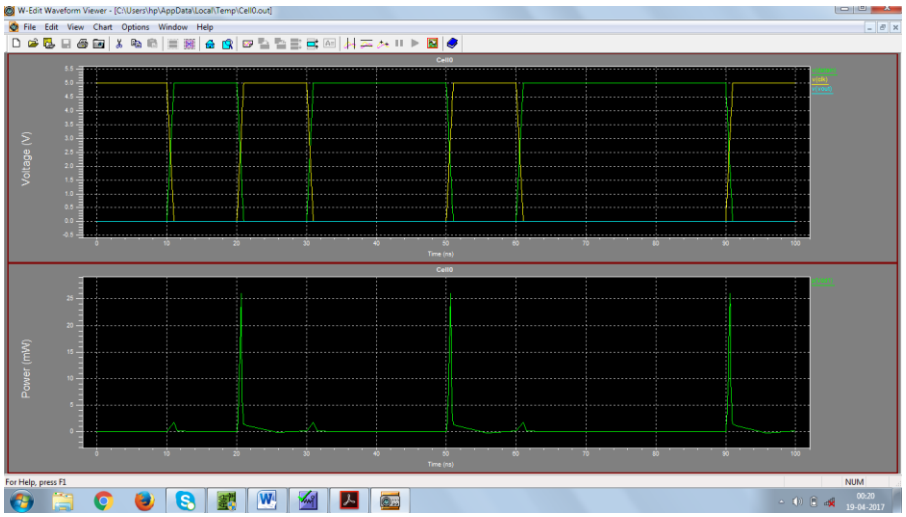


Figure 7. Simulation result for MHLLFF Design

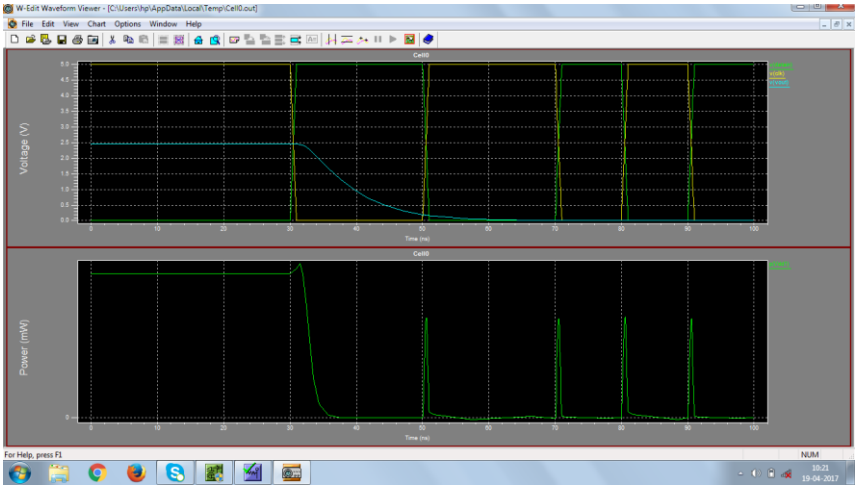


Figure 8. Simulation result for SCCER Design

On comparison, the proposed design have less power consumption

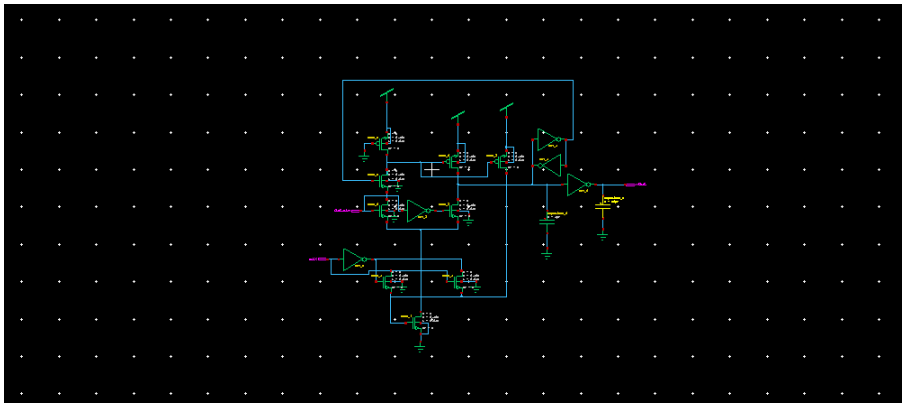


Figure 9. Proposed P-FF Design in Tanner EDA

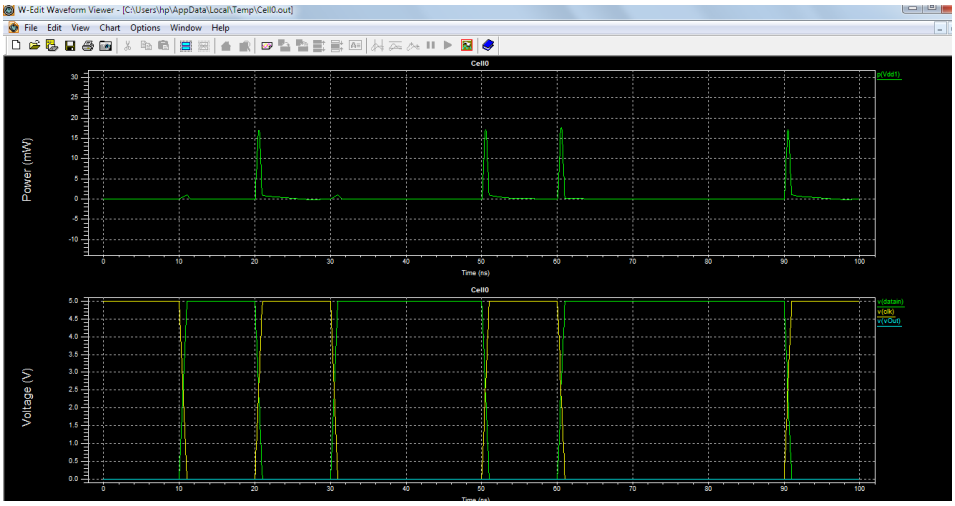


Figure 10. Simulation Result for Proposed P-FF Design

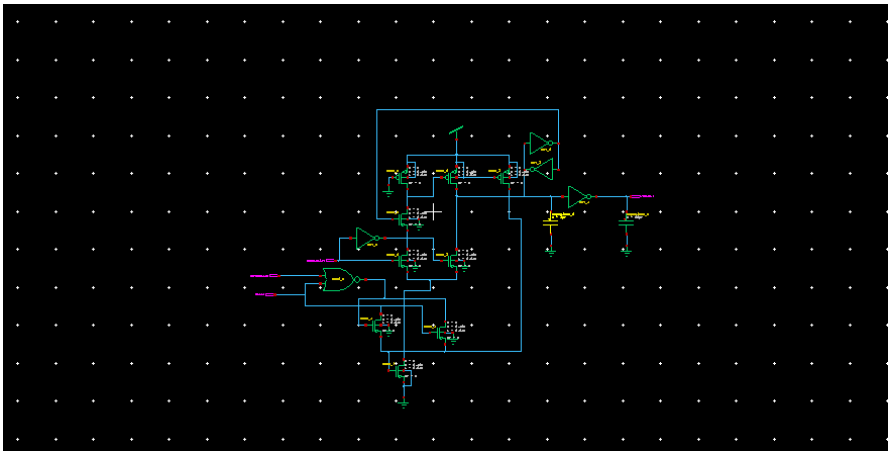


Figure 11. Modified P-FF Design in Tanner EDA

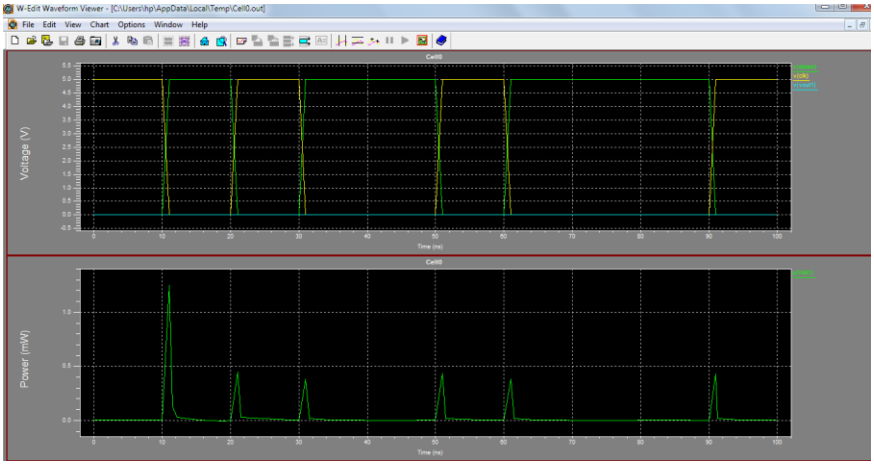


Figure 12. Simulation Result for Modified P-FF Design

TABLE I.FEATURE COMPARISON OF VARIOUS P-FF

Index	Ip-DCO	MHLLF	SCCER	Proposed P-FF
no.of transistors	23	19	19	19
power consumption (mW)	50	25	18	16
speed (sec)	8.40	8.05	7.69	7.14

V. CONCLUSION

In this paper, several flip flop designs such as ip-DCO, MHLLFF, SCCER are discussed. These designs were been designed in Tanner EDA tool of 180nm technology and result waveform of those such flip flop are also discussed. Comparing the result from the Table 1.it is clear that proposed P-FF performed better than other design. The proposed design used two new design steps. The first one is reducing the number of transistors stacked along the discharging path by adding a PTL-based AND logic. Another one is by supportinglimited improvement to the height and the width of the discharging pulse in such a way that the transistors size in the pulse generation circuit is kept minimum. Thus because of shorter discharging path the power consumption of the proposed P-FF is lowest.

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