Fault Tolerant Parallel Filter in Digital Communication Systems

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Abstract:
There are various types of filters are used by Digital signal processing (DSP) applications. In which digital parallel FIR filters are very widely used in numerous application. Over the years, many implementation techniques of digital FIR filter for DSP application has exploited the various practical difficulties such as low speed, high delay and above of all fault tolerance. Due to the VLSI complexity scaling, there are many complex systems that embed with many filters. The filters operations in those complex systems are usually parallel. As filters are the unit that comes in any type of communication system ranging from simple voice data to complex real-time data conversation. So it is then mandatory to implement some technique that shows the fault tolerance achieved in parallel filters. In this paper, we are going through various ideas that show that parallel filters can be protected using error correction codes (ECCs).

Keywords: *Error Correction Codes (ECC), Digital Signal Processing (DSP), Finite Impulse Response (FIR) Parallel FIR, Very Large Scale Integration (VLSI).*

I. INTRODUCTION

The demand for high performance and low power DSP is getting exponentially higher due to the bombardment of multimedia application such as automotive, medical and space applications where reliability is critical. And in those specific applications, the electronic circuits should have to provide some degree of fault tolerance. Although there are various other techniques that can be used to protect a circuit from errors. These errors can be removed ranging from modifications in the manufacturing process of the circuits for reducing the number of errors by adding redundancy bits at the logic or system level in order to ensure that these errors can do not affect the system functionality.
As in this paper, we are more focusing on Filter processing so it is mandatory to emphasize on the application area of Filters. The filters are the basic unit of any type of communication. In the basic communication system, the transmission of information/raw data is not always free from unwanted information bits or Noise. Thus it is very necessary for any communication systems to must have appropriate means for the finding and correction of errors in the information received over any communication channels. This paper deals with the study of the use of the various Error corrections coding scheme into Digital FIR Filter design.

II. ERROR CORRECTING CODES– AN OVERVIEW

During the Digital communication system, the information always travels through a medium. And the transformation of the information through this channel could not always be free from noise. Also, we know that in digitally encoded data, there is a series of symbols denoted generally in the terms of 0s and 1s. Suppose that we want to transmit the information that "There is no class on Monday". This information can be defined by 01101111, say, and transmitted over a channel where some unwanted data i.e. "noise" may be introduced. Noise means simply errors. By error, we mean that there is an unwanted change in data which is required to be correct for efficient and reliable reception of data.
The following diagram represents the communications channel.

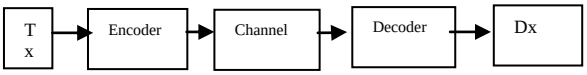

Fig 1: Basic Communication System

An error is a change or the mismatching takes place between the data unit sent by the transmitter and the data unit received by the receiver e.g. 10101010 sent by sender 10101011 received by the receiver. Here is an error of 1 bit. Error control refers to mechanisms to detect and correct errors that occur in the transmission of the frame. There are various techniques available for error control but the basis of all error detection and correction is the inclusion of redundant information.

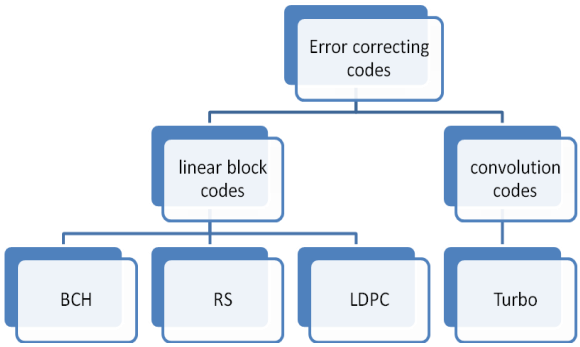

Fig2: Classification of Error Correcting Codes

III. PARALLEL FILTER

A discrete time filter follows the following equation:

$$y[n] = \sum_{l=0}^{\infty} x[n-l].h[l] \quad \text{.....(1)}$$

As stated in equation 1, x[n] is the input signal, y[n] is the output, and h[l] is the impulse response of the filter. The FILTERS has been categorized by this impulse response. For a FIR FILTER the response h[l] should be nonzero, only for a finite number of samples. Otherwise the filter is an infinite impulse response (IIR) filter. There are several structures to implement both FIR and IIR filters.

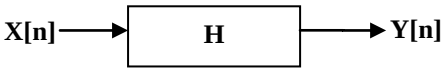

Fig 4: Digital Filter

We can also cascade n number of filters in a single communication systems.

IV. PROPOSED BLOCK DIAGRAM

In this work we are generating a Self error detector and corrector for FIR Filter. We are integrating two different topologies into a one solution. The proposed block diagram is shown in figure 3.

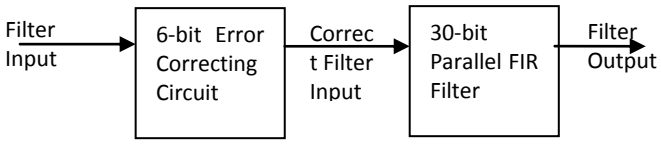

Fig 3: Proposed Block Diagram

The figure 3 shows the proposed schematic for our research work. The filter input first propagates through the error detection and correction circuit. Then the output from the error correcting detecting circuit will finally go to the parallel FIR filter.

V. SYNTHESIS & SIMULATION RESULTS

This section shows the various results obtained from the XILINX ISE Tool. The figure 6 & 7 shows the RTL view of our designed circuit i.e. Fault tolerant FIR Filter. As shown in the figure there are two inputs named as A , and error . The input A denotes the original message to be filter through the FIR filtration. While error signal are for stimulating the various number of errors.

Fig 5: RTL for Fault Tolerant FIR

The figure 5 shows only the input output ports which can be used as a physical interface for real world implementation. On the other hand figure 6 shows the internal structure of the Fault tolerant FIR filter. In this two separate block has been connected together to achieve the desired output.

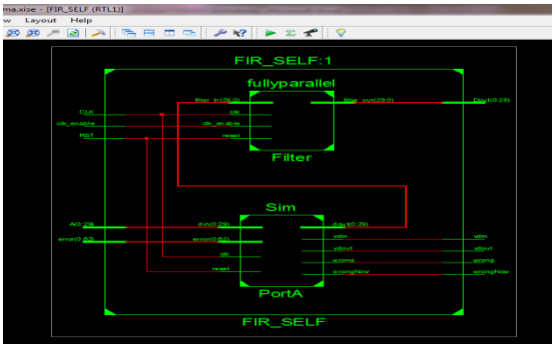

Fig 6: Internal RTL

The figures 7, 8 shows the cumulative result for the fault tolerant fir filter with different input conditions.

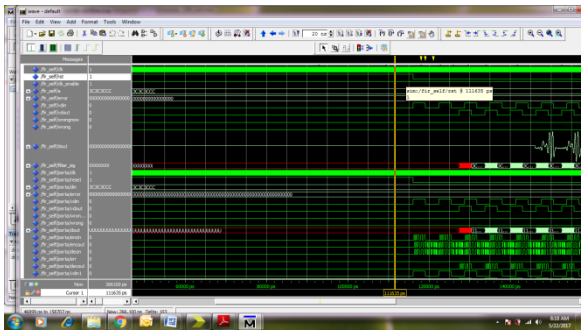

Fig 7: Simulation Result with initial Conditions.

The figure 7 shows the simulation results with initial conditions i.e. RST='1'. For initialization of all the registers, signals into its original states/values.

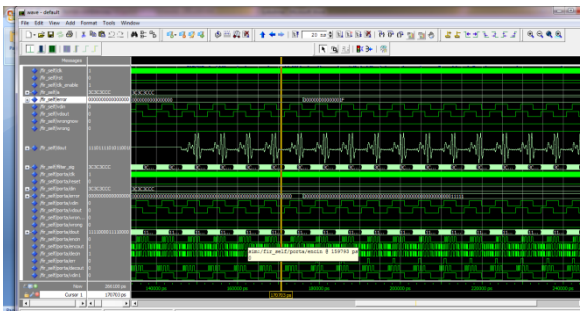

Fig 8: Simulation Results with 4 bit Error Correction

The figure 8 shows the result with stimulation of 4 bit error values through error signal. And we can easily observe that there is not a slight change in the output waveform.

VI. CONCLUSION

During our research, I observed from the literature discussed in the previous section that there are five primary criteria: area, speed, energy dissipation per bit, latency and error performance gap from the Shannon limit that must be considered in a BCH decoder design based on the application requirement. Current research has focused on the decoding algorithm, code design and VLSI implementation to meet the demands e.g. Less error, hardware reconfigurability, very high throughput and high efficiency. Although significant development on both construction and implementation of BCH codes has occurred in the past several years, the efficient realization of high-speed BCH decoders still remains a challenge for ever-increasing high-speed applications. Now we are going further to design our work i.e. using efficient coding scheme for fault-tolerant FIR Filter. Although FIR Filters can also be made using different structures i.e. Parallel, Serial and each design has the common feature i.e. the multiplication and shifting process which requires lots of hardware area, so we are planning to reduce the hardware area by using Distributed Arithmetic structure. Our work will do require the Xilinx ISE tool for implementation of FIR Filter with Fault tolerant features.

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