Efficient Multiplication by WTM using Compressors

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Abstract

This document produce the discussion of multiplication process by compressors. Multiplier gives a critical application in DSPs. This decides the reduction of power and improvement in the speed of operation in DSP systems. This use a key hardware blocks in various DSP systems. This architecture considers the various compressors among those are 3:2 and 7:2 . The compressors used in this discussion concentrates on minimizing delay, and area, which also quantifies the performance of the entire system. This discussion is about signed and unsigned multiplication with 3:2 and 7:2 compressors involved in WTM, this leads to the improvement in the performance of a multiplier with less area and power.

Key Words - *Compressor(3:2,7:2), WTM*.

I. INTRODUCTION

The main hardware key of in DSP system is multiplication. Multiplication process mainly involves two steps, first step is generation of the partial products and next step involves addition of those partial products. The partial product accumulation occurs where it is combined with final result. They will be trade-off with power, area and timing in digital circuits, by using the different Compressors multiplier performance will increase..

II. EXISTING MULTIPLIER:

3:2 Compressor is one of the existing system. The working principle is exactly similar to the full adder. Applying inputs are three inputs and producing outputs are two.

SUM=A'B+AB'
CARRY=AB+BC+CA

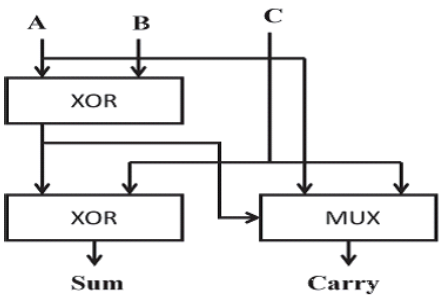

Fig1: 3:2 compressor.

WTM is effective hardware design of digital electronic circuit which multiplies two values of integers. Generally, multiplier has three different stages such as Partial products, addition of partial products, at last final addition. PP works similar to long hand multiplication, these binary values multiplied parallely with AND gates, it is faster and gives N^2 AND gates due to parallel multiplication it provides faster performance.

The outputs of partial products are added with digital compressors, this step takes long full adders (compressors) and addition are done simultaneously. Eventually addition is performed by adding the outputs of adders therefore this output of adders are the final product.

III. PROPOSED MULTIPLIER

7:2 compressor is the proposed system. This type of compressor utilizing the number of inputs are 7 and generating two outputs. one output is sum and another output is carry. The pervious lower block carries are also applied to the compressor, these structure generating carry outputs. Those are applied to the next higher block stages.

A. WTM Using 7:2 Compressors

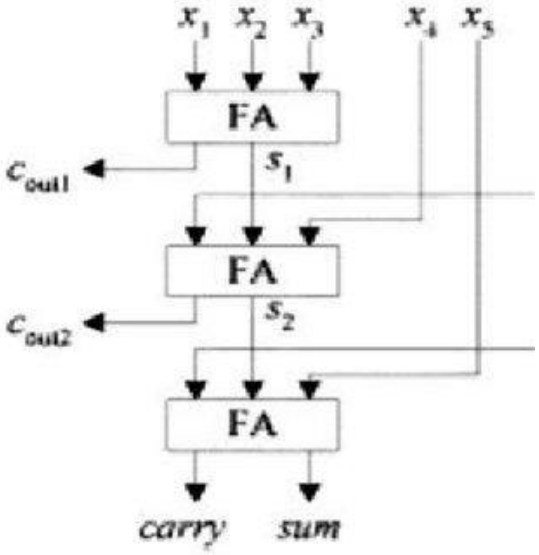

Fig2 : 7:2 Compressor

By considering the above compressor an implementation of the WTM and its PP stages are somewhat better than the 3:2 compressor. It can also prove that, 7:2 compressors is more efficient than the 3:2 compressors. Let us consider the 8 by 8 WTM by using the 7:2 compressors operation, it produces 16 partial products, in 8th column top most of the 2 bits are performing with half adder operation and 9th column of the top most two bits perform the half adder operation.

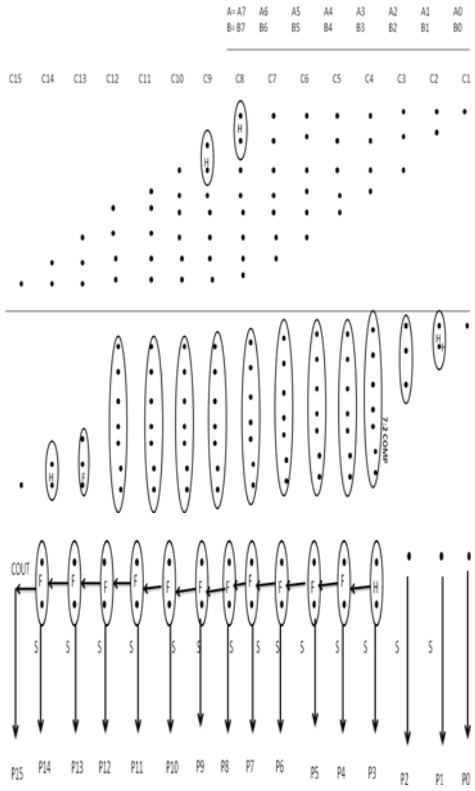

Fig3 : WTM using 7:2 compressor

8th column of the half adder generating two outputs, sum and carry.sum is placed in same column, and carry is propagated to 9th column of the top most bit. In the same way 9th column, sum is placed here and carry is propagated to the next stage. 2nd column of the 2 bits can be performed half adder and its sum is the partial product, 3rd column has 3 bits, it can be performed by full adder and sum is directly partial product. In 4th column adding three zeros for balancing the 7 inputs purpose, and also colomn1,colomn 2 carries are analyze as the initial carries and two extra carry's are applied as '0'.these 4 carry's are applied to the colomn4, this column performs the 7:2 operation. Producing two outputs sum, carry.colomn 4 generating the 4 carry outputs these are applied to the next stage.

In these way of operation is performed up to the 12th column. In 13th column full adder operation is performed and its carry is propagated to the next stage. In 14th column again full adder operation is performed. In the final partial product stage, colomn1 directly getting partial product, in colomn4 the sum and carry are performed half adder operation and its sum is taken as partial product, carry is propagated to the next stage, next sum and carry and pervious carry all are combined to perform full adder. And it continues up to the last column The full adder sum's are the partial product and carry is propagated to next stage

IV. CONCLUSION

In this paper a comparison of WTM a using 3:2 and 7:2 compressors are given and finally concluded that 7:2 WTM design produces less number of PP stages when compared to 3:2 compressor it leads to less carry computational delay and area interms of ha's and fa's. A comparative analysis is done using Xilinx 13.2, and its simulation is observed.

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