# Design of SRAM based BTI Sensor for Improved Cell Stability

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***Abstract***

*The semiconductor industry has reached its focal point with exceptional hike and success in integrated circuit (IC) manufacturing. Due to technology scaling a major reliability issue exists which is time dependent degradation-bias temperature instability (BTI). The parametric variations-PVT (Power, supply Voltage, Temperature) lead to degradation of System-on-chip (SOC's) performance thus increasing the delay over long periods. An aging sensor is thus proposed, for CMOS memories in particular for SRAM cells, to detect the delay faults by active monitoring. The performance of sensor is achieved by tracking the bit line transitions and the output is set high for slow transitions i.e., if transitions didn't occur in expected time frame. The sensors' operation is demonstrated in MENTOR GRAPHICS simulations using 35nm technology.*

**Keywords** — *Aging sensor, CMOS memories, slow transitions.*

## I. INTRODUCTION

We are in an era of mega scale integration and production of System-on-Chip (SOCs) in small overheads to ensure high performance products which are a tremendous driving force in IC industry. As we scale down the CMOS technology, there is a pressure about reliability. The most affecting issue now in semiconductor industry is bias temperature instability (BTI). It is distinguished into two types: Negative Bias Temperature Instability (NBTI) which commonly occurs in p-channel MOSFET and Positive Bias Temperature Instability (PBTI) which is seen in n-channel MOSFET. BTI mainly affects the threshold voltages and this variation depends on the technology used. NBTI is caused due to trap generations at the interface of Si-$SiO_2$ in PMOS transistors [1][2]. These traps induced by NBTI increase with decrease in oxide layer thickness, thus making it sensitive to ultra thin oxides in sub-micron technology.

Most of the System-on-Chip (SOCs) area is occupied by SRAM's which is key factor that decides the robustness of any circuit. Due to BTI effects, the stability of SRAM is degraded; hence accelerating the cell's aging and finally resulting in failure of chips.

The main objective of this paper is to actively monitor the aging sensor for CMOS memory cell. It detects the timing degradation during SRAM access i.e. read/write operations. When a slow transition is detected i.e. if the transitions did not occur in expected time frame output is set high indicating that the cell is aged [3][4]. The sensor is connected to bit line of SRAM cell and thus active monitoring evaluates the transition timing and the sensor analyzes the circuit performance.

## II. LITERATURE REVIEW

Aging is defined as degradation of circuit performance over time. In SRAM cells, the read/write timing diagrams depend on the transistors switching time, temperature, W/L ratio [5]. If any of the above are altered, the output from bit lines during the read/write access gets delayed and over time it leads to damage of device. The previous work about the aging sensor includes many methods of detecting the BTI affects.

According to the concept proposed by Liu and Chan [6], it consists of a group of testing, diagnosis and repair methods for NBTI induced causes. This technology identifies either read or writes' access state of SRAM cell and hence can't access the aging state for both operations.

Another sensor for aging is given by Z. Qi and J. Wang [7]. Here the sensor is built along with SRAM cell in each column and is identical to SRAM cell architecture. Each sensor in the array of SRAM cells is asymmetric and thus the detection of delay faults induced by NBTI/PBTI is not equal and can't guarantee the aging of cells.

In the sensor designed by P. Pouyan, E. Amat and A. Rubio [8], the bit line current is calculated for a specified column of the cell. Here the shift in Vth is very small as the current through access transistors is very small and needs to be amplified. In order to do so, multiple write operations are to be performed which violates the standard SRAM operation that activates only one cell per column at a time.

## III. SRAM (STATICRAM)

### A. The SRAM Cell

The schematic of a 6T SRAM memory cell is shown in figure.1. As its name implies, static, means that as long as power is supplied to the cell, it retains data bits in its memory [9]. It is a type of semiconductor memory that consists of a bistable unit cell storing '1' or '0' as a single bit.

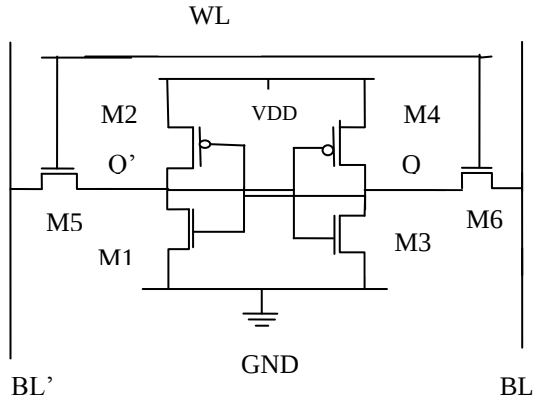


**Fig 1: CMOS 6T SRAM cell**

The SRAM cell consists of 6 transistors. Four transistors form a pair of cross-coupled inverters and other two transistors are the access ones and they are connected when WL=1, which is bidirectional stream of current between the cell and the bit lines.

#### 1) Read Operation

We consider the reading operation with logic value '1' stored, that is, Q=Vdd and Q'=0V.Before the reading operation, the bit lines (BL and BL') are precharged with Vdd. When the word line is high, the access transistors M5 and M6 are connected. The current flows from Vdd through M4 and M6 and charges the BL capacitance CB and even flows into precharged BL' through M5 and M1 transistors, discharging CB'.

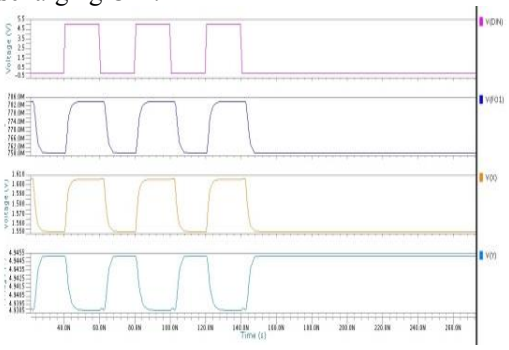

**Fig 2: SRAM read operation**

In this operation CB voltage rises and the voltage in CB lowers. It creates voltage difference between BL and BL' and the sense amplifier will sense the presence of logic '1' stored into the cell. 0.2V of differential voltage is enough to detect this logic level according with [4].

#### 2) Write Operation

In SRAM write operation, we should select the bit line as input and injects the data value '0' or '1' which is to be stored on the memory cell. Before write operation, both the bit lines are precharged with Vdd and the cell supposing to store the logic value '1' and it writes the logic '0', the bit line is set to 0V and bit bar is set to Vdd. When the word line is high, the access transistors are connected selecting the cell [10].

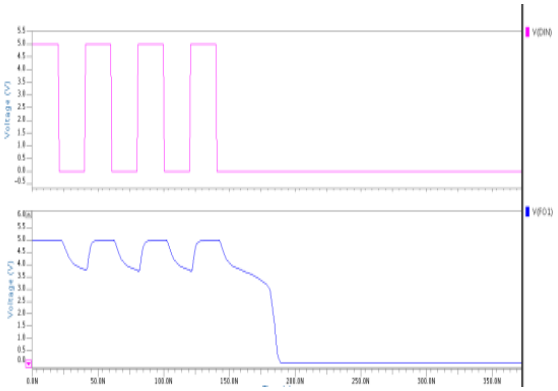

**Fig 3: SRAM write operation**

When M5 and M6 transistors are connected selecting the cell, then the current flows through Q node to BL, discharging the capacitor CQ by decreasing the voltage on Q from high to low. Later the current flows into BL and the node Q charges CQ' capacitor. Then, the positive feedback starts and the new logic value is stored without applying to the previous circuit.

### B. Pre-Charge Circuit

The pre-charge circuit is a part used in SRAM. SRAM charges the bit and bit bar lines to low voltages. Except during the read and write operation, the pre-charge circuit enables the bit line to be charged high. Pre-charge circuit consists of three PMOS transistors, two are used for pre-charging the bit lines and the other one is used to avoid capacitive coupling between two bit lines.

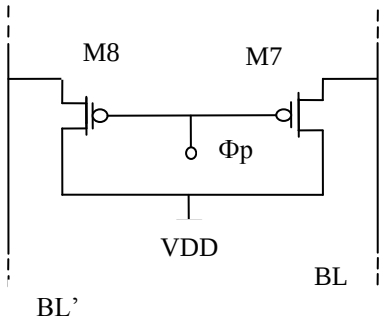


**Fig 4: Pre-charge Schematic**

In the figure, the drains of the below transistors are connected and sources are connected to bit lines. Due to this, the bit lines are pre-charged to Vdd. During pre-charge both bit lines are shorted so the voltage difference across them is zero.

### *C. Sense Amplifier*

Sense amplifier is one of the essential components used in read circuitry. It is used to read the data from the memory sensing the low power from a bit line which represents a data value '1' or '0' stored in a memory cell. Sense amplifier is mainly used to amplify the small voltages to recognizable logic levels. The M5 and M6 transistors act as switches which reduces power consumption.

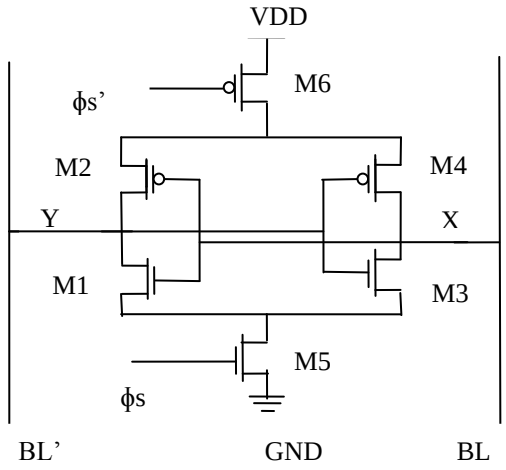


**Fig 5: Sense Amplifier Schematic.**

### *D. Complete SRAM Cell:*

The complete SRAM cell is shown in figure 6. It consists of sense amplifier, pre-charge circuit, and the SRAM cell.

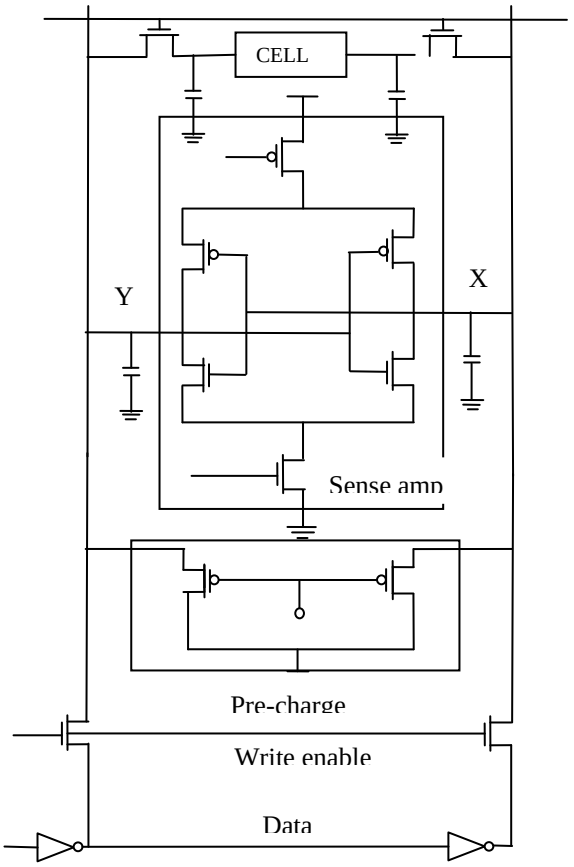


**Fig 6: Complete SRAM Schematic**

The I/O terminals are connected to bit lines and two NMOS MOSFETS along with two inverters are used in order to connect with the column decoder.

## IV. TRANSITION DETECTOR

Transition detector is used to detect the transitions on the memory cell bit lines and generate pulses in the presence of a signal transitions. The generated pulse will have a time duration ($t$) proportional to the transition time of input signals, connected to a bit line (when used for memory aging monitoring).

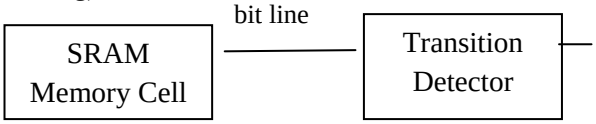


**Fig 7: Transition Detector block diagram**

This way, the switching time of the bit line is measured in a pulse. There are different implementations of the transition detector which have been designed and simulated, to understand which fits better with the aging and performance sensor. A simple way to detect transitions, to measure its switching time is to use inverters with different P/N ratios, to ensure a switch at different voltage levels.

### *A. Transition Detector Implementation-1*

This implementation consists of two paths; one of the paths has the more conductive NMOS transistor and an additional normal inverter which creates a longer path, when compared to the second path which consists of only one inverter with more conductive PMOS transistor. In this way, it will generate an output pulse whenever it detects transition nes.

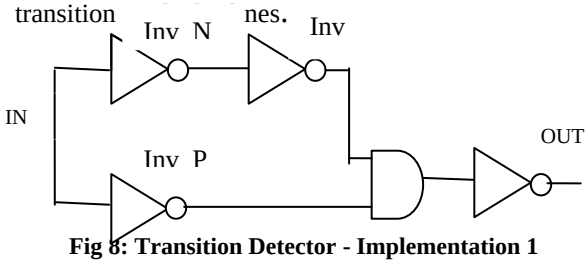


**Fig 8: Transition Detector - Implementation 1 schematic.**

The simulation was performed at 3.5V, 25°C, using 35nm BPTM transistor models and the transistor sizes are described in Table 1.

| Path | Inverter | NMOS | PMOS | L | Vth_n | Vth_p |
|---|---|---|---|---|---|---|
| 1 | Xinv1 | 4*WNmin | WPmin | 35nm | 0.7490 | -0.680 |
| | Xinv2 | WNmin | WPmin | | | |
| 2 | Xinv3 | WNmin | 3*WPmin | | | |

**Table 1: Transition Detector Implementation-1, transistor sizes.**

Under the test environment, the following results were observed in which the peak to peak voltages at rising and falling edges are different and also small duration pulses, are generated.

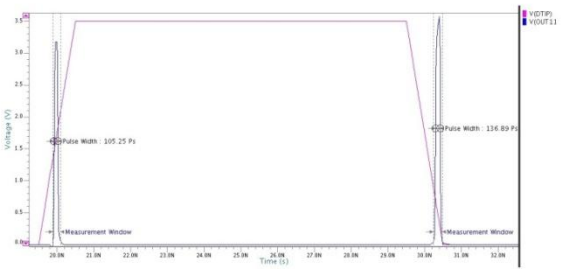

**Fig 9: Transition Detector - Implementation 1, output response**

To find the robustness of the transition detector to PVTA variations the temperature was raised to 110°C, operating voltage was set to 1.1V. It is expected that the transition detector generates high duration pulses, in the presence of higher PVTA variations, but from the output, it was observed that

there is no much increase in the pulse widths hence this implementation is not robust, as it is less sensitive to higher power-supply voltage and temperature degradations.

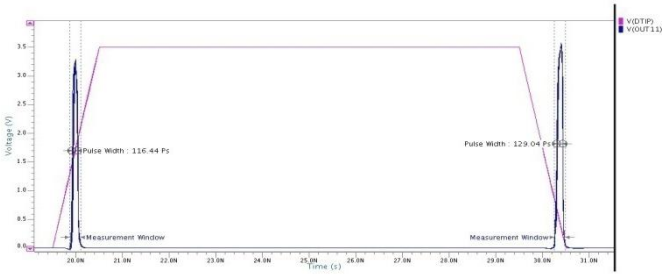

**Fig 10: Transition Detector - Implementation 1, output response for PVTA variations**

### *B. Transition Detector Implementation-2*

This was an attempt to improve from previous implementation-1, by creating two similar paths, having the same number of gates(two inverters each), connected to a CMOS XOR gate to detect the difference in those paths.

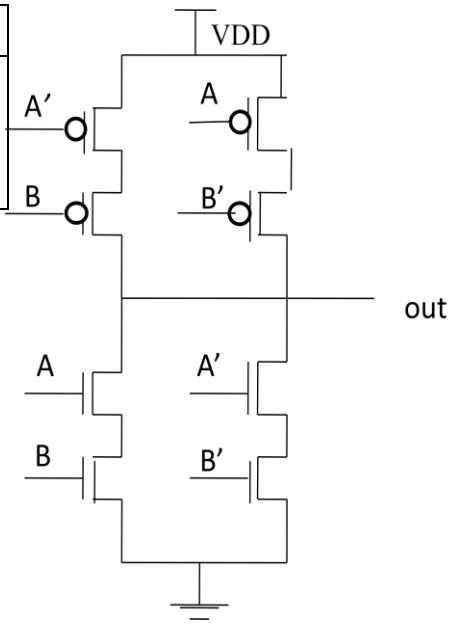


**Fig 11: CMOS XOR gate schematic**

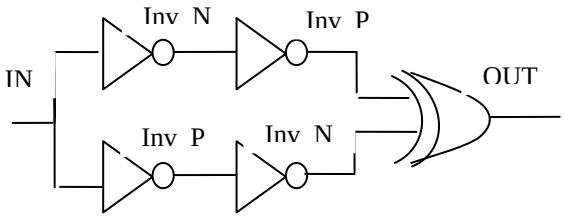


**Fig 12: Transition Detector Implementation-2 schematic**

**Table2: Comparison of rise and fall times of transition detectors at different conditions.**

| Implementation | At normal conditions | | At PVTA variations | |
|---|---|---|---|---|
| | Rise time(ns) | Fall time(ns) | Rise time(ns) | Fall time(ns) |
| 1 | 105.25 | 136.89 | 116.44 | 129.04 |
| 2 | 513.60 | 548.72 | 521.06 | 543.69 |

The simulation was performed at 5V, 25°C and using 35nm BPTM transistor models and the transistor sizes are described in table 2.

| Path | Inverter | NMOS | PMOS | L | Vth_n | Vth_p |
|---|---|---|---|---|---|---|
| 1 | Xinv1 | 5*WNmin | WPmin | 35nm | 0.7490 | -0.680 |
| | Xinv2 | WNmin | 4*WPmin | | | |
| 2 | Xinv3 | WNmin | 4*WPmin | | | |
| | Xinv4 | 5*WNmin | WPmin | | | |

**Table 3: Transition Detector Implementation-2, transistor sizes.**

| Path | Inverter | NMOS | PMOS | L | Vth_n | Vth_p |
|---|---|---|---|---|---|---|
| 1 | Xinv1 | 10*WNmin | WPmin | 35nm | 0.7490 | -0.680 |
| | Xinv2 | WNmin | 10*WPmin | | | |
| | Xinv3 | 10*WNmin | WPmin | | | |
| | Xinv4 | WNmin | 10*WPmin | | | |
| 2 | Xinv1 | WNmin | 10*WPmin | | | |
| | Xinv2 | 10*WNmin | WPmin | | | |
| | Xinv3 | 10*WNmin | 10*WPmin | | | |
| | Xinv4 | 10*WNmin | WPmin | | | |

From the output waveform, it was observed that the pulse widths have been increased compared to the previous implementation.

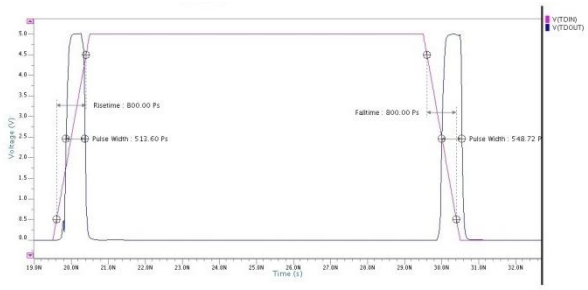

**Fig 13: Transition Detector Implementation-2, output response**

The behavior of the transition detector implementation-2 is observed under PVTA variations, a simulation is performed by increasing the temperature to 110°C and decreasing the operating voltage. But we can observe that there is a small increase in the pulse widths and also due to the usage of CMOS XOR the power dissipation is more so this is not considered as robust.

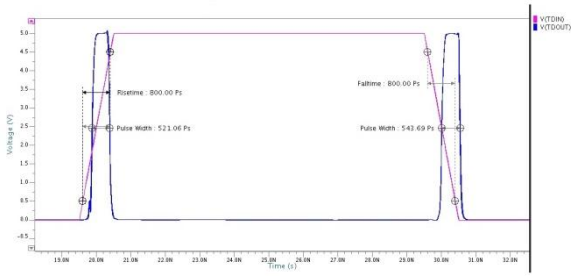

**Fig14: Transition Detector Implementation-2, output response for PVTA variations.**

### *C. Transition Detector Implementation-3:*

This implementation contains two path with 4inverters each, 2 inverters with more conductive NMOS and 2 with more conductive PMOS converging to a pass- transistor logic XOR gate includes an inverter at its output, ensures good performance and less power dissipation when compared to the previous implementation.

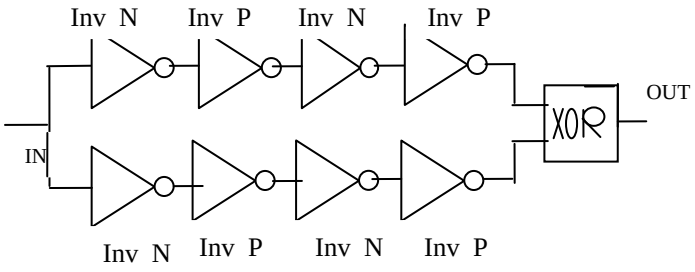


**Fig 15: Transition Detector – Implementation-3, schematic**

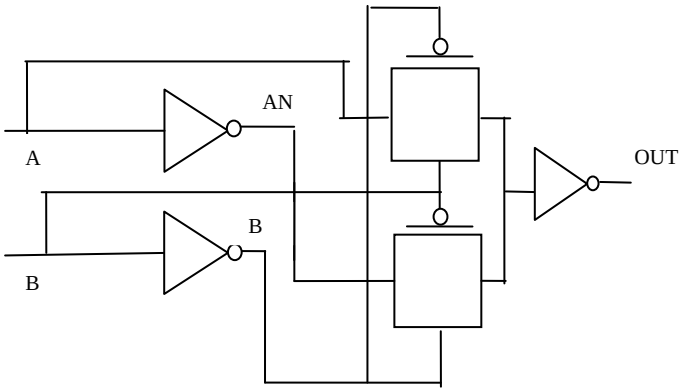


**Fig 16: Pass-Transistor XOR gate Schematic**

**Table 4: Transition Detector Implementation-3, transistor sizes**

The simulation is performed at 3.5V using 35nm BPTM transistor models and the results are presented in the figure. As it can be seen, the generated pulses are having the high duration pulse widths.

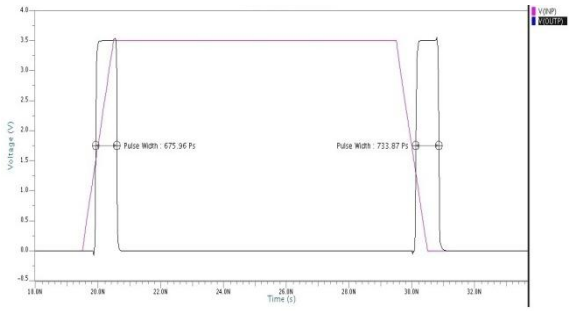

**Fig17: Transition Detector – Implementation-3, output response**

Transition detector implementation-3 robustness is observed under PVTA variations and from the results it was demonstrated that when transistors suffer a performance degradation then transition detector generates larger pulses, and this result can be used to consider this implementation as robust. This implementation is tested under various technology scaling [11], different voltages and the test results are tabulated below.

| Technology scaling | Under normal conditions | | At PVTA variations | |
|---|---|---|---|---|
| | Rise time(ns) | Fall time(ns) | Rise time(ns) | Fall time(ns) |
| 130nm | 359.87 | 408.97 | 370.99 | 420.59 |
| 180nm | 451.37 | 488.99 | 464.88 | 495.08 |
| 250nm | 522.85 | 563.50 | 529.96 | 570.69 |
| 350nm | 675.96 | 733.87 | 677.88 | 736.10 |

**Table 5: Technology scaling for transition Detector Implementation-3, comparison of rise and fall time**

## V. PULSE DETECTOR

The output pulses of transition detector is transferred to pulse detector block, which are indicated by pulse width (The time duration of a transitions as the input signal).When SRAM circuits aging occurs and the transitions slow down, the pulse width increases. When the pulse width of transition detector output pulses exceed a specific amount, it signalizes as an error to the pulse detector output. There are two implementations in pulse detector – Stability Checker implementation, NOR based implementation.

### *A. Stability Checker*

In this the pulse detector is to use a stability checker to detect transitions in the pulses created by the transition detector, after a specific time defined by the clock.

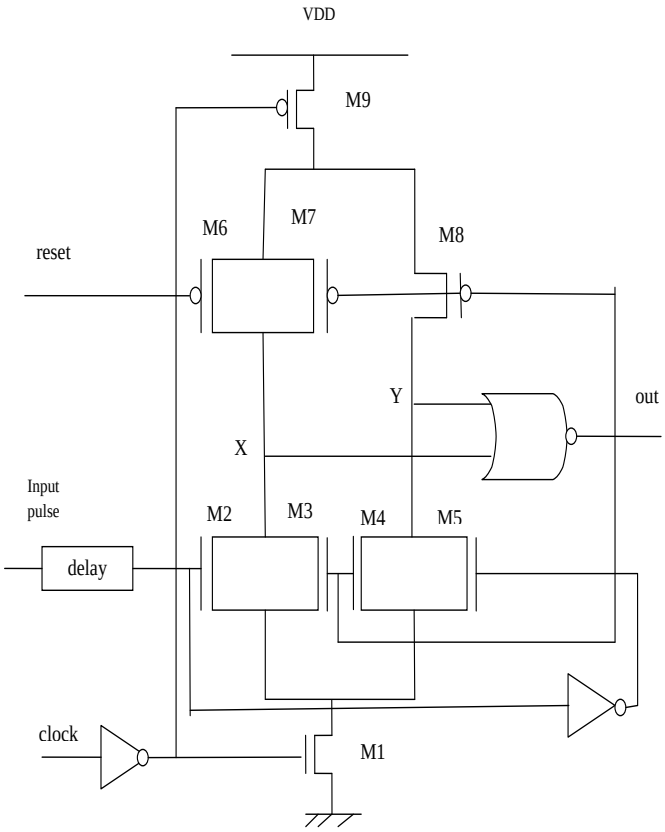


**Fig 18: Stability Checker Implementation Schematic**

It detects all transitions in the data input signal that reaches the stability checker during the active pulse of the clock.

Consider, the complete outputs of the aging sensor using transition detector implementation 3 and stability checker. This simulation is performed to validate the complete aging sensor.

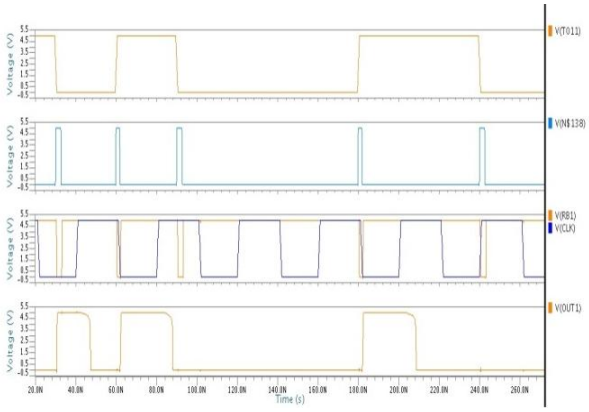

**Fig 19: Stability Checker Implementation, output response**

Considering, PVTA parameters for stability checker, the voltages are considered as per the

technologies. The temperature variations are 25-80 degree Celsius with step 10

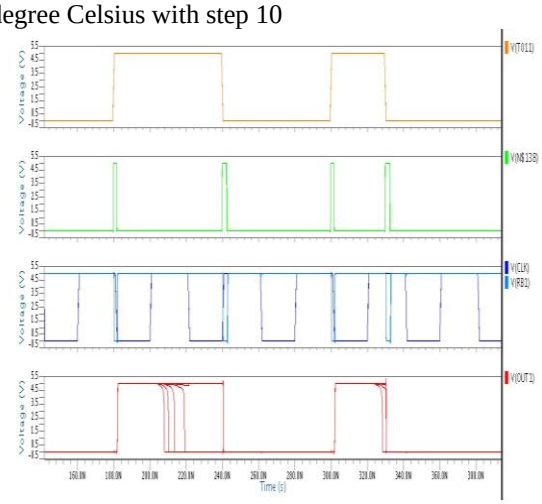

**Fig 20: Stability Checker Implementation, output response with PVTA variations**

The previous section represents a robust pulse detector implementation. However, the obtained circuit can be improved, this implementation by improved version of pulse detector, reducing the number of transistors and space. The following is he improved pulse detector implementation.

### *B. NOR based implementation*

In order to simplify the stability-checker functionality when applied to a pulse detector, a new pulse detector implementation was tried, the NOR-based pulse detector presented in this section.

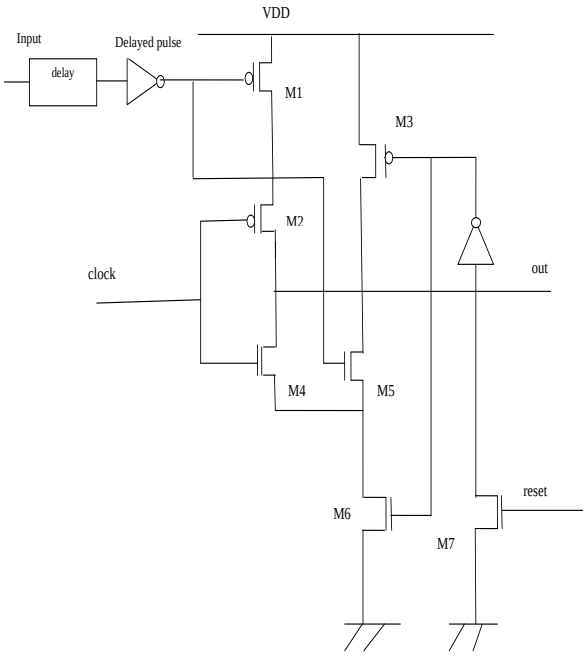


**Fig 21: NOR Based Implementation schematic**

In the SRAM memory, all the control signals and all the instructions are generated synchronously with the main clock. Therefore, considering that output pulses of the transition detector are generated, the pulse width of transition detector output are exceeding a specific amount, signalizing an error in the pulse detector output, an error signal will be obtained.

Consider, the complete outputs of the aging sensor using transition detector implementation 3 and NOR based implementation. This simulation is performed to validate the complete aging sensor.

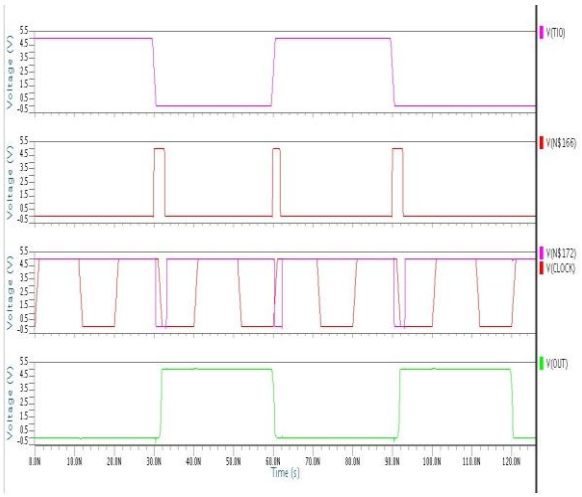

**Fig 22: NOR Based Implementation output response**

Considering, PVTA parameters for NOR based pulse detector, the voltages are considered as per the technologies. The temperature variations are 25-80 degree Celsius with step 10.

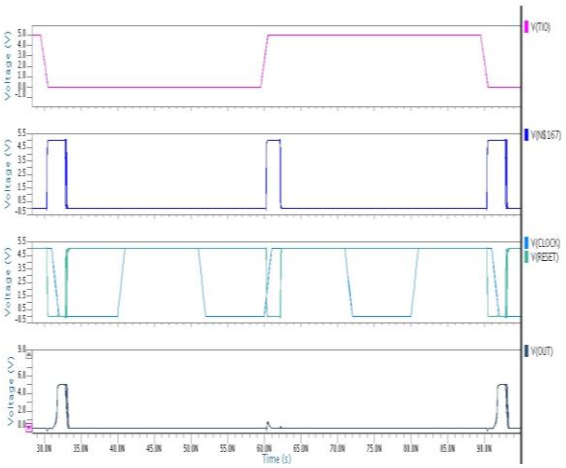

**Fig 23: NOR Based Implementation output response with PVTA variations**

Hence, by design we have two parameters to control the delays in the sensor and the error/non-error decision. (1) To increase the width of the pulses generated in the transition detector; and (2) the time delay in the signal in the pulse detector's delay element.

## VI. COMPLETE SENSOR

Therefore, considering that output pulses of the transition detector are generated, the pulse width of transition detector output are exceeding a specific amount, signalizing an error in the aging sensor output. An error signal will be obtained.

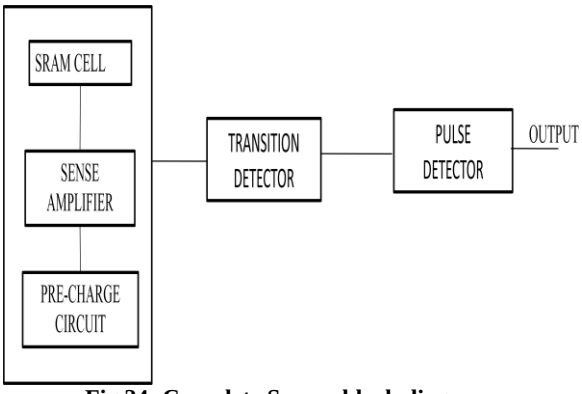


**Fig 24: Complete Sensor block diagram**

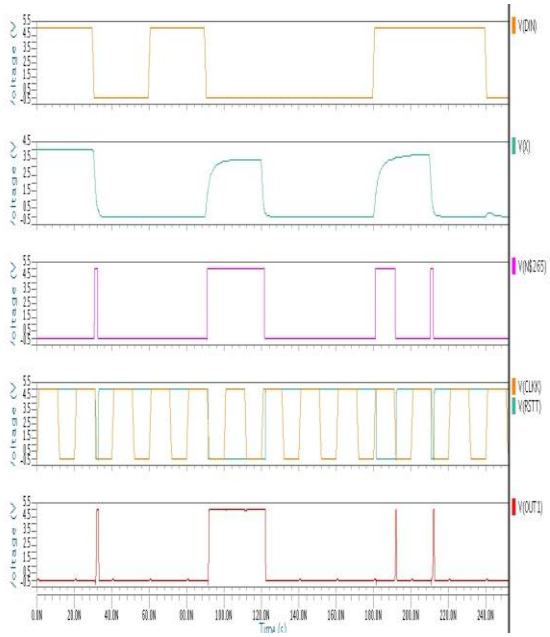

**Fig 25: Complete Sensor Result**

Considering the complete solution for the sensor, using for the SRAM the transition detector and the pulse detector, simulations were performed to validate the entire sensor solution.

### *A. Layouts*

The layouts are designed using CMOS 35nm foundry available. First we have designed a 1 bit SRAM cell and then the remaining memory circuitry (sense amplifier, pre-charge).

### *B. SRAM cell*

The layout of the SRAM cell is shown in the figure 26. The two inverters are driven by the two NMOS access transistors, which are activated by the word line (WL) to provide an extra drive capability and allow cell's writing.

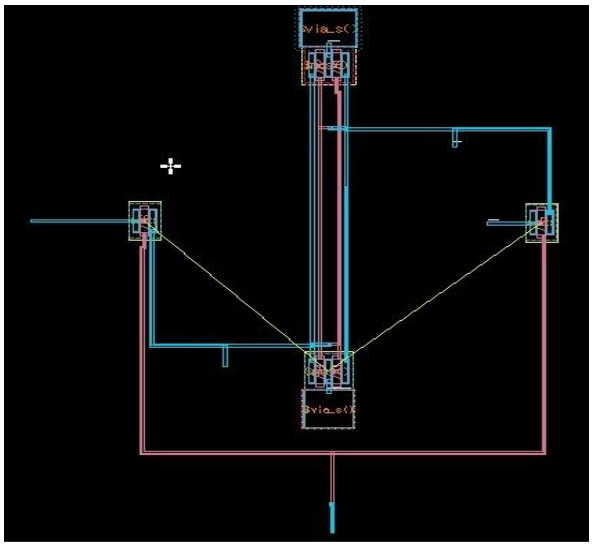

**Fig 26: SRAM cell layout**

The above layout consists of two cross-coupled inverters along with access transistors.

### *C. Sense Amplifier:*

The sense amplifier is used to amplify the small signal differences between the bit lines.

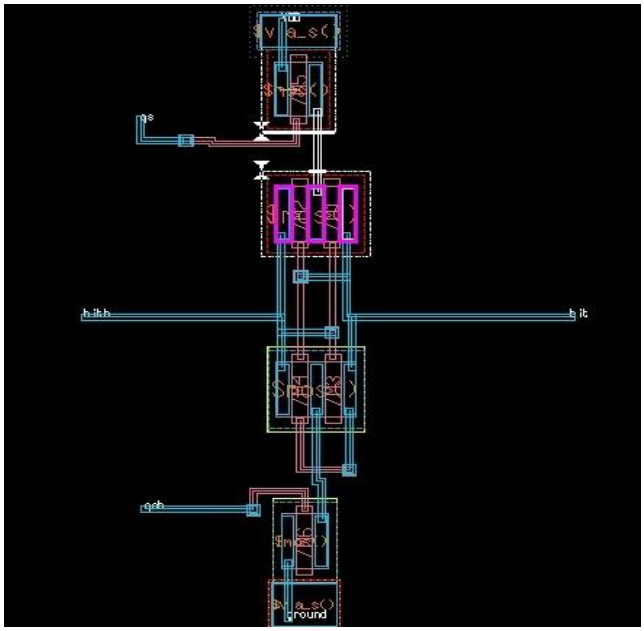

**Fig 27: Sense Amplifier layout**

The sense amplifier is controlled by the sense signal ($\phi_{s}$).

### *D. Pre-charge*

The pre-charge circuit layout is shown in the figure 28. The pre-charge circuit is controlled by the signal ($\phi_{n}$).

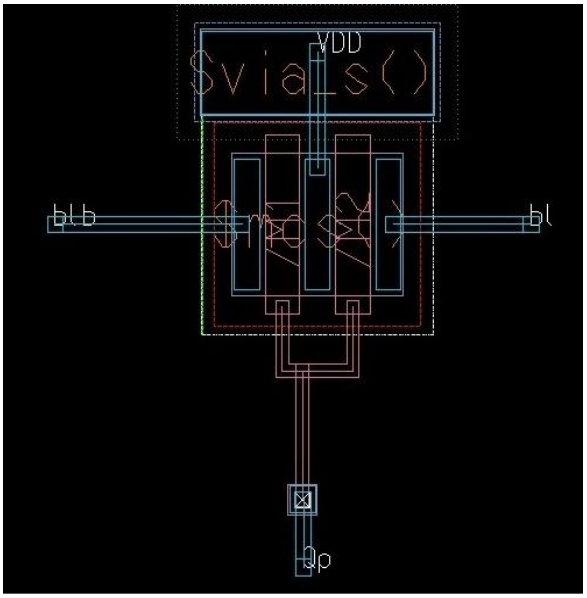


**Fig 28: Pre-charge circuit layout**

This circuit pre-charge bit lines to VDD, before a cell read/write.

## VII. CONCLUSION

This paper focused on the development of an aging sensor for CMOS memories, detecting the aging on SRAM memory cell. The circuit's aging over the time, reflects longer propagation times and degrades the circuit's performance. BTI is pointed as the most relevant effect for the performance loss. The four parameters that can influence enormously the performance of nanometer technologies are Process, power supply Voltage, Temperature and Aging (PVTA). Circuit's aging is due to high operation temperatures, and lower power-supply voltages slow down the circuit's performance, due to switching activity. In this work, the main objective is to detect aging, in particular the CMOS memory cells aging, and how its performance degradation, affects the basic memory cell operations, the read and also the write. The main goal was to develop an aging sensor, aiming the identification of slow transitions occurrences on memory cells caused by the aging, in specific SRAM cell.

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