6T FA Using 2T EX-OR Gate

M.Sai Lakshmi[1], K.Mahammad Haneef[2], T.V.Nirmala[3], Dr.T.Lalith Kumar[4], S.Saleem[5]
P.G. Student, Dept. of ECE
AITS, Kadapa, India

Abstract

EX-OR gate plays a major role in digital circuits. This paper presents the 6-transistors FA with a 2-T EXOR gate. In these design we using few transistor and it does not uses the additional complementary input signal. By decreasing the transistor count in a FA circuit, we can able to decrease the area, expenditure of the power and delay. The proposed 6 Transistor FA has been contrast with the earlier 38T,28T,14T,10TFAs.

Key words: ***6-T FA, area, delay, 2-T EX-OR gate.***

I. INTRODUCTION

Addition is the one of the fundamental operation performed in various process like multiplications, filtering ,etc., A FA is used to perform the addition operation , it operates with three 1-bit binary numbers of inputs A,B,C and two 1-bit binary numbers of output sum(S),and carry(Cout).

SUM=X (xor) Y (xor) Z - (1)

COUT=(X and Y) or (Y and Z) or (Z and X)– (2)

There are some different ways to represent theseFAcircuit in terms of the CMOS logic by enlarging the speed and reducing the power consumption . one of the approach to decrease the transistor count so that delay and power consumption is reduced. The output will be understood by examination of the FA truth table. For example when the three input bit is '0' i.e., A=0,B=0,C=0 then the sum for the given inputs is '0 'and carry also '0' that are combined with an OR gate.

SUM=X (xor) Y (xor) Z - (1)

COUT=(X and Y) or (Y and Z) or (Z and X)– (2)

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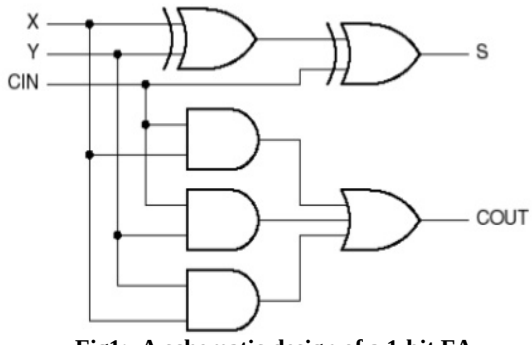


Fig1: A schematic design of a 1-bit FA.

The basic 1-bit FA is realized from the truth table which is shown in below figure. A FA output equation can be given as equation (1) and (2).

Here, our task is to implement a FA circuit which consumes the less power and performs at high speed. Most of the power in digital circuit is consumed by power utilization of data path of the circuit which contains the large no. of transistors. So, that we can able to degrade the power consumption, and also increases the speed of the operation.

II.EXISTING SYSTEM

A. 38-Transistor Fa

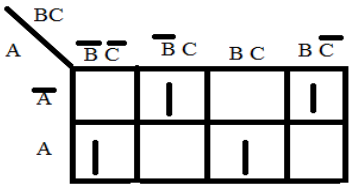
38 transistor FA is implemented with the 38 transistors, it contains three number of inputs A,B, C and two outputs SUM and CARRY. These 38 transistors are arranged based on the SUM and CARRY Boolean expression . The functioning of these 38 transistors FA is verified by the FA truth table which is shown in below .where ten transistors are utilized for five inverters remaining 28 transistors are utilized for the FAcircuit arrangement , in other words 24 transistors are used for defining the SUM and 14 transistors are used for defining the CARRY.

TABLE1: FA Truth Table

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In the above truth table the two outputs SUM and CARRY are generated based on the karnaugh-map shown below.

k-map for SUM



$S=\overline{A}\,\overline{B}\,C+\overline{A}\,B\,\overline{C}+A\,\overline{B}\,\overline{C}+A\,B\,C$

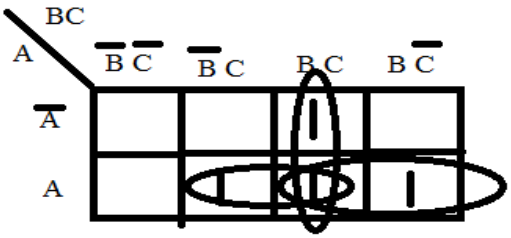
$S=C[\overline{A}\,\overline{B}+A\,B]+\overline{C}[\overline{A}\,B+A\,\overline{B}]$

$S=[C\,\overline{X}+\overline{C}\,X]$ (A XOR B)

S=[C XOR X]

S= (A XOR B XOR C)

k-map for CARRY



C=AB+BC+CA

Fig2: k-map for generating sum and carry

A karnaugh map is an efficient method for reduction of the Boolean expressions, it has some Boolean algebra theorems and also it is used for equation manipulations. Hence, By the k-map method we can able to minimize the Boolean expressions easily.

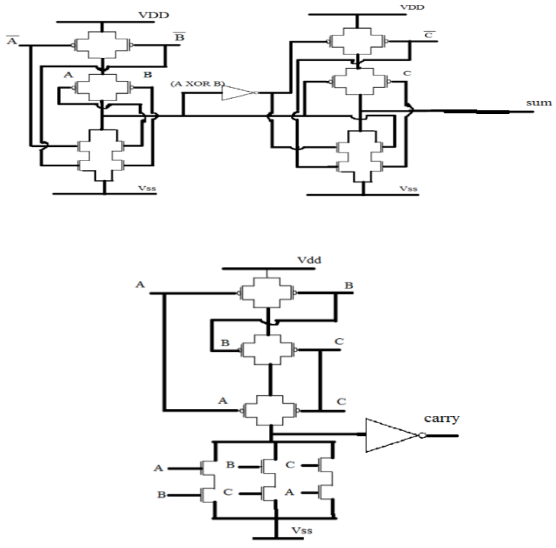


Fig3:Transistor level schematic for Generating of sum and carry.

B. 28 Transistor FA

28-transistor FA circuit contains the 28 transistor count, in that 14 transistors are n-mos transistors and 14-transistors are p-mos transistors. These 28 transistor FA is implemented with the help of output Coutbar .where theseCout bar is generated as the inversion of carry output by using demargons law ,then we can simplify this expression as shown in below equations. Here 10 transistors are used for this carry output bar.

Cout = [(AB)+(BC)+(CA)]'

= (AB)'. (BC)'.(CA)'

Cout = (A'+B'). (B'+C').(C'+A')

SUM=A (xor) B (xor) C

The below figure shows the gate level schematic of a 28- transistor one bit FA circuit.

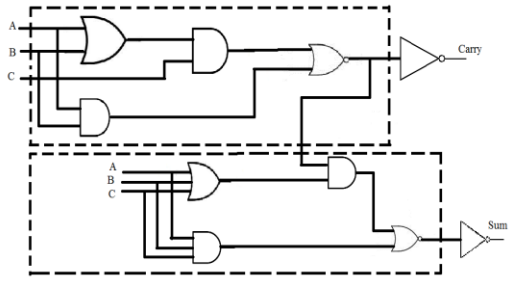


Fig4: gate level schematic of 28-transistor FA circuit.

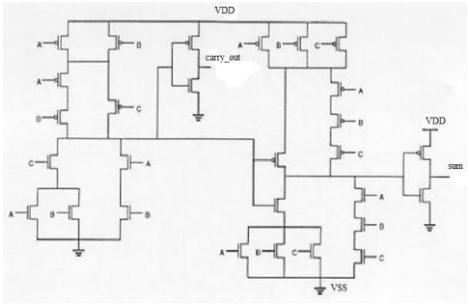


Fig5 : 28-transistors transistor- level schematic of one bit FA circuit.

By using these 28 transistor implementation we can decrease the circuit density ,transistor count and complexity. So, that we can customize the reduction of the chip area.

C. 14 Transistor FA

A traditional 14 transistor one bit FA consists of 14 number of transistor count . It is implemented by the two - 4transistor xor gate and two - 2 transistor transmission gate logic as shown in the transistor-level 14 transistor FA circuit .

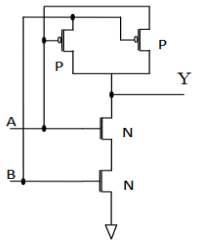


Fig6: 4-Transistor ex-or gate

TABLE2: 4T Ex-OR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

The above figure and truth table shows the implementation of xor gate with the four in that two are P-MOS transistor and another two are N-MOS transistor . Here, input A passes as control signals to P2 and N1 transistors ,likewise another input B passes to P1 and N2 transistors as control signals. In other words it gives the exor gate output as '1' when both A and B inputs are in alternate to each other as shown in the above table.

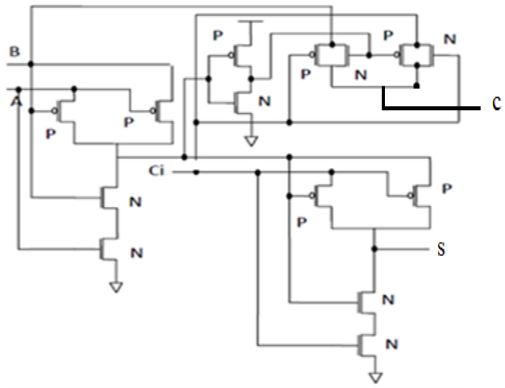


Fig7: 14 –Transistor schematic FA circuit

By observing the schematic of a 14 transistor FA , we can ensure that two xor gates are used for the generation of SUM ,and CARRY is generated by using the two transmission gates.

SUM = A (xor) B(xor)C

CARRY = A(and)B+B(and)C+C(and)A

The first XOR gate 1 contains two inputs A and B gives the output as A(xor)B ,the output of xor gate 1 is given as an input to the xor gate2. The xor gate 2 output gives the SUM , in other words it gives the output as A(xor)B(xor)C. Another output of FAi.e; a CARRY is generated by using two transmission gates, the output of xor gate 1 is given as input to the inverter such that it produces the output of xnor gate and these act as a control inputs to the first transmission nmos transistor and the second transmission pmos transistor.

D. 10-Transistor FA

As the trends of digital electronics in VLSI design increases day by day one must concentrate on specifications such as effective speed, area, power. Because of the demerits present in 38T,28T,14T we are choosing here 10 Transistor for implementing the FA there by reducing the transistor count so as area also reduced ,with increase in the speed, then it leads to decrease of the power consumption. A 10 transistor FA circuit that contains 10 number of transistors, is implemented by using the one 4T xor gate logic and three 2T xor gate logic. Here two 2Txor gates are used for the generation of the SUM and another xor gate is used for generating CARRY expression.

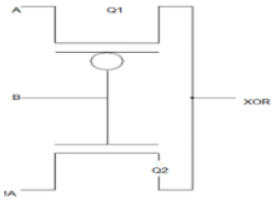


Fig8 : 2T xor gate

A 2T xor gate contains one nmos transistor and one pmos transistor. The source terminal of pmos and nmos transistor are complementary with each other. The output 2T xor gate depends on the control input.

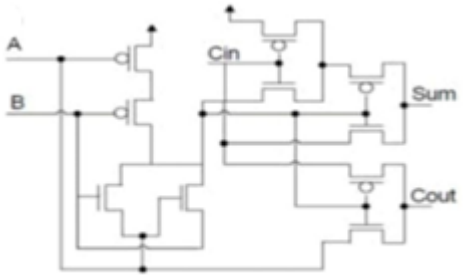


Fig9:10-Transistor FA circuit

III. PROPOSED SYSTEM

A. 6-Transistor FA

A 6T-FA using two transistor EXOR gate is our proposed system. Here, we are using 2T-EXOR gate so, that we provide decrease transistor count .therefore, the circuit operates at high speed by reducing the transistor count. By using six transistor not only speed is incremented , we are going to decrease the area

but also power consumption is decreased using the less transistor so, that it decreases the expenditure of power.

.A 6-T FA contains three blocks in that two blocks are 2-Transistor EX-OR gate and another one is a two transistor multiplers as shown below. The sum and Cout can be obtained by using the eq(1) and eq(2).

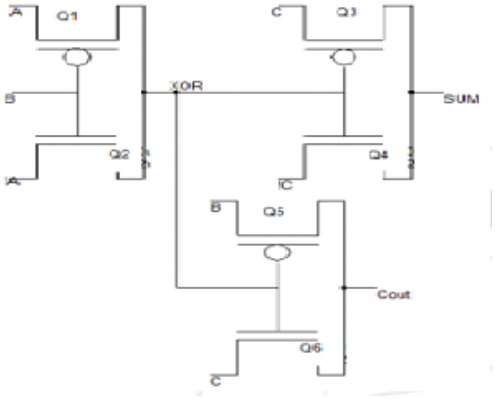


Fig10: 6-T FA circuit using EXOR gate

However, it performs the operation with the high speed when compared with the existing 14-T FA and allow the expenditure of the less power than the 14-T FA.

Fig11: 2 input ex-or gate

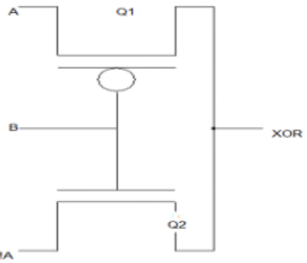


Fig12: 2-T EXOR gate

The above shows 2-T EX-OR gate that contains the NMOS transistor and a PMOS transistor Q1 and Q2 respectively A and B are inputs. When the two inputs are in logic low then PMOS transistor Q1 turns to ON state and the NMOS transistor Q2 turns to OFF state. The output equation of an 2T exor gate is given as

Y=A(xor)B=AB+BA.

IV. RESULTS AND ANALYSIS

The below tabular column shows the transistor count, expenditure of power for the existing and the proposed system. The simulation is performed with the different supply voltage which is suitable to compare transistor, and power consumption.

TABLE3: 14T vs 6T FA

PARAMETERS	14-T FA	6-T FA
TRANSISTOR COUNT	14	6
POWER	7.185µW	4.45µW

V.CONCLUSION

After examine all the possibilities in the design of the FA , it came into conclusion that 6T FA has less area in terms of transistor count and also it provides better results in terms of power.

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