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Different parameter analysis for SRAM

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Abstract: *In today's VLSI design circumstances, upscaling of technology and downscaling of transistors are inversely proportional. Power dissipation impactsSRAM cells widely as the technology shrinks down. Static Random Access Memory (SRAM) is designed to interface with CPU directly, DSP processors, µprocessors, and low-power applications such as handheld devices with long battery life. In the total power consumption, leakage and other parameters also play an important role in the circuit's performance. In this paper, we have applied two diverse technologies on 6 T SRAM, and the result has been comparedwith6T SRAM formed with memristor.*

Keywords: *SRAM, DTMOS, Memristor, Sleep transistor*

INTRODUCTION

Due to the endless escalation of MOSFET technology, the component diameter of integrated circuits faces many physical constraints. In integrated circuits, excessive leakage current and device/circuit reliability are the two major factors in the scaled devices. Power efficiency and reliability are conflicting issues that have been considered, especially for reliable circuit designs [1].

In the integrated circuits, the transistors suffer multiple temporal degenerations such as Hot Carrier Injection (HCI), Time-Dependent Dielectric Breakdown (TDDB), Bias Temperature Instability (BTI). This may cause significant discrepancies in the devices because of:-

(i) the improper manufacturing process, (ii) improper biasing, and (iii) improper working environmental conditions during their operation, resulting in degradation of device performance with time.[2]-[3].

Transistors also suffer from Process, Voltage, and Temperature (PVT) variations, which cause suspicion in VLSI integrated circuits. The reliability of the circuit degrades due to processing variation, such as variation in channel length, oxide thickness. [4]

With the progression of technology, SRAM has become an important component of technology scaling since chip area can be shrunk to a large extent in the memory for high-performance applications [5-6]. In modern technology, due to the continuous enlargement of nanoscale range devices, power consumption and packaging density have become the main restrictions in many designs. More than 40% of total active mode power is due to leakage current in high-performance I.C.s, though it is the only source of power consumption in idle circuits. Shortly, SRAM will likely be the preferred memory in embedded technology for various microprocessors and Systems on Chips(SoC) because of its speed and compatibility with typical logic processes. Variations in device geometry are based on threshold voltage due to dopant fluctuations and also on various fabrication processes and variations in it. These are most prominent in SRAM as the cell size is minimized using a width of devices and minimized gate length. The cell stability, which furnishes minimum array operation voltage and yield, is of primary concern and has become more difficult to focus on [7-8]. The design of power-efficient SRAM has become the principal factor in scaled technology of the modern era.

A. 6T-SRAM

Fig. 1 shows the conventional 6T-SRAM cell. It consists of two CMOS inverters, which are cross-coupled with each other. During read and write operations, transistors are connected to the word line to activate read and write operations. In the active mode, the first-word line gets activated and is turned ON for access transistors to read data from the memory cell to write data on the memory cell through the bit line. During all read/write processes, power dissipation takes place. There are three types of operation taking place in SRAM

1) Stand by operation
2) Read operation
3) Write operation

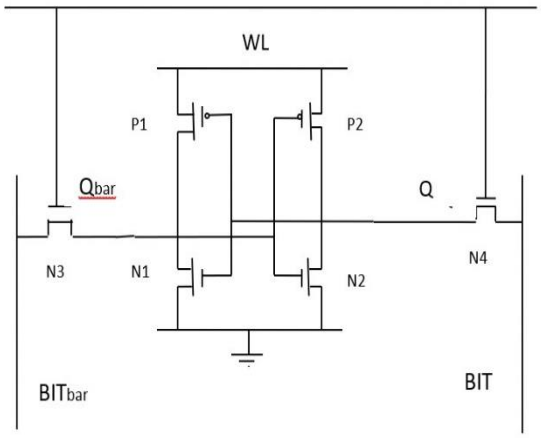


Fig. 1 Standard 6T SRAM

B: STAND BY OPERATION

A standard one bit 6T SRAM structure is presented in Fig. 1. A one-bit SRAM cell operates in Standby, Read and Write modes. In each mode of operation, the SRAM cell suffers from strong power dissipation. A standard 6T-SRAM cell consists of two cross-coupled inverters- P1, N1, P3, N3, and two pass transistors-N2, N4 to access the data in both the operations. The Write data-enabled line W.L. is pulled to HIGH to turn ON pass transistors N2 and N4 so that it can access the values from the Read access line B.L. and B.L.'.Q and Q' are the stored nodes in Write/Read operation.

Standby Mode: In this mode, SRAM will store the value '1' and '0' in Q and Qbars, respectively, so that the pre-charge cycle in SRAM circuitry pulls capacitors HIGH for Bit and Bit bar.' When Write line W.L. will be '1', the access pass transistors are turned ON with a Standby of Read '1' mode for SRAM cell.

Read Mode: In this mode, memory should hold some values such that Q=1and Qbar=0 and W.L. should be one, Bit and Bit bar lines should be output lines, the capacitor should be pre-charged, which means voltage should be Vdd near the capacitor point. There is a voltage difference between the $Q_{bar}$and the node pt so that the capacitor near the Qbar discharges. Therefore, bit bar voltage decreases, and the output value is one.

Write Mode: In the write operation, memory block holds Q=0 and Q_{bar}=1, and W.L. should be one, bit and $bit_{bar}$are equal to I/P because we have to write into the memory, so we have to make bit_{bar} grounded.

C: MEMRISTOR

Memristor's (memory-resistor) theory was propounded by Leon Chua in 1971 and formalized by Kang [9,10] as a new fundamental circuit element. Memristor consists of a thin nanolayer (6 nm–8 nm) of insulating TiO_2 and a second Oxygen deficient nanolayer of TiO_{2-x}sandwiched between two Pt nanowires [11,12]. The electrical behavior, as a memory, is determined by the boundary between these two regions. It is based upon the principle where one part of the TiO_2nanolayer receives oxygen ions (O2-) while the other part of TiO_2 nanolayer loses oxygen ions. A change in the distribution of oxygen ions within TiO_2 nanolayer changes the resistance [13]. The voltage/current relationship of the memristor defined as *M(q)*, can be modeled as:

Fig. 2: Memristor

$$v(t) = \left[R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right] i(t) \text{ .....(1)}$$

where D is $Ti_{o2/Ti_{o2-x}}$, film thickness$R_{ON}$is the resistance for completely doped memristor while $R_{0ff}$is the resistance for the undoped region. The width of the doped region w(t) is given as:

$$w(t) = \mu_D \; R_{\frac{ON}{D}} \; q(t) \qquad \text{…….(2)}$$

for R_{ON}<<R_{off} that is the case of the digital circuit; Eq 1 is modified to:

$$M(q) = R_{OFF}\,(1 - \tfrac{\mu_D R_{ON}}{D^2} q(t)) \qquad \text{…..... (3)}$$

where $\mu D$is the average dopant mobility (m2S-1V-1).

Low Power Techniques

For VLSI designers, SRAM plays an important role. There are two main reasons; first, it plays a middleman role between the DRAM and CPU as a cache memory, and second, it replaces the DRAM where low power consumption is required.

Power Dissipation

There are four types of power dissipation

1) Dynamic power dissipation

2) Switching power dissipation

3) Short-circuit power dissipation

4) Glitching power dissipation

Here, we are considering peak power and average power dissipation

Peak Power Dissipation

It occurs due to the turning of the power of a laptop or computer. Peak power affects the ckt, supply, and ground line heavily and also impacts other components of the ckt. Due to this, glitches may occur. When read and write operations are held, we may read or write wrong data due to its transient nature. For reducing the amount of power dissipation, we are using different techniques and comparing them with 6T SRAM formed with memristor as explained below:

1) SRAM with memristor
2) SRAM with sleep transistor technique
3) SRAM using DTMOS technique

D: 6T SRAM WITH MEMRISTOR

Memristors (also known as memristance) are passive elements with varying resistance [14]. These devices are resistors with varying resistance, which depends on the history of the device. Memristors can be used as a memory where the data is stored as a resistance. For memristive devices, memory is a common application, whereas the additional applications of these memristive devices are functional blocks, such as analog circuits, neuromorphic systems, and logic circuits. The definition of Memristive devices is broader than the definition of the memristor. It is common to use the term memristor for all memristive devices [15,16]. Every change in memresistance depends upon its prior history. The total change takes place through it or the total flux through it.

In this figure, memristors are connected with two NMOS. N1 is cross-connected with the M2 memristor, and N2 is connected with the M1 memristor.

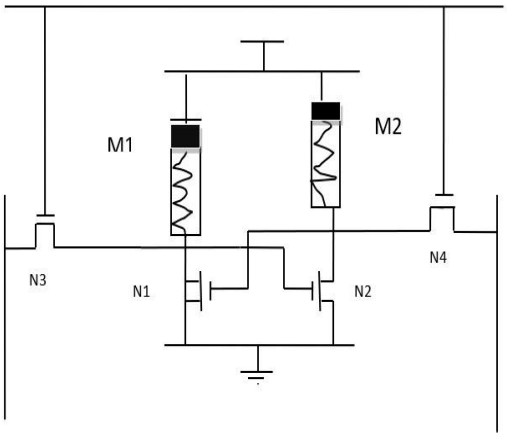


Fig. 3: 6T SRAM with Memristor

E: SRAM WITH SLEEP TRANSISTOR TECHNIQUE

Fig. 3 shows the SRAM circuit with two sleep transistors, applied on the upside and downside of the circuit. One PMOS transistor and one NMOS transistor are connected in series with the transistors of the cell in such a way so that virtual ground NMOS side and virtual power supply towards PMOS side is formed [17]. The working of the circuit is such that when the circuit is on, the sleep transistor gets activated so that the working of the circuit remains retained, whereas, in OFFstate, the sleep transistor gets OFF so that the source node of the gate floats. Because of this leakage, the path gets cut off. There are two main reasons for power reduction: the low sub-threshold leakage current of high Vthand the other is the stacking of transistors.

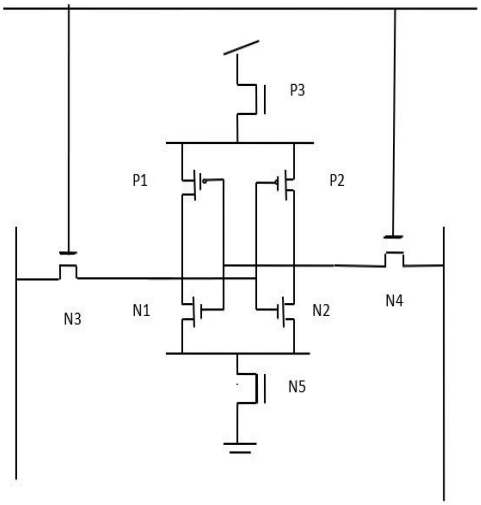


Fig. 4: SRAM with Sleep Transistor Technique

E: 6T SRAM WITH DTMOS TECHNIQUE

Fig. 5 shows the implementation of the SRAM circuit using the DTMOS technique. In DTMOS, dynamic body biasing is used as a substrate, and the gate terminals are connected. Due to this, there is a body effect that changes the threshold voltages of PMOS and NMOS dynamically. If we consider one part of the SRAM using the DTMOS technique, i.e., an inverter, we can see that in the active mode, the logic changes from low to high with a higher speed as the threshold voltage is low for PMOS. In the standby mode, the static leakage current is determined by the sub-threshold current of the NMOS, which has a high threshold voltage. Because of this, the static leakage current decreases considerably [18]. The main advantage of using DTMOS is that it increases cell stability while body biasing improves the tolerance variation in logic.

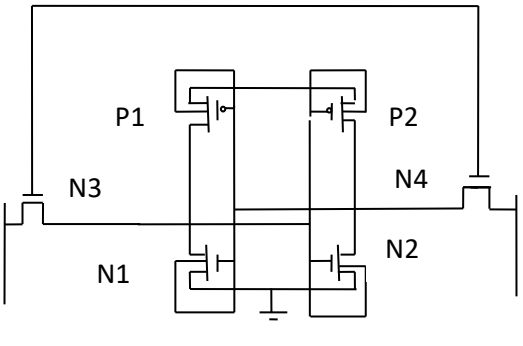
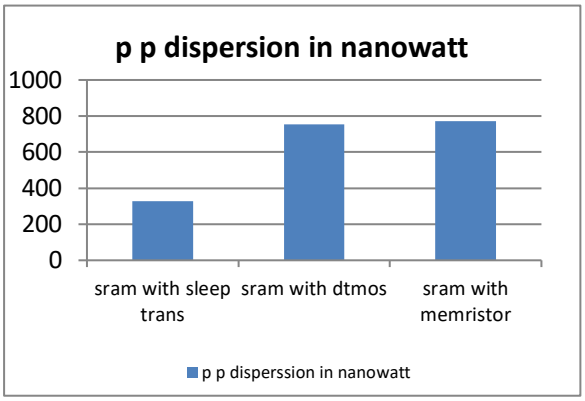
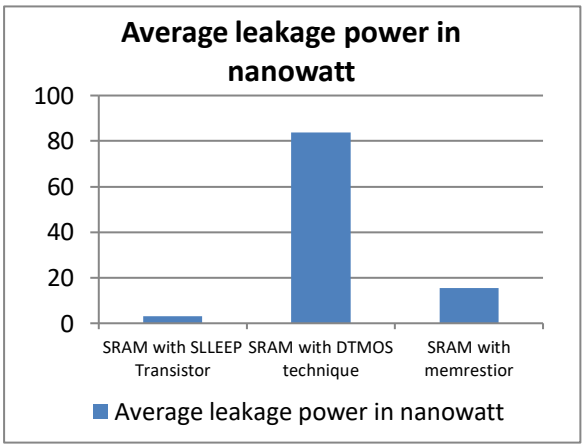


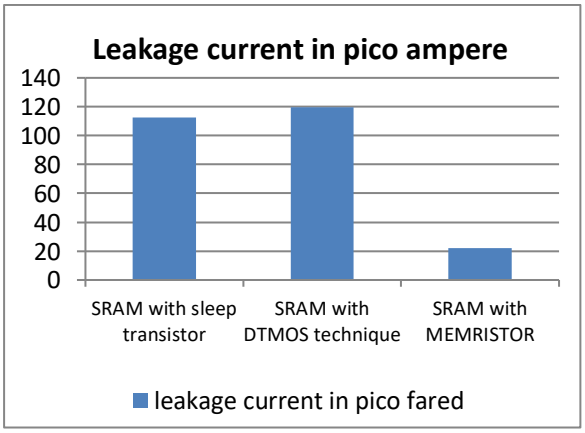
Fig. 5:Basic 6T SRAM with DTMOS Technique

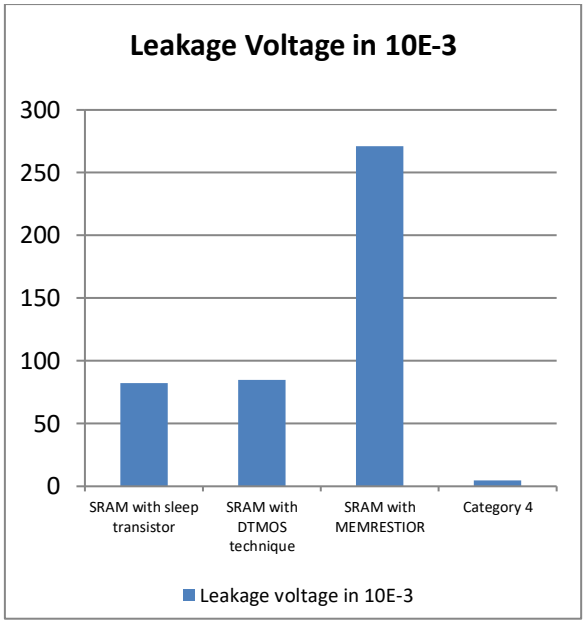
TABLE -1

TECHNIQUE	Peak Power Dispersion	Average Leakage Power Dissipation	Leakage Current	Leakage Voltage
SRAM with Sleep Transistor	329.0E-9	3.084E-9	112.5E-12	82.29E-3
SRAM with DTMOS Technique	754.7E-9	83.85E-9	119.79E-12	84.61E-3
SRAM with MEMRESTIOR	771.7E-9	15.44E-9	22.06E-12	271.1E-3









Conclusion

By studying and comparing the simulation results obtained from implementing the SRAM cell usingDTMOS, sleep transistor and 6 T SRAM with memristor, we can infer the following:

1) For the peak power dissipation, we saw that SRAM with sleep transistor gives better results than other techniques applied on 6 T SRAM.

2) From the results, we saw that the average leakage power dissipation is minimum for the sleep transistor technique.

3) Leakage current is minimum for SRAM with memristor.

4)We have also seen that average leakage power is also minimum for the SRAM with the memristor.

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