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# Optimized Design of Low Power and High-Speed Ring Counter

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***Abstract***

*Sequential circuits have an important role in designing the digital system. As VLSI technologies' growth increases day by day, the main concern for researchers is to implement low power and high-speed sequential circuit with downscaling of chip size. The counter is a basic element to design many applications like timing circuits, memories, frequency synthesizer, and processor. In this paper, the implementation of the 4-bit Ring counter has been done using BICMOS logic. Bipolar and CMOS transistors are combined to make this logic to get advantages of both the logics. Cadence Virtuoso schematic editor and Cadence Virtuoso analog design environment have been used to design the proposed counter's schematic circuit and for the simulation process, respectively. Calculation of power dissipation and delay has been performed for the proposed counter circuit, which is 214.45pw of power dissipation and 73.96ps of delay, then compared these results with previously designed counter circuit results. Performance analysis has been done based on this comparison by which we can conclude that the proposed counter circuit has low power dissipation and high speed compared to prior implemented counter circuits.*

**Keywords:** *BICMOS, Master-Slave D flip flop, Latch-up, Cadence, Ring counter.*

## I. INTRODUCTION

In digital systems, the counter plays a very vital role. Whenever an event happened, counters follows a particular pattern sequence. So when the clock is 1, the present state of the counter replace with the next state. As in the recent era, the main concern for any VLSI circuit is to reduce power dissipation with downscaling of chip size. Ring counter has a unique counting sequence that uses a shift register that contains flip flop that cascaded to circulate a bit 1 through all flip flops. Therefore, the output of the previous flip flop decides the input of the next flip flop. We need to set external input pre-set to the first flip flop while other flip flops are cleared. Here a 4-bit Ring counter has been implemented with the use of BICMOS logic, and calculation of power dissipation and delay has done for this proposed circuit. When we compare these results with previously implemented research results, we can get an efficient counter circuit with low power and high speed. Cadence EDA tool has been used to implement this circuit. As BICMOS logic combines CMOS and Bipolar transistors, it is used to design high speed and reduced power circuits. Compared with BJT, the CMOS transistor has low power dissipation, but this circuit has some drawbacks like high propagation delay and latch-up condition. BJT has some benefits compared to CMOS logic, like high current driving capabilities and high speed. When we use a combination of both the logic, BICMOS logic, the latch-up condition can be eliminated, and also we can jointly use the advantages of both BJT and CMOS logic. [1]

In previously implemented work, many techniques have been used for designing a counter circuit that aims to increase the speed and reducing power dissipation.

In [1], Divya Bora et al. used the Tanner EDA tool to design digital circuits like logic gates and adder circuits with BICMOS logic. Because using this logic circuit has the benefits of high gain, large current driving capabilities, low static power, and fast switching. The use of this logic can also remove the Latch-up condition.

In [2], Sandeep Thakur et al. implemented a ring counter with the Cadence EDA tool using 45nm CMOS technology. For design simulation multimode simulator has been used. Master-slave D flip flop is used to design a proposed counter circuit. This proposed ring counter has 219.85pw power dissipation and 5.216ns of delay. In [3], Tanushree Doi et al. proposed a ring counter using CMOS logic at 90nm technology in the Cadence tool. Pulse latch technique has been used to design this counter for reducing the power dissipation. This counter circuit needed less number of transistors as compared to the conventional counter circuit and has a power dissipation of 167µw & a delay of 51.49ps.

In [4], Ankita Mahajan et al. implemented an area-efficient ring counter using CMOS logic; also, comparison analysis has been performed using three layout designs that are auto-generated, semi-custom, and fully custom. They concluded that full custom the approach has reduced area up to 43% as compared to the auto-generated layout.

In [5], Abhishek Rai et al. designed a 4-bit Johnson ring counter with the following design accents: high speed, cost-effective and low power. A negative edge-triggered D flip-flop has been used to design this circuit. Microwind tool has used for performance

analysis by comparing auto-generated and semi-custom layout design has a power dissipation of 25.095µw result from auto-generated layout design and power dissipation of 139µw result from the semi-custom layout design.

In [6], Ranjana Yadav et al. implemented a counter circuit using MTCMOS technique aiming to reduce power. Calculation of power dissipation has been done at some frequencies and compared with conventional circuit results. In [7], M. R.Sangameswari et al. implemented a counter with D flip flop and dual-mode logic at 90nm technology using the Tanner EDA tool. This circuit is efficient in terms of power and delay.

In this paper, a Ring counter has been implemented using BICMOS logic. Section 2 explains the proposed counter circuit. Section 3 shows implemented schematic diagrams of the counter along with its components using Cadence Virtuoso schematic editor. Section 4 showing simulation results and their analysis. Section 5 concluded the paper.

## II. PROPOSED COUNTER

The proposed Ring counter circuit is shown in figure 1. In this circuit output of the last flip flop has given to the input of the first flip flop. Throughout the circuit, the Ring counter transfers the same output, which means if the output of the first flip flop is 1, it will transfer to the next stage, i.e., the second flip flop. This process will be continuing for all the stages. For a 4-bit ring counter, if the initial flip flop has a value of 1000, then successive patterns are 1000, 0100, 0010, 0001, 1000. With every triggering edge of the clock ring counter stage is evaluated. Here 4 D flip flops are in cascade to design this ring counter, so its mod count is 4. The output of the first flip flop has given as the input to the next flip flop and so on. The output of the last flip flop has been given to the input of the first flip flop.

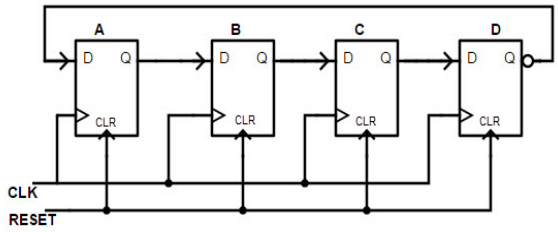


**Figure 1: Circuit diagram of a Ring counter**

Master-slave D flip flop is shown in figure 2. Clock inverter is using for holding the output, and by the use of either clock and inverted clock, inputs can be disabled. To prevent glitches at the gate node of the device, PMOS MP3used at the input terminal. When input=0 and clock=1, then there may be glitches. This eliminated the requirement of a clocked inverter at the input terminal [8]. By using this phenomenon, delay and area of the circuit can be reduced. A feedback inverter has been used for controlling the PMOS in the feedback switch. Pull down section has been used to steer the NMOS; all this is used to shunting the BJT. The clock and the input direct two switches connected in series. Because of any reason, if clock skew occurs, it will still not affect the BICMOS circuit.[10]

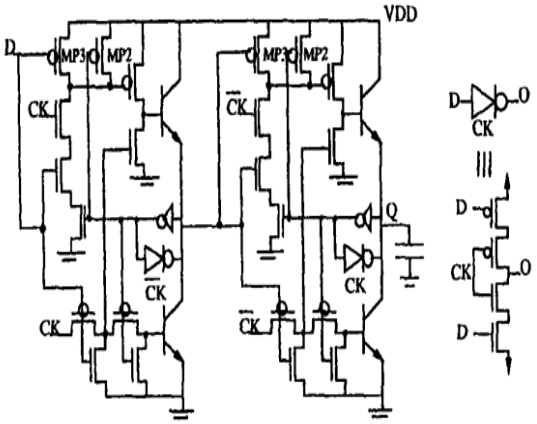


**Figure 2: Master-Slave D flip flop designed by using BICMOS logic**

## III. SCHEMATIC DESIGN

For designing the schematic diagram of the Ring counter, we are required to design all its components individually then simultaneously use all of them. [9] Schematic diagram implementation of NOT gate AND gate, XOR gate, and Ring counter has done with Cadence Virtuoso schematic editor using BICMOS logic along with successive specifications: Length L=180nm, Width W= 2 µm. The most significant flip flop's output drives the input of the least significant flip flop. Along with the reset circuit, the same clock is associated with the design to make a synchronous ring counter. Whenever required, it will start the count with an initial state of 1000.

Figure 3 showing the schematic design of the NOT gate. Figure 4 showing the schematic design of the AND gate. Figure 5 showing the schematic design of the XOR gate. Figure 6 represents the schematic design of the Ring counter, which has implemented using all the above schematic diagrams.

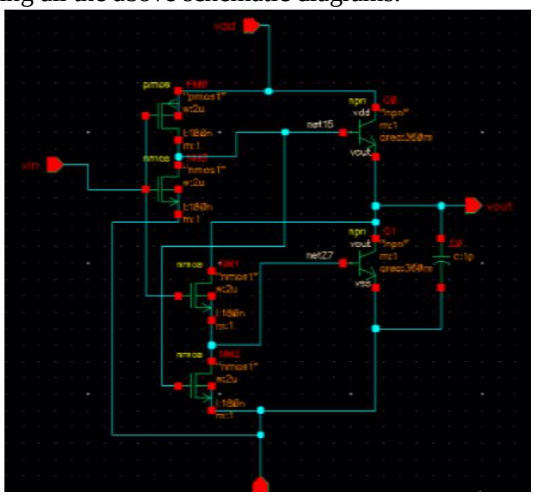

**Figure 3: Schematic design of Inverter**

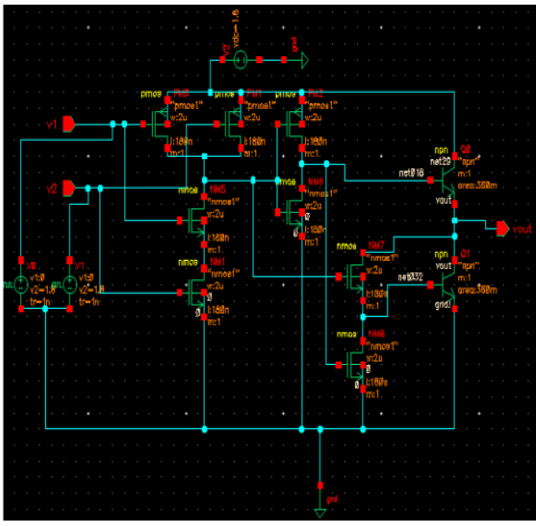

**Figure 4: Schematic design of AND gate**

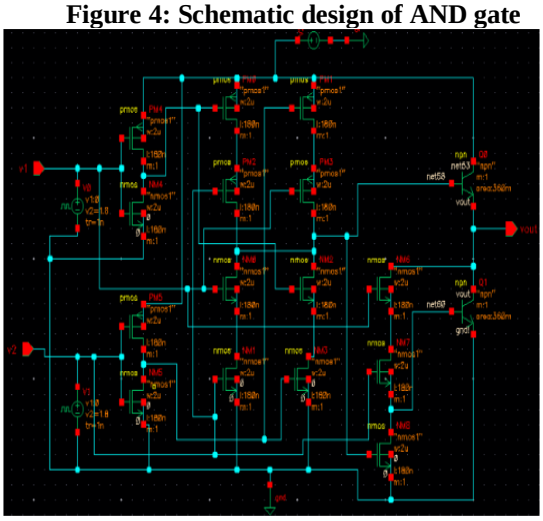

**Figure 5: Schematic design of XOR gate**

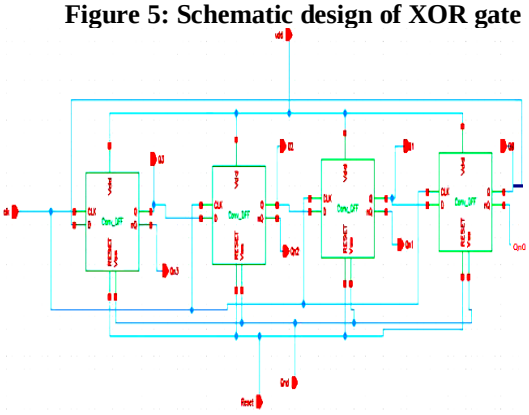

**Figure 6: Schematic design of Ring counter**

## IV. SIMULATION RESULTS

Cadence design environment has been used to simulate the proposed counter circuit with its individual components. Using simulation results of proposed circuits, we will demonstrate the transient response.

The transient response clearly shows that in all the flip-flops of the ring counter, only bit 1 is circulating. In the design, Q0 is the most significant bit, and Q3 is the least significant bit. Calculation of delay and power dissipation of the proposed counter has been calculated using transient responses. With the help of simulation results, we can also get transistor count. Performance analysis of the proposed ring counter has been done by comparing its results of delay and power dissipation with previously researched results. Table 1 showing this comparison.

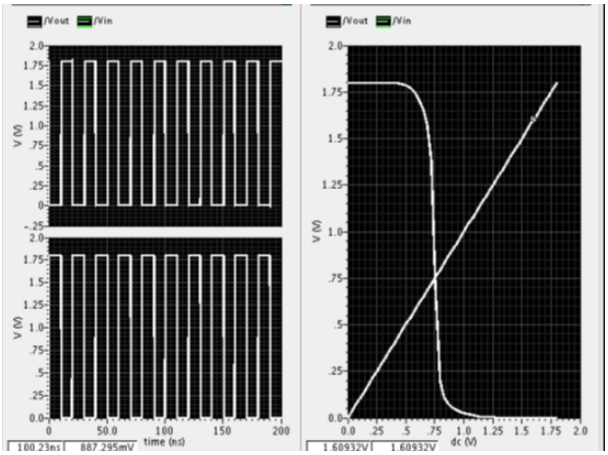


**Figure 7: Simulation waveform of Inverter**

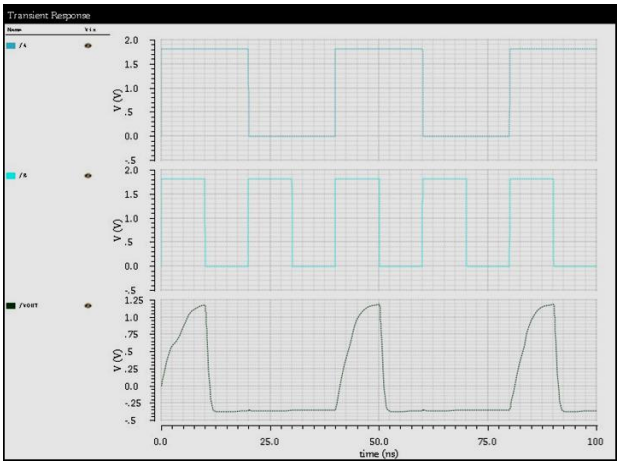


**Figure 8: Simulation waveform of AND gate**

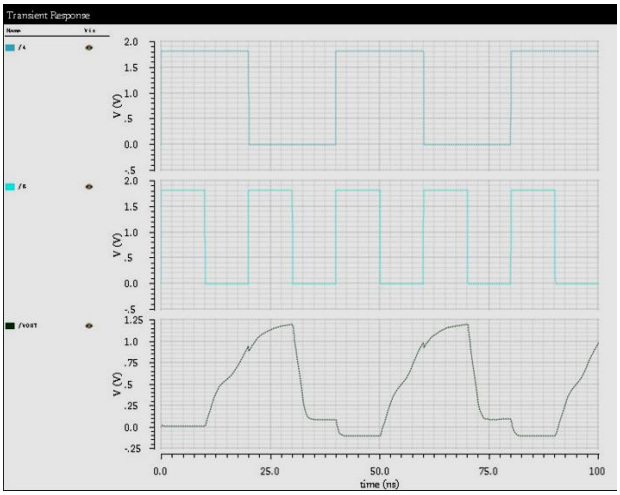


**Figure 9: Simulation waveform of XOR gate**

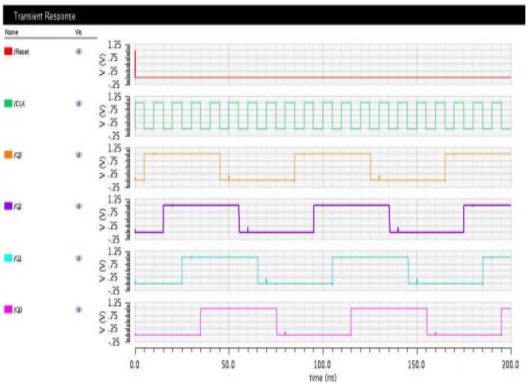


**Figure 10: Simulation waveform of the counter**

**Table 1: Performance analysis of Proposed Ring Counter**

| Parameter | Ring counter using pulsed latch technique | Proposed Ring counter |
|---|---|---|
| Power Dissipation | 610.8µw | 214.45pw |
| Delay | 78.48ps | 50.96ps |

## V. CONCLUSION

In this paper, a 4-bit Ring counter is implemented using master-slave D flip flop, which is efficient in terms of power dissipation and delay. BiCMOS logic is used to design this proposed counter. Parameters of the proposed counter have compared with prior implemented counter results, as shown in table 1. Based on this comparison, we can conclude that the proposed counter has low power dissipation and low delay. Therefore, the proposed counter design is suited for power-efficient and high-speed VLSI designs. This can be useful in designing processors, digital to analog converters, memories, timing circuits.

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