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Characterization of Organic Inverter

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Abstract:
In this paper, the transport properties of pentacene thin films are studied, the carrier mobility is determined using the space charge limited current (SCLC) method. After we have demonstrated the realization of the ''diode load inverter'' with two transistors of P-channel type having different channel lengths. The use of two different channel lengths allows the drive transistor to unload the load transistor effectively in the inverter. The load transistor has a channel length of 250 µm and mobility of 0.04 $cm^2.V^{-1}.s^{-1}$, where the drive transistor has a channel length of 50 µm and mobility of 0.02 $cm^2.V^{-1}.s^{-1}$.The fabrication technique used is simple and allows broad integration. This inverter's performances are given in terms of static input-output characteristics, and they are comparable to that of a complementary organic inverter.

Keyword—*Thin Film Transistor, Pentacene, Inverter.*

I. INTRODUCTION

The organic thin-film transistors are expected to replace their counterpart based on amorphous silicon as soon as long-term stability will be demonstrated and small switching times will be reached. Encapsulation and decreased channel length already allow organic electronics to compete with thin-film inorganic electronics. Low-cost manufacturing processes employing low temperature motivate the use of organic materials[1]: plastic electronics offers the possibility of using a based solution process, allowing to implementation of printing techniques on flexible substratum when inks are formulated[2]–[4]. Despite its limited performance and stability problems, organic electronics have applications, especially as new generations of labels, displays[5], e-papers[6], [7], sensors, and radio-frequency identification tags [8]. The thin-film transistor also appears in the logic circuit where inverters are the key elements [9].
In this study, we demonstrated the realization of an inverter circuit composed of two Organic Field-Effect Transistor(OFETs) in "top contact" geometry. The transistors are based on pentacene with Poly (methyl methacrylate) (PMMA) as the gate dielectric. The inverter's performance is studied in terms of the geometry of contacts (length and width of the channel) and transport properties of pentacene.

II. EXPERIMENT

The inverter in**Fig.1** is realized on a glass substratum covered with indium tin oxide (ITO). The gate electrodes are etched in the ITO, the gate dielectric layer (PMMA) was spin-coated and then annealed at a temperature of about 120°C for 60 min. We set the thickness of the PMMA layer at around 1µm after calibration of the spin speed. The organic and metal layers were deposited by vacuum thermal evaporation. As with other materials deposited by evaporation, low-speed evaporation causes impurities in the film; a rather too fast deposition rate induces structural defects. The pentacene layer is always deposited at an optimized speed of 0.1 nm/sec in this study. The thickness of pentacene is about 50 nm to optimize the characteristics of the top contact transistors. The two transistors' electrodes are made of gold, evaporated through a shadow mask as the gold-pentacene contact is ohmic. The channels are 50µm and 250 µm length and 3 mm in width. After this realization, we make the connection between the two transistors, as in**Fig.1**.
A 150 nm-thick pentacene film was sandwiched between an ITO anode and an Al cathode on the glass substrate for the study of the pentacene film's charge transport properties.

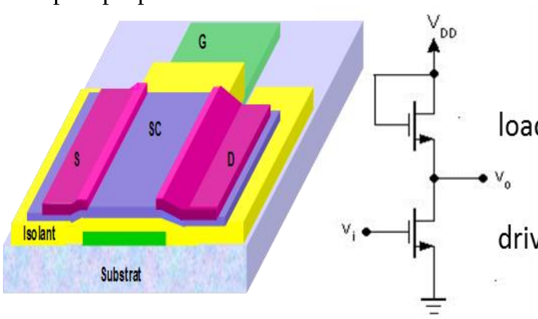

Fig.1: a) Pentacene OFETs fabricated in top contact geometry b) the diode load inverter.

III. RESULT AND DISCUSSION

A. Transport proprieties of pentacene:

The SCLC method was used to precise the electrical characteristic of the pentacene. We consider that the conduction occurs by localized traps. We followed Pool Frenkel's model, which shows that the active layer's polarization by an electric field release trapped electrons and increases the current density as a function of the electric field[10]. **Fig.2**shows current density versus voltage (J-V) in a logarithmic scale, four regions can be distinguished:

The first region, for V<0.5, is the ohmic region. In this regime, the carrier density (n_0) can be determined from the relation:

$$n_0 = \frac{9\varepsilon\varepsilon_0 V_\Omega}{8qd^2}$$

where ε is the permittivity, d the thickness of the pentacene film and$V_\Omega = 2.5 \times 10^{-2} V$is the transition voltage corresponding to the intersection of the ohmic regime (J_Ω) with the SCLC regime without traps. for ε=4 and d=150 nm, we obtain $n_0 = 2.7 \times 10^{20} cm^{-3}$.

For 0.5< V< 1.2 V, the second region is described by the space charge limited current with traps.

For 1.2 < V < 2.6 V, the third region is defined by the trap filling limited current. From this region, we can determine the traps density N_t by using the Poisson equation:

$$V_{TFL} = \frac{qN_t d^2}{2\varepsilon\varepsilon_0}$$

then

$$N_t = \frac{2\varepsilon\varepsilon_0 V_{TFL}}{qd^2}$$

Where V_{TFL} is the transition voltage when all the traps are filled.

We obtain a trap concentration of about $N_t = 3.61 \times 10^{16} cm^{-3}$.

For 2.6 V <V< 10 V, the fourth region is an SCLC regime where all the traps are field. From this region, we calculated the mobility (µ)using the equation:

$$J_{SCLC} = \frac{9\varepsilon\varepsilon_0 \mu V^2}{8d^3}$$

Thus, from the logarithmic scale representation of the current density versus voltage for the ITO/pentacene/Al structure (**Fig.2**), we can easily calculate the mobility in the SCLC regime of the fourth region, which is about $1.4 \times 10^{-5} cm^2.V^{-1}.s^{-1}$(it is the volumemobility that is different from the mobility of accumulated carriers by field effect).

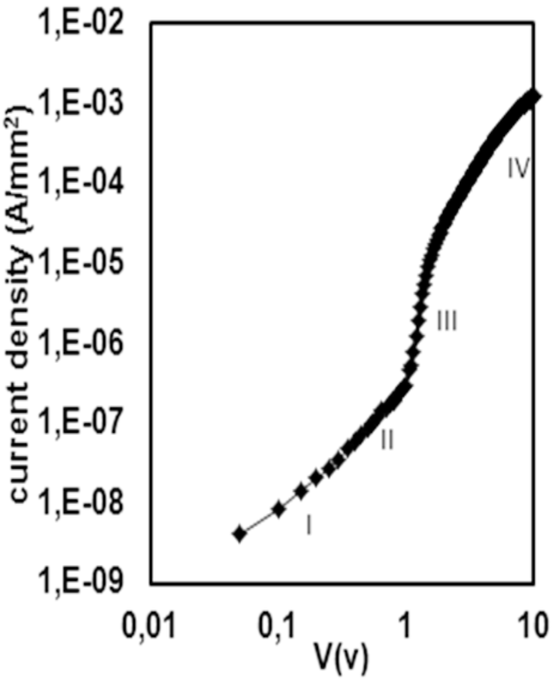

Fig.2: Current density-voltage characteristic of an ITO/pentacene (150nm)/AL.

B. Organic inverter:

To overcome the problems of reproducibility, each transistor was characterized individually. The electrical characteristics of the OFETs were measured under ambient conditions after the fabrication. The field-effect mobility and the threshold voltage can be extracted from the transfer characteristics of the transistor; in the saturation region, the field-effect mobility is calculated by:

$$I_{ds}^{sat} = \frac{WC_i\mu_{sat}}{2L}(V_{gs} - V_{th})^2$$

Where W and L are channel width and length respectively, Ci is the capacitance per unit area (C_i=2.3 nF.cm^{-2} per 1 µm PMMA), V_{th} is the threshold voltage of the transistor.

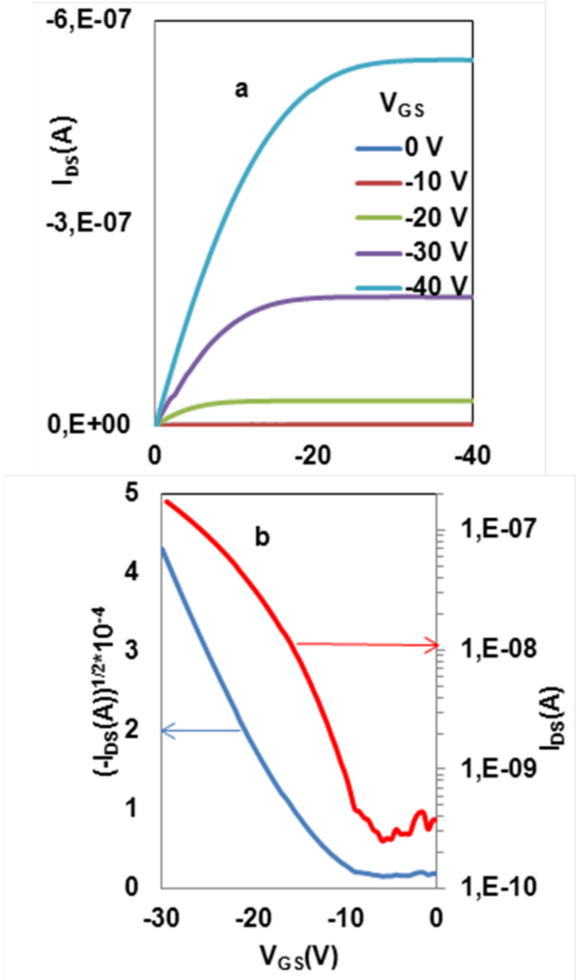

Fig.3: (a) output characteristics of the load transistor (b) the transfer characteristics of the load transistor for V_{DS}= -40 V.

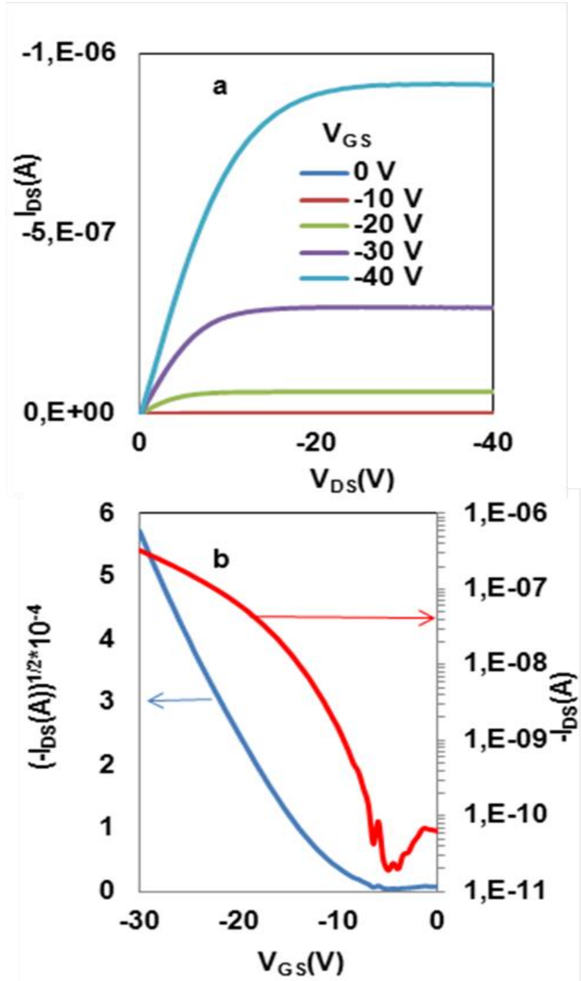

Fig.4: (a) output characteristics of the drive transistor (b) the transfer characteristics of the drive transistor for V_{DS}= -40 V.

In **Fig.3**we present the characteristics of the drive OFET with L_{load} = 250 µmandW_{load} =3 mm, µ=0.04 $cm^2.V^{-1}.s^{-1}$ and V_{th}= -15 V and the current ratio I_{on}/I_{off} = 10^3.

Fig.4show that µ = 0.02 $cm^2.V^{-1}.s^{-1}$ and V_{th}= -12 V and the current ratio I_{on}/I_{off} =10^4 for the load OFET L_{drive} = 50 µm and W_{drive} = 3mm. The shift of the threshold voltage to the positive voltages is related to reducing the length of the channel, and thus the number of carriers passed through the semiconductor is more important because the transit time decreased (tr∝ L2) with the constant field. Such behavior can be explained by lowering the potential barrier in the depletion regime at the interface drain/semiconductor [11], promoting the injection of holes.

In **Fig.5**we present the voltage transfer curve of the diode load inverter for a supply voltage V_{DD}= -30 V. In this case, when V_{in}= V_{DD}, the V_G of both the driver and the load transistor are initially equal to V_{DD}. The driver transistor has to be able to pull up the output node. On the other hand, when the input V_{in}=GND, the load transistor will be at first heavily ON and will easily pull down the output node against the driver transistor, almost OFF. Some important terms in the static input-output characteristics of an inverter are the separation of logic high and low level, the maximum gain defined as$(\frac{dV_{out}}{dV_{in}})max$of the diode load inverter is 4.5, the noise margins at a high level $NM_H = (V_{OH} - V_{IH})/V_{DD} = 40\%$and at the low level$NM_L = (V_{IL} - V_{OL})/V_{DD} = 13\%$. The results obtained are consistent with those found by H. Klauk[12] for the same structure of the inverter(maximum gain=2.1 and noise margin=0.5V). The performance of the inverter, which consist of two P-channel transistors in term of separation of logic level and maximum gain and noise margin comparable to that of complementary organic inverter [13] and ''V_{GS}=0'' inverter [14], [15].

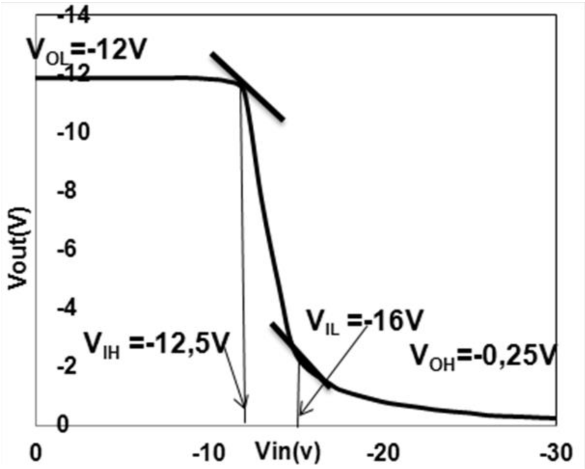

Fig.5: Transfer of the diode load inverter. The input Vin scanned from 0 to -30 V with a supply voltage of -30 V.

IV. CONCLUSION

Using a simple fabrication process, we succeed in this study to fabricate the organic inverters using the top contact transistor with P-channel. Our investigation of the transfer characteristics and the diode load inverter's performance showed that this inverter is comparable with the complementary organic inverter, with the simplest fabrication process. For the transport charge proprieties, the values determined with the SCLC method are in good agreement with other studies [16].

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