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A Review of Leakage Power Reduction Techniques for VLSI Applications

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Abstract: *Power dissipation has become one of the VLSI circuit structure's significant worries with the fast launching of battery worked applications. In high-performance structures, the leakage segments of power consumption are equivalent to the switching segment. This will keep incrementing with innovation scaling, except if effective procedures are introduced for controlling the leakage. This paper gives a thorough report, examination, and correlation of leakage power reduction systems and techniques. Additionally, the advantages and disadvantages of different strategies for decreasing leakage power are introduced. These methods can be stretched out to any complex advanced digital implementation.*

Keywords: *Leakage/ Spillage Power reduction, CMOS circuits, Leakage/Spillage current, MTCMOS*

I. INTRODUCTION

With the ongoing developments in VLSI innovation, transistors' requests in Integrated Circuits are yet developing, which requests costly cooling and bundling advancements. Subsequently, because of this, the supplied voltages are downsized for diminishing the power dissipation. Be that as it may, scaling of supply voltage has brought about an exponential increase in sub-threshold leakage current, causing static (spillage) power dissemination. In the present life, the primary spotlight is on low power gadgets on account of development in mobile devices; and however, even before the introduction of mobile devices, power dispersal was an endless issue. Higher power utilization prompts lower execution and reliable quality of the circuit. There are numerous strategies to lessen the leakage power. Static power constitutes about half of the all-out power utilization in the present high-performance chips. As per the need, a decrease of leakage power is the way into a low force VLSI plan.

$$\mathbf{P_{leak} = I_{leak} * V_{DD}}$$

Where,

I_{leak} - When the transistor is OFF, the Spillage current which streams in it.

V_{DD} – Voltage supplied

P_{eak} – Power leaked

The leakage current is directly proportional to the leakage power. Therefore I_{leak} must be reduced to get reduced leakage power P_{leak}. The leakage power commands the dynamic power, especially in crucial VLSI circuits and what's more in the circuits that leftover parts in the inertly mode for an extended time, for example, cell power. In real life, every application draws out the battery life anyway. With a developing pattern towards portable computing and remote communication, power dissemination has turned out to be one of the most basic components. In this way, the primary spotlight is on the decrease of leakage power.

As the technology pattern took another stage, leakage power expanded exponentially with more transistors' reconciliation on the substrate. The leakage power is said to be that static force scattered when there is no useful outcome from the current or when the circuit is out of gear state. When gate voltage (Vg) in the transistor is lower than the Vth, i.e., threshold voltage, the transistor can't be totally turned off, which prompts little current flow called **leakage current**. The key sources of leakage/spillage current in CMOS transistors are as follows:

1. Reverse-biased junction leakage current
2. Gate induced drain leakage
3. Gate-direct tunneling leakage
4. Subthreshold (weak inversion) leakage current

The sub-threshold current flow stream is considered the most supernatural among all the spillage current flow sources, which ends up going after exploring in the present and future silicon advancements. This paper gives a comprehensive

examination of systems and techniques to diminish power in VLSI circuits.

II. Review of Related Work

High spillage current has changed into a gigantically of force dispersing of submicron VLSI circuits since the edge voltage (V_{th}), length of the channel, and door oxide thickness are said to be decreased. There are different methodologies for spillage current decrease. All of these systems are persuading in diminishing spillage power lastly completely boiled down to the essential idea: spread is reduced by chopping down stock voltage, actual capacitance, trading development, swinging voltage. Another method is by introducing a peak impediment way among V_{DD} and ground.

At the point when flexible voltage level circuits are thought of, the circuit's threshold voltage is related with any of the stack circuit [4]. The most outrageous supply voltage is supplied by the circuit to the load circuit for quick operation when in either dynamic or active mode. The transistors which are weakly ON provide lower V_{DD} to the stack circuit when working in hold mode. The moment when the channel to source voltage is lessened, channel induced obstruction in bringing down/drain incited barrier lowering (DIBL) sway is reduced, and this consequently fabricates the V_{th} of NMOS transistors. In this manner, the sub-threshold spillage current in the OFF MOSFETs reduces, thus spillage power gets restricted, and the information is held.

The procedure of turning off the gadgets by removing their supply voltage, leading to leakage power control, is called Power Gating [5]. This methodology uses some more resting transistors that are implanted in the course of action between supplied power and pulled-up framework or might be in between pull-down framework & ground for the reserve spillage currents reduction When the circuit is working in dynamic mode, and the sleeping transistors are whereas they are switched-off when the circuit is available for reserve mode.

Another strategy in which the dependence of spillage current on the data vector to gate is used is called the Input Vector strategy [6]. Extra control logic is utilized to put the circuit in a low-spillage backup state when inactive & reestablished to one-of-a-kind states when reactivated. When reactivated, the circuit never again holds the essential state data prior to going into a low-spillage save state. In this way, for holding the state information, it requires phenomenal latches/hooks, which grows the zone of the given circuit (area of the circuit) by around multiple times in most awful situations.

The semiconductors of various limit voltages are said to be utilized in the Dual edge voltage CMOS system. Low limit voltage semiconductors are utilized for entryways on essential methods for keeping up the show, whereas the high edge voltage semiconductors are utilized for the doors on the non-major course for diminishing of spillage current.

The semiconductors of various cutoff voltages are utilized in the Dual edge voltage CMOS framework. Low breaking point voltage semiconductors are said to be utilized for entryways in this fundamental strategy for keeping up this show, whereas, on the other hand, high edge voltage semiconductors are utilized for the doors on the non-major course to diminish the spillage current.

III. SPILLAGE POWER

Also known as Leakage Power in VLSI circuits. Two sorts of power utilization are there in the CMOS circuits:

1. Static Power Consumption: This power utilization is leakage power, which has a conspicuous job in complete power utilization.
2. Dynamic Power Consumption: This power utilization is unavoidable to wipe out as a result of exchanging and registering movement.

Static power dissipation is due t**o Junction leakage** – source to drain to the substrate through reverse biased diodes, **Gate induced tunneling leakage** – leakage through the oxide layers above the substrate which acts as an insulator, **Sub threshold leakage** – leakage current of a transistor when working in a region of weak inversion. Thus, the biggest leakage in CMOS circuits happens as a result of lower threshold voltage in the present-day CMOS circuit.

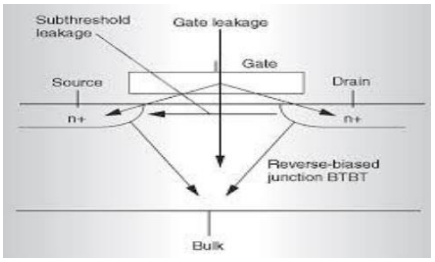

Fig 1: Types of Leakages in CMOS Circuit [1]

IV. TECHNIQUES FOR LEAKAGE POWER REDUCTION

There are numerous techniques or methods for the reduction of leakage power based on system operation modes.

Two operation modes are:

A. ON mode
B. OFF/Sleep mode

Generally, power reduction methods work on the basis of cutting-off down the supplied power V_{DD} to the system in OFF mode.

A. VTCMOS - Variable threshold CMOS:

The VTCMOS method includes progressively adjusting the V_{th} (threshold voltage) during dynamic mode that is traditionally called the reserve control decrease. VTCMOS technique includes the increment of the limit voltage (Vth) in reinforcement mode by interfacing the substrate voltage either lower than (for N semiconductors) or higher than ground (for P semiconductors). It is discovered that the only drawback of VTCMOS is that an additional power supply is required in this technique that might not fit in most of the business structures.

B. DTMOS - Dual threshold CMOS:

In DTMOS, high-threshold voltage transistors are utilized to decrease the spillage power. To keep up circuit execution on essential ways, low-edge semiconductors are used. Subsequently, this system requires a count of filters for the entryways where the high-Vth contraptions can be used [7]. This framework has been comprehensively known as the Dual Vth CMOS technique. In DTMOS, the entryway, as well as the body of every semiconductor, is incorporated with the objective that the spillage/spillage is least if the semiconductor is in an OFF state. The current will be high when the semiconductor is in an ON state.

C. SC-CMOS - Super cut off CMOS:

A procedure called [9] SC-CMOS is similar to MTCMOS appeared in Fig.2. According to Super cut off CMOS, in the reserve/standby mode, Gate to source voltage of resting semiconductors are PMOS or NMOS, and accordingly, this overdriven component supports the level of standby current. . Additionally, the captivating component of SC-CMOS is that the resting semiconductors have low limit voltage (Vth) which is comparable to the Vth of organized reasoning circuit. Along these lines, the lower Vth ensures quick assignment of reasoning circuits.

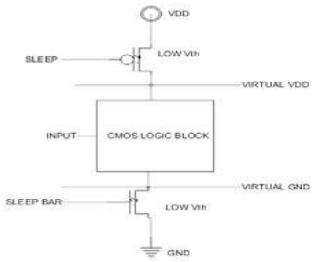

Fig 2: SC-CMOS – PMOS structure

D. MTCMOS – Multi threshold CMOS / Power Gating:

Power gating is a technique in which a SLEEPING semiconductor is outlined by putting high limit threshold gadgets in serial arrangement with lower edge semiconductors connecting the supplied power and ground [8], which Fig.3 depicts clearly. In the dynamic mode, resting semiconductors are turned ON, with the goal that ordinary working isn't influenced since there is a route in between the supplied power and ground. While talking about the backup mode, the resting semiconductors are said to be shut down, subsequently closing down the $V_{DD,}$ making virtual stockpile as well as ground rails. This strategy is predominantly known as SLEEP TRANSISTOR.

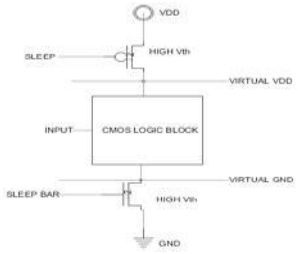

Fig 3: MTCMOS Structure

E. Sleepy stack:

The sleepy stack technique [11], as appeared in Fig.4, is the same as the Forced stacking method. In Sleepy stack methodology, constrained stacking is said to be utilized in the beginning, and it is sought after by the expansion of resting semiconductor in corresponding to one of the stacked semiconductors. In the dynamic mode, the 2 transistors connected in parallel are switched-on in this manner, compelling opposition of the way to decrease. Thus, it outcomes in less propagation deferral or delay. While in the backup mode, the reset transistor is switched-OFF, and the leakage power is decreased by the stacked transistor.

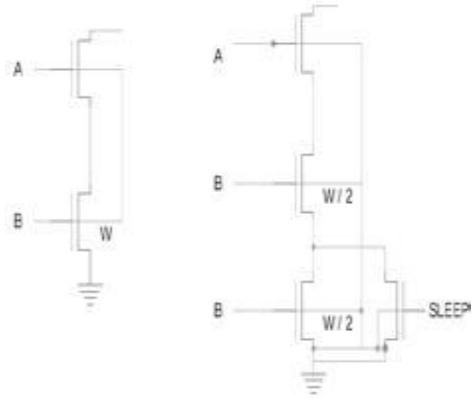

Fig.4: Sleepy Stack

F. Sleepy keeper:

A sleepy keeper is an approach [12] in which one extra pull-down semiconductor is set in parallel connection to the pull-up resting semiconductor associating supply voltage to the pull-up system, which is Fig.5 depicts clearly. When sleeping, i.e., the rest semiconductor is in an off state, the

main wellspring of supplied voltage to pull-up system is the NMOS transistor. Also, to the existing pull-down rest transistor, one extra single PMOS transistor is put in parallel connection, which turns into the main wellspring of ground to the pull-down system. To keep up an estimation of "0" / "1" in resting state, as given that "0"/"1" has just been determined, this methodology utilizes the yield/output estimation of "0"/"1" for PMOS transistor associated with the ground to keep up yield equivalent to "0" or NMOS transistor associated with V_{DD} to keep up yield worth equivalent to "1" individually in rest mode.

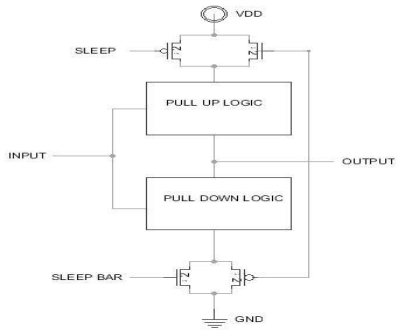

Fig 5: Sleepy Keeper

G. Transistor stacking:

A strategy that is used in the dynamic mode for reducing the leakage power is called Transistor Stacking. Also, the detailed significance of the stack impact is studied and mentioned by Siva et al. [10]. The leakage current is said to be declined when at least 2 arrangement transistors are switched off, which is known as Self-Reverse bias or Stack impact. The transistor stacking impact misuses the reliance of sub-threshold current, and the sub-threshold leakage current is reduced exponentially due to the expansion in the source voltage (V_s) of the transistor. Circuits with no stacking structures can use the constrained stacking method easily. In the constrained stacking, 2 transistors with width "W/2" can be used to supplant a single solitary transistor having width "W" as appeared in Fig. 6. As a result, when two transistors are turned-off in the meantime diminishing leakage current.

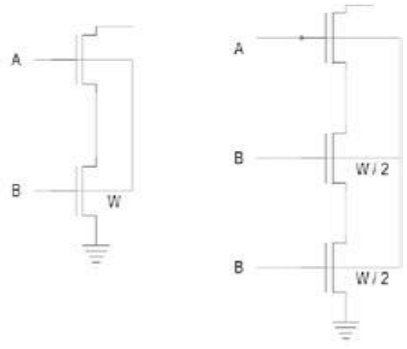

Fig 6: Forced stacking

V. RESULTS

These days in VLSI advanced structure, particularly for portable frameworks and high-performance frameworks, low power and rapid speed is a significant thought. The decrease of the transistor size permits a high incorporation thickness. In numerous applications, wherein the circuit stays in the idle state for longer-term, a decrease in standby power is a serious issue.

The utilization of the leakage feedback method has risen as a viable method to accomplish high performance and low power plans. Based on investigating different procedures of decreasing leakage power, it is discovered that every strategy has its own preferred position just as a disadvantage. These focal points of various strategies are introduced in Table 1. Looking at these, any of the procedures referenced beneath can be utilized in a VLSI circuit for power decrease according to the prerequisite.

Table 1 Leakage Power Reduction Techniques with their Advantages & Disadvantages

Technique	Advantages	Disadvantages
Forced stacking	• Implementation is trouble - free • Leakage saving	Propagation delay is high
Sleepy Stack	When comparison is made with forced stacking, Propagation delay is less	Control circuit is required by sleep transistors
Power gating with stacking	In both operating modes, great leakage savings	Delay is high
Power gating with PMOS and NMOS	• Larger power savings • Best technique of preference	Requirement of control circuit
SCCMOS with PMOS and NMOS	• Power savings are great • Fabrication is simple	Requirement of control circuit

VI. CONCLUSION

Power leakage reduction is an important job in low power submicron circuits. Additionally, considering the above review, obviously, for bigger savings of leakage power, the most favored strategy is Power gating, for example, the Multi-threshold CMOS system. Additionally, the rate decrease of leakage power is more with the MTCMOS method when contrasted with some other strategy. MTCMOS can be actualized on various circuits, and the power, delay, and different parameters can be estimated just as contrasted with different methods.

Also, based on the above review, it is clear that for larger leakage savings of power, the preferred technique is Power gating, i.e., the Multi-threshold CMOS technique. MTCMOS method has the highest power leakage savings in comparison to all the other techniques. MTCMOS can be implemented on different circuits, and the power, delay, and other parameters can be measured as well as compared with other

techniques. The previously discussed and stated procedures of power spillage reduction are appropriate at the circuit level of abstraction till now. Accordingly, in the near future, recently developing procedures to control leakage power at the block as well as gate-level deliberations are a lot of needed to give more power investment funds than the procedures at the present circuit level.

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