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Original Article

RF-Microwave Double-Balanced Diode Mixers as Up-Converter MMIC module in RF Front End Transmitter Section for 5G Communications

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Abstract *- This paper presents design investigations of RF (Radio Frequency) Mixers in three configurations: Single Diode Mixer, Double Diodes based Balanced Mixer, and Quad Diodes based Double Balanced Mixer. Also, results for a comparative analysis of these designs with the Transmission lines implement microwave Balanced Diode Mixer and Microwave Double-Balanced Diode Mixers are shown. Mixer performance metrics such as Power spectrum at ports, Conversion Gain, and Isolation addressing Diode non-linearities are depicted thoroughly. Modeled results and analysis presented here benefit in realizing aneffectiveRFFront End Transmitter on a monolithic stage having minimal co-channel interferences and out-of-band rejection. Mixer operation in Microwave G-band (formerly C-band) encompassing low to mid 5G frequency regime for applications in the New 5G Radio spectrum is detailed exclusively for these conformations.*

Keywords *- 5G Communications, Monolithic Microwave Integrated Circuit (MMIC), Transmission lines, RF front end, Up-Converter mixer.*

1. Introduction

The RF Front End (FE) Transmitter (TX) system of modern Radio architecture encounters an output frequency that is usually higher than the input frequency [1]. Up-Converter Mixers, which are three-port reciprocal networks, are deployed on the TX side for filtering Image frequencies resulting from mixing high Local Oscillator (LO) and low Intermediate Frequencies (IF). This shall then effectively perform cyclic frequency transformations by producing a sum and difference of frequencies due to the frequency multiplication progression. Required IF, which is the difference between RF and LO frequencies, is being amplified in the preceding amplifier stages of the Mixer placement before the Bandpass Filter (BPF).

Various efforts in RF-Microwave Mixer design are referred back extensively during the literature search. For instance, a Single balanced Mixer using the Schottky diode in ADS [26] is briefly discussed in [2], along with presenting the Mixer measurement results. [3] provides a dual-gate FET's based Double balanced Mixer using active and passive techniques fabricated in planar MMIC technology to eliminate the IF removal issues. For millimeter range Mixing [4] depicts the metamorphic HEMT diode and Co-planar Waveguide (CPW). Coupler established a single-balanced diode mixer design. [5] gives analysis and optimations of I-Q FE 1.9 GHz Receivers with Mixers designed through current as bias and transmission gates built on 65 nm CMOS technology. Passive Mixers in CMOS technology for application in Software Defined Radio (SDR) Receivers with BPF are exemplified in [6]-[8] for dynamically programming Radio constraints up to 2.4 GHz. For the definition of Mixer performance metrics and design schematics at 2.4 GHz in ADS [26], referring to [9]-[10] conveys enormous information while [11] highlighting X-band Mixer design using Schottky diodes in SiGe technology. In late 2017, GaAs-based Double balanced Mixers on the MMIC platform addressing the 5G inceptions are cited on a limited basis in literature, as given in [12]-[13] individually. However, they do not address issues emphasizing suitability in integrating the RF TX Front End System model of Fig. 1 or Filter Banks or BPF redundancy in frequency selective applications despite presenting 10 dB Conversion loss.

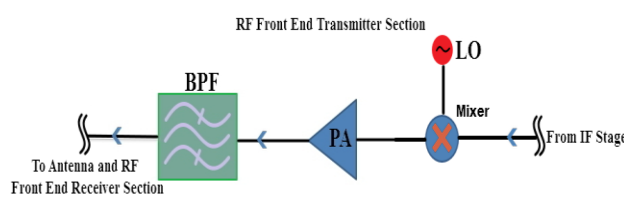

Fig. 1 RFFE TX System Model [21]

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3D Modeling of Transmission lines (TLIN), Microstrip Lines (MLIN), Coupled MLIN (MCLIN), and BPFalong with materials, methods, and FEM formulation for Characteristic Impedance of TLIN to create RF models in ADS [26] are detailed in [14]-[15]. [18]-[20] provide PIN diodes-based design of power limiters without the need for biasing in microstrip technology, validating the application of Schottky diodes and p-n junction theory.

The systematic design of a passive Down-Converter Mixer is provided in [22] using Schottky diodes with ADS [26] RF and Momentum-Microwave suites. Mixer designs using EDA tools such as NI-AWR [16]AWRDE Microwave Office suite incorporating HSMS series Schottky Diodes [17] are initiated in this paper for graphing the Up-Conversion process solely. Presented aspects play a vital role in comprehending the Mixer for the operational TX section of the RFFE in the 5G MMIC Transceiver Chipset outlined in [21].

2. Mixer Configurations

In the Up-Conversion Mixing process, a Double Sideband (DSB) suppressed RF carrier signal f_c = 4.89 GHz results when the RF signals from LO and IF are multiplied, with a mixing order of (LO ± IF) frequencies. Two important metrics for a practical Mixer are Conversion Loss/Gain and Isolation. The ratio of one of the output spectral components in the wanted RF signal to the input IF signal is defined as the Conversion loss of an Up-Converter [1]. For example, a practical Mixer with a 6 dB Conversion loss has a 6.5 dB Noise Figure (NF) due to the NF associated with the Receiver (RX) section [1]. This was the primary reason why the amplifier in the RFFE RX section designed during the investigations in [21] adapted a high Gain value of 9 dB to ensure that the Mixer Noise does not dominate over the RX performance. NF can be approximated conveniently by the Conversion loss factor during Mixer design. After that, the NF simulation alone is done for a Single Sideband (SSB) and all Sidebands in the power spectrum [22] of frequency bands under investigation. DSB NF is relatively easier to quantify, as it is 3 dB less than the SSB NF [22], which is a prominent feature for Mixer characterization.

The isolation, which is converse of the Insertion loss, is desired to be higher between the three ports, i.e., LO, IF, and RF ports of the Mixer. Typical Mixer designs have at least 30 dB isolation [17]. The performance of Schottky diodes-based devices such as RF power limiters is presented extensively in literature depicted through [18]-[20], alongside the diode datasheet of [17].In this paper, a Double Balanced Up-Converting Mixer with Quad Schottky diodes is demonstrated using Bridge topology for achieving a balanced configuration, in that better Conversion Loss and higher port Isolations are deemed. All along the design process, the diode non-linearity has been addressed using the Large Signal S-Parameters at Harmonics and Harmonic Balance Analysis in AWR [16] for the One-Tone excitation scheme to verify the practicality of the designed Mixer.

Single, Double and Quad Schottky Diodes in balanced topology using a low turn-on voltage of 0.34 V at 1 mA [17], HSMS 282-x series diodes are used to study and design an efficient, passive RF Mixer had been modeled using AWRDE Microwave Office (MWO) suites [17] and [16] respectively. To model the device, the 2-port SDIODE [16] of HSMS series are de-embedded using AWR Microwave Office suite tools, and a Double Balanced Mixer layout was generated, which can be tested exhaustively and prototyped if desired using the conventional foundry, microfabrication tools, and available methods. The three Mixer configurations are listed below:

- Single Schottky Diode (SDIODE) Mixer.
- Double Diodes in the anti-parallel arrangement, also known as Balanced Diode Mixer (BDM).
- Double-Balanced Diode Mixer (DBDM) is a diode bridge mixer that uses two single-ended differential center-tapped transformers to attain the multiplication process.

3. Schematics and Simulation Results

3.1. AWR Schematics for Single diode-based Mixer Design

The Mixer was designed using a single Schottky Diode with a Diplexer to separate HF RF-LO from LF IF signals. Diplexer causing IF to RF and IF to LO isolations was executed using Low Pass-High Pass Filter setup.

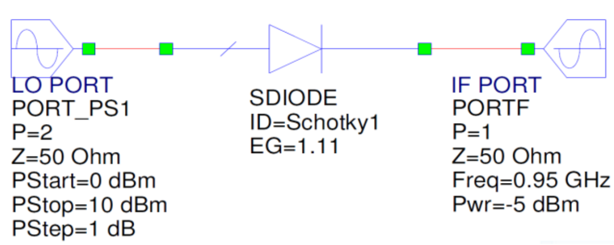

Fig. 2 AWR circuit with two ports of a simple Schottky Diode (SDIODE) [23]

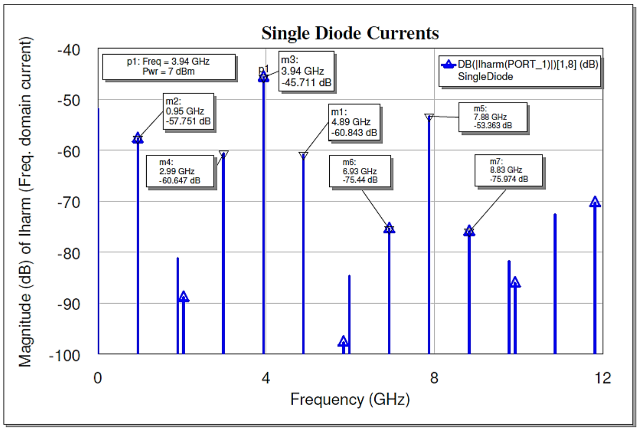

Fig. 3 AWR Rectangular plot of the Current nonlinear spectrum through SDIODE at port 1(P=1) with 7 dBm power at port 2 (P=2), LO sweep frequency of 3.94 GHz, and using AWR Harmonic Balance simulations on Fig. 2

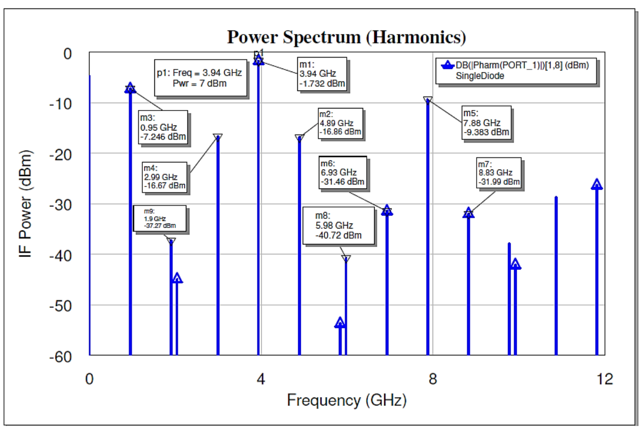

Fig. 4 AWR Power spectrum of port 1 (IF port) with a source excitation of –5 dBm (0.316 mW) vs frequency in GHz, with an input power P_{in} of 7 dBm (5 mW) at swept LO port (port 2) of SDIODE in Fig. 2

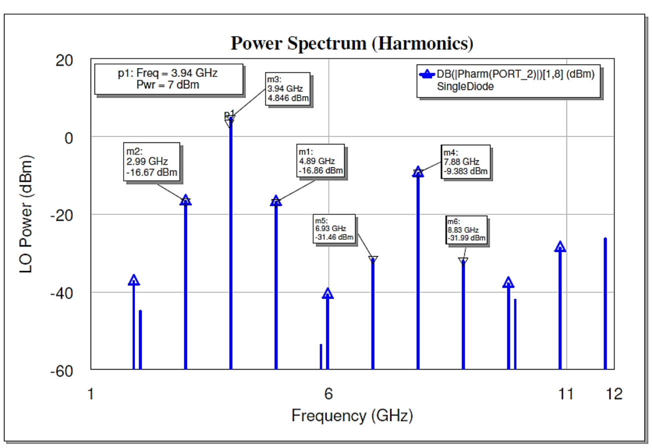

Fig. 5 AWR depictions of frequency components centered on LO (port 2) to signify the multiplication of sum and difference harmonics in the Power spectrum of SDIODE

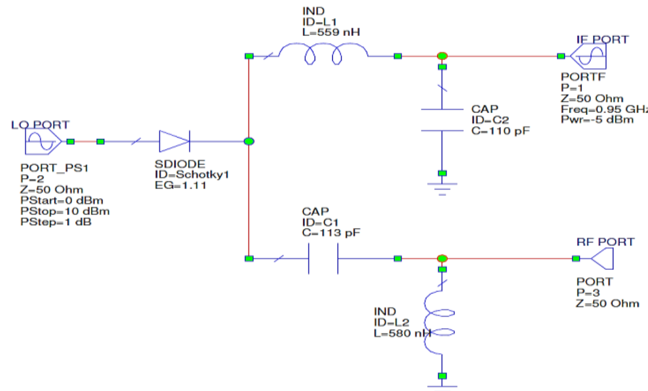

Fig. 6 AWR Diplexer circuit with SDIODE to extract the RF signals from diode current by creating an IF current path separate from RF current. LF components pass through the inductor while RF frequencies pass through the capacitor to the IF and RF ports, respectively [1], [16], [23]

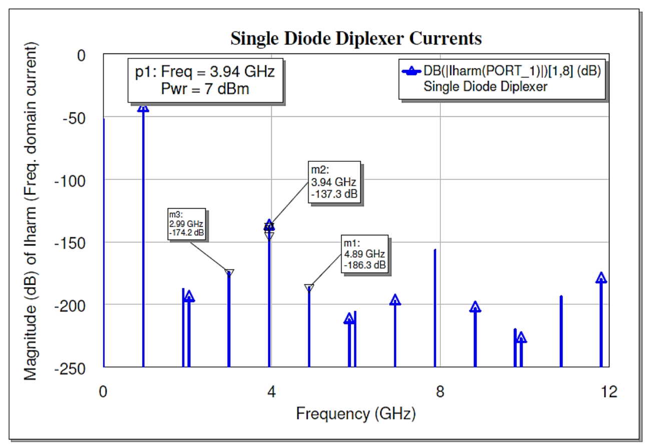

Fig. 7 Spectrum of Current at RF port with excitation of 7 dBm (5 mW) at LO port. Markers depict important dB magnitudes of Iharm [16] around 5 GHz frequencies

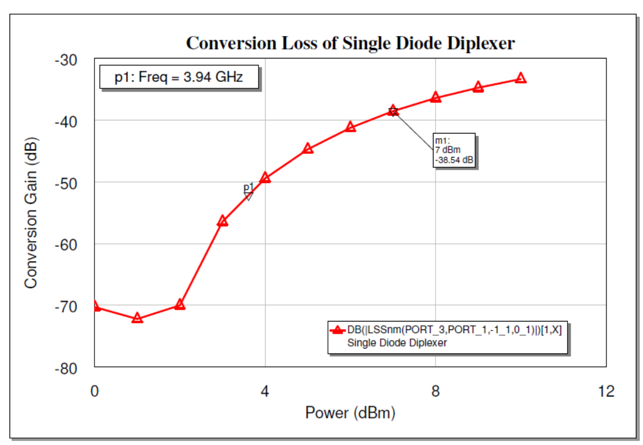

Fig. 8 Conversion Loss (port 1 to port 3) in dB vs. input power P_{in} at LO (port 2) using LSSnm-the "Large Signal S-parameters at Harmonics" [16] for Diplexer circuit of Fig. 6

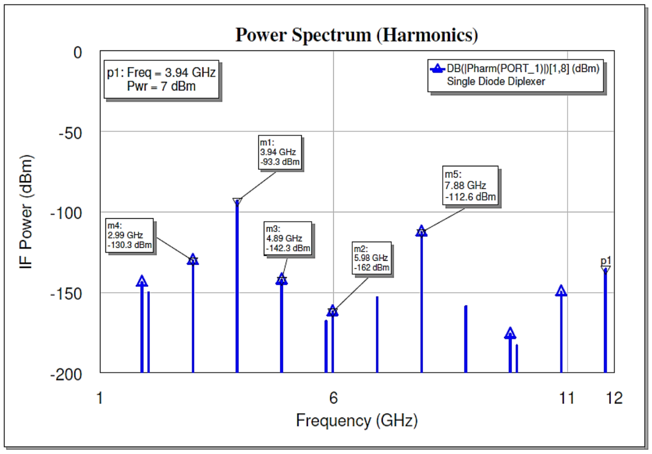

Fig. 9 Plot of the IF spectrum at port 1 to quantify the Isolation between IF to RF ports for the single SDIODE-based Diplexer circuit of Fig. 6

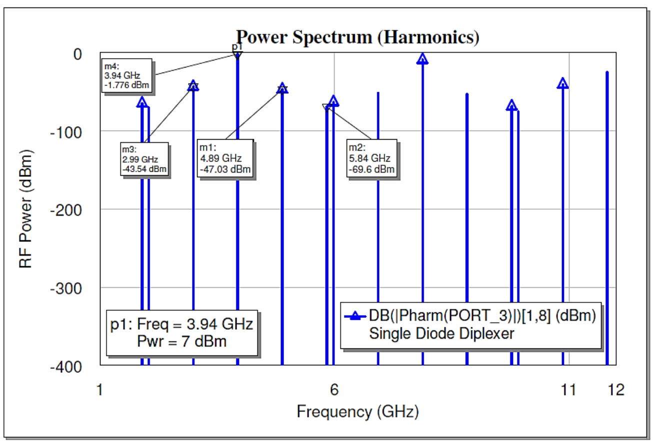

Fig. 10 Spectral components of RF power at port 3 to quantify the Isolation between LO to RF ports for the single SDIODE-based Diplexer circuit of Fig. 6

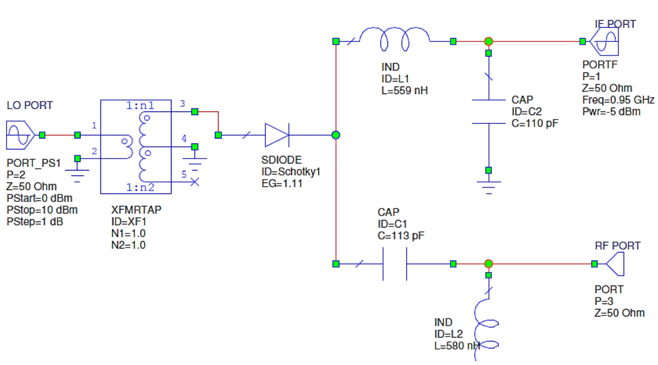

Fig. 11 AWR circuit diagram of SDIODE as an Up-Converter Mixer using a simple 1:1 turns ratio centre-tapped transformer "XFMRTAP" [1], [16], [23]

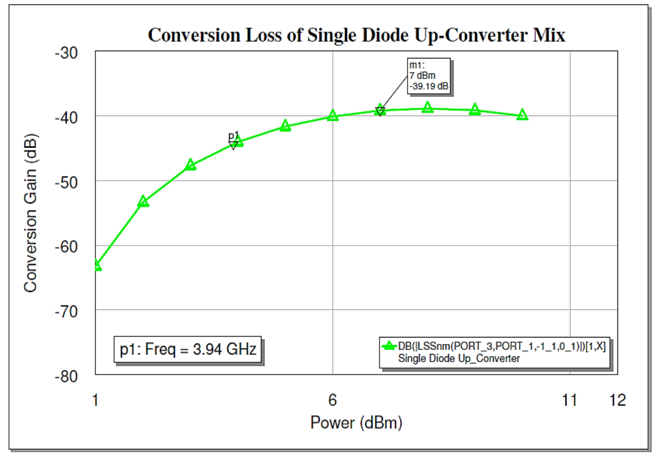

Fig. 12 Conversion losses (port 1 to port 3) in dB as a function of LO power levels for the SDIODE Up-Converter Mixer in Fig. 11. Increasing LO power drive at port 2 results in a Conversion loss decrease. However, high LO source power increases the Mixer power consumption

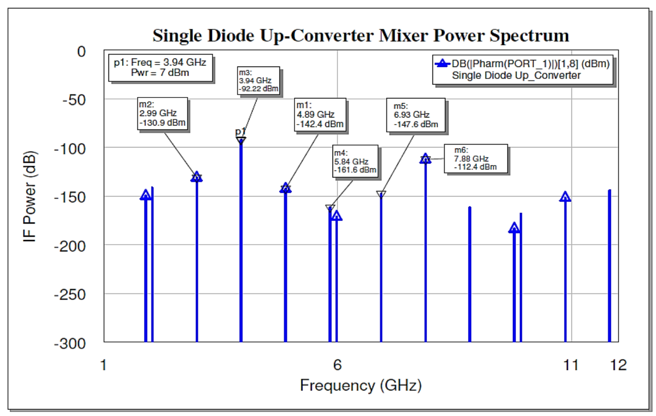

Fig. 13 IF power spectrum of SDIODE Up-Converter Mixer in Fig. 11 using the frequency domain Power measurement feature, Pharm [16] at port 1

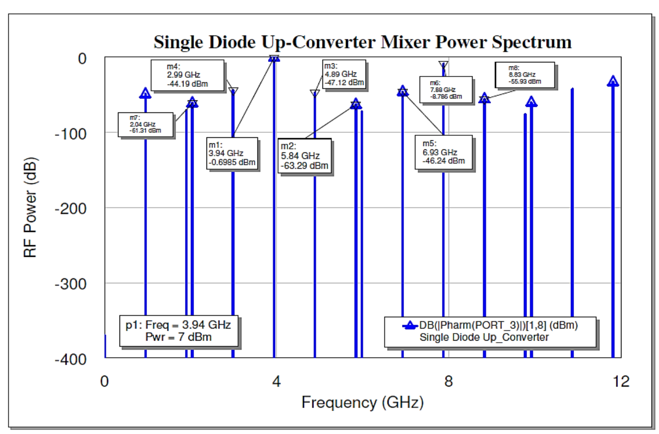

Fig. 14 Spectral components of RF power in SDIODE Up-Converter Mixer of Fig. 11 using the frequency domain Power measurement feature, Pharm [16] at port 3

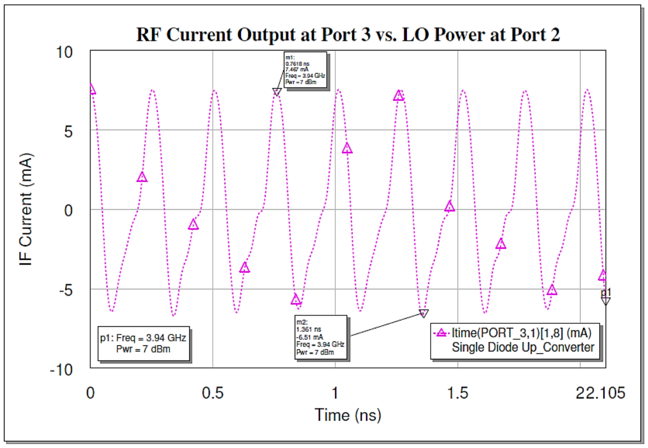

Fig. 15 Asymmetrical RF Currents waveform in SDIODE Up-Converter Mixer of Fig. 11 using the nonlinear current measurement feature, Itime [16]

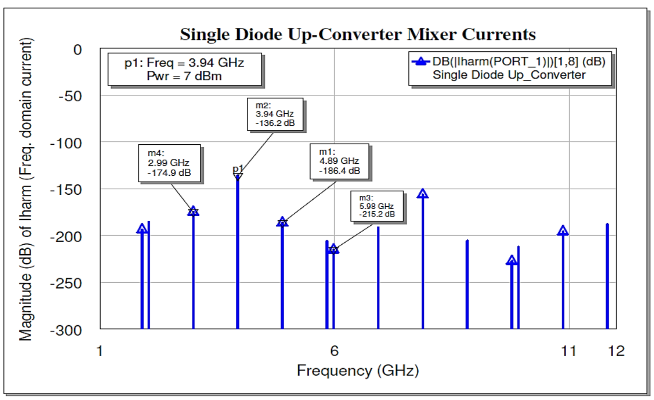

Fig. 16 Rectangular plot of the Current nonlinear spectrum through SDIODE Up-Converter Mixer at port 1(P=1) with 7 dBm power at port 2 (P=2), LO sweep frequency of 3.94 GHz, and using AWR Harmonic Balance simulations on Fig. 11

3.2. AWR Schematic of Double diodes based Balanced Mixer design

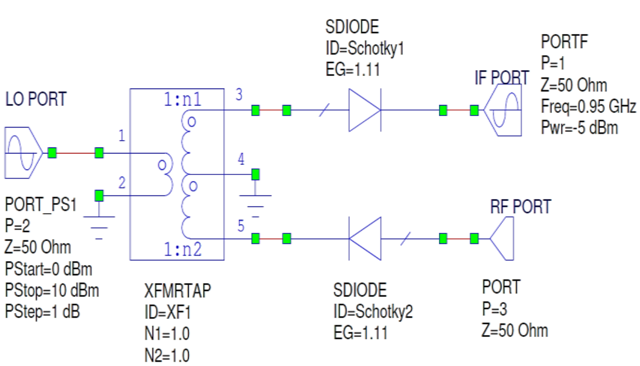

Fig. 17 AWR circuit diagram of BDM as an Up-Converter Mixer using a simple 1:1 turns ratio center-tapped transformer "XFMRTAP" [1], [16], [23]

A balanced Diode Mixer (BDM) was formed by placing double diodes in the anti-parallel arrangement, as in Fig. 17, to eliminate the extra Diplexer circuitry (causing generation of unwanted harmonics) needed for passive Single diode configuration. A BDM achieved Conversion Gain improvement. The RF and LO inputs levels for design and simulations were given according to the specifications listed in Table 1. The difference between the RF input power and desired output IF power is the Conversion loss, which varies along with the input RF power level. RF power level was kept 10dB away from the LO power level in typical RF circuit designs [22].

Table 1. Frequency and Power

Parameter	Design Value
RF (GHz)	4.89
LO (GHz)	3.94
IF (GHz)	0.95 (RF-LO); 8.83 (RF+LO)
LO power (dBm)	Greater than 0 dB
RF power (dBm)	Less than -10dB
Conversion Loss (dB)	(P_{RF} - P_{IF})

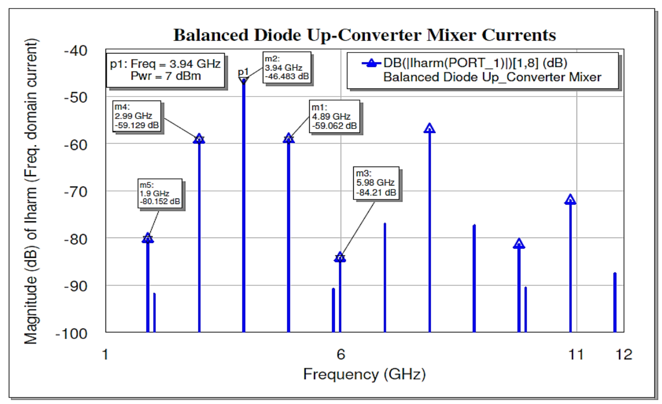

Fig. 18 Spectrum of nonlinear Current at RF port with excitation of 7 dBm (5 mW) at LO port. Markers depict dB magnitudes of Iharm [16] around 5 GHz frequency

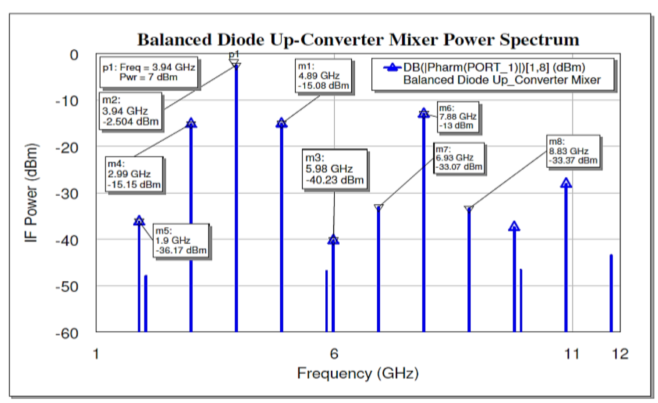

Fig. 19 AWR IF power spectrum of BDM Up-Converter in Fig. 17 using the frequency domain Power measurement feature, Pharm [16] at port 1

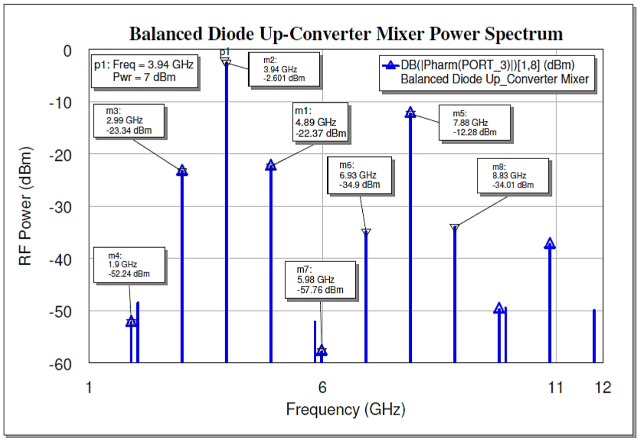

Fig. 20 Spectral components of RF power in BDM Up-Converter of Fig. 17 using the frequency domain Power measurement feature, Pharm [16] at port 3

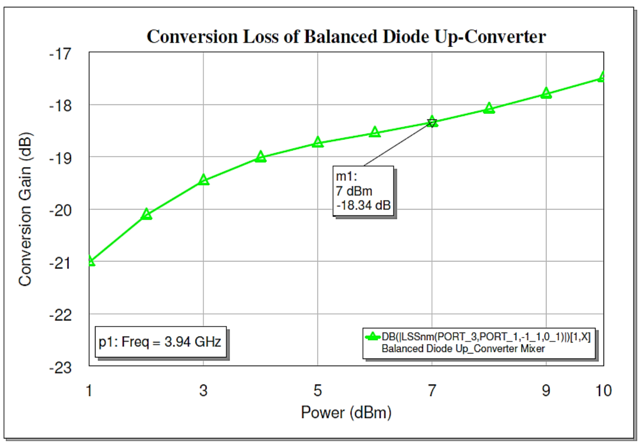

Fig. 21 Conversion losses (port 1 to port 3) in dB as a function of LO power levels for the BDM Up-Converter in Fig. 17. Increasing LO power drive at port 2 results in Conversion loss decrease; however, high LO source power increases the Mixer power consumption

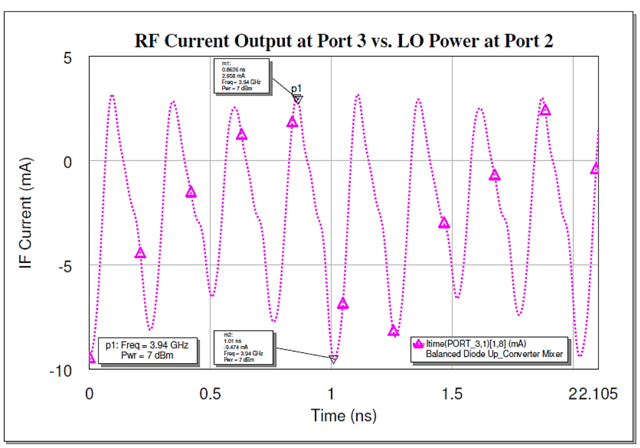

Fig. 22 Asymmetrical RF Currents waveform in BDM Up-Converter of Fig. 17 using the nonlinear current measurement feature, Itime [16]

3.3. AWR Schematic of Quad diodes Double-Balanced Mixer design

The Double-Balanced Diode Mixer (DBDM) was formed by placing 4 diodes in the Bridge topology design to eliminate the generation of unwanted harmonics in BDM configuration along with two transformers providing port isolations as shown in Fig. 23. For mixing using non-linearity where multiplication is done using nonlinear transfer function, while DBDM being operated in the non-saturation mode for SDIODE's [1]. As the Local Oscillator (LO) creates oscillating ± polarity RF signals, mixing operation at LO frequency is similar to the multiplication of RF signal by a Square wave (Pulse) from ± 1 V and applying Taylor series expansion for Square wave function [23]. For the same amount of power levels at an LO port of 7 dBm(5 mW), the improvement in Conversion Gain achieved by DBDM is at least three folds lower (in dB scale) compared to that of a BDM Up-Converter Mixer, as evident from the comparison of Fig. 28 and Fig. 21 respectively.

The Double-Balanced Diode Mixer setup was reasonably candid, wherein numerous diodes were arranged to build the necessary drive level. The LO signal turns ON the initial arm consisting of two diodes. Afterwards, the second arm comprising the other two diodes inside the diode ring of Fig. 23 is actuated sequentially. The high-performance design utilizes circuit symmetry to create a balanced design that offers isolation between the ports and causes the suppression of intermodulation products. For DBDM, LO power levels can be acquired through an assortment of drive levels with 3 dB order increments, such as +3, +7, +10, +13, and +17dBm with a widely acknowledged power level of +7dBm [22].

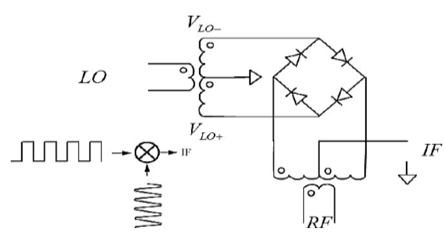

Fig. 23 Block diagram of a 3-port DBDM using four Schottky diodes in Bridge topology and two single-ended differential center-tapped transformers [23]-[24]

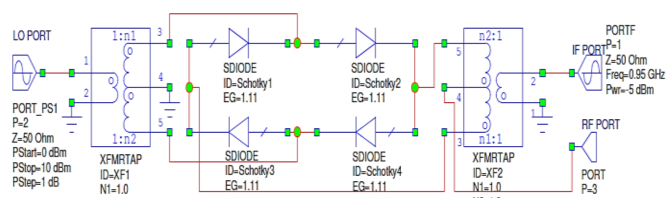

Fig. 24 AWR circuit diagram of DBDM in Fig. 23, as an Up-Converter by 2 single-ended differential 1:1 turns ratio center-tapped transformers "XFMRTAP" [1], [16], [23]

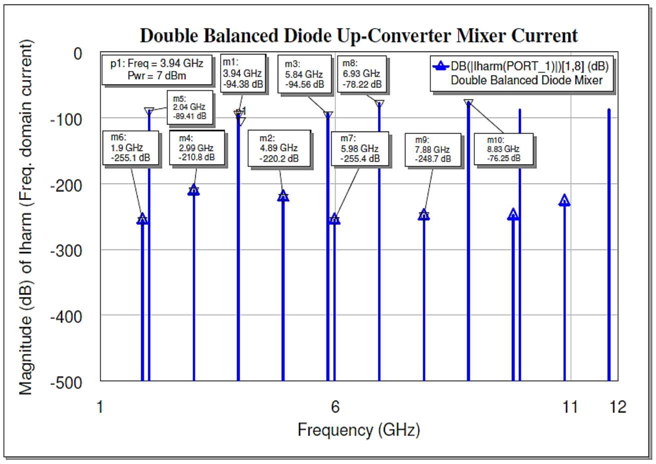

Fig. 25 Spectrum of nonlinear Current at RF port with excitation of 7 dBm (5 mW) at LO port. Markers depict dB magnitudes of Iharm [16] around 5 GHz frequency

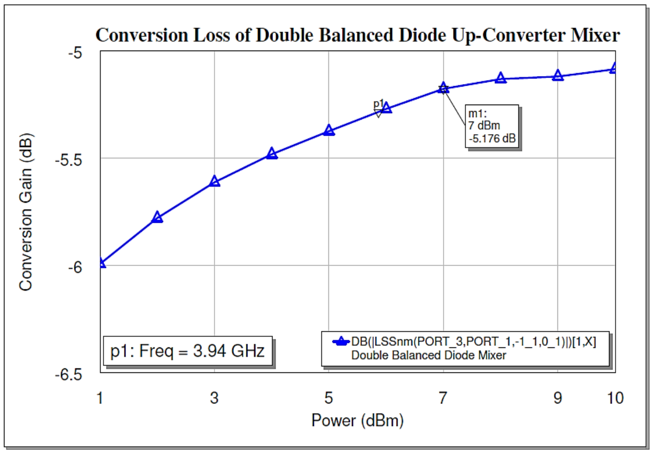

Fig. 28 Conversion losses (port 1 to port 3) in dB as a function of LO power levels for the DBDM Up-Converter in Fig. 24. Increasing LO power drive at port 2 results in a Conversion loss decrease. However, high LO source power increases the Mixer power consumption

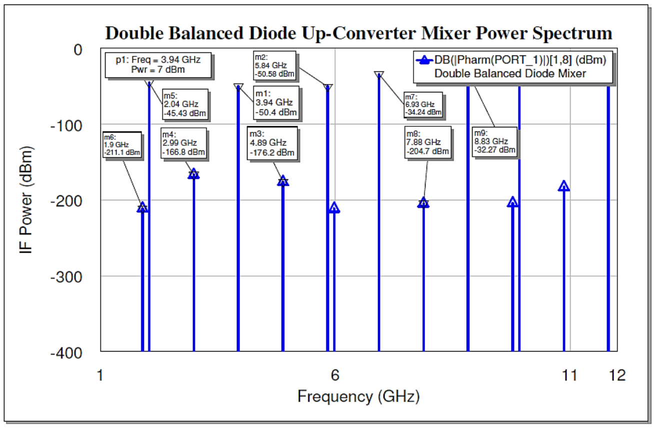

Fig. 26 AWR IF power spectrum of DBDM Up-Converter in Fig. 24 using the frequency domain Power measurement feature, Pharm [16] at port 1

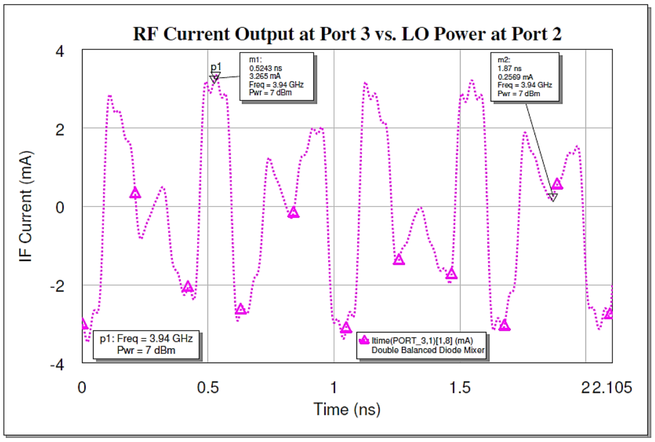

Fig. 29 Asymmetrical RF Currents waveform in DBDM Up-Converter of Fig. 24 using the nonlinear current measurement feature, Itime [16]

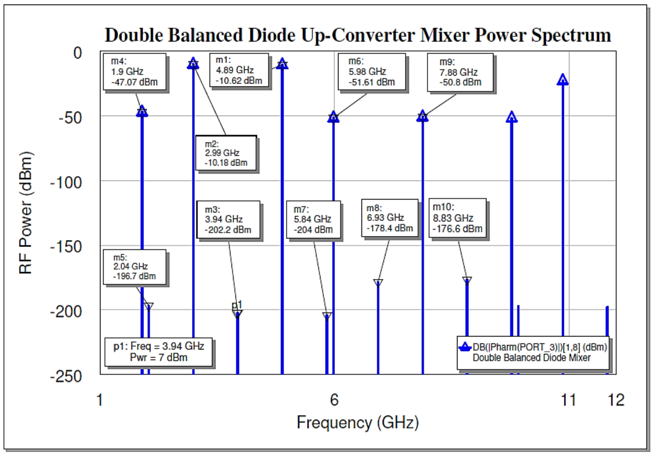

Fig. 27 Spectral components of RF power in DBDM Up-Converter of Fig. 24 using the frequency domain Power measurement feature, Pharm [16] at port 3

4. Microwave-Balanced and Double-Balanced Diode Mixers

Design and fabrication of center-tapped transformers "XFMRTAP" [16] at the 5 GHz range becomes challenging because the center frequency f_0 tends to fluctuate due to dispersion effects. Also, at HF, the diode Capacitance 'C' makes the Mixer configuration less efficient due to the dependence of C on the Impedance [1]. This ultimately leads to larger losses in Conversion Gain and Conductor skin depth, causing abrupt Impedance variations with f_0 and thus introducing network mismatching on the transmitter side of integrated transceiver systems. Tapped transformers-based Mixer designs hold good up to 12 GHz frequency range [1]. In order to utilize the ease of MMIC fabrication of Backend designs with Microstrip technology, Microwave models based on transmission line designs offer viable options for 5G Next Generation Mixers. Center tapped transformers in the Double-Balanced Mixer design of Fig. 24 are replaced with transmission lines, which at microwave frequencies generate outputs that are 180° phase shifted at a single frequency [1]. Mixer performance is not altered by this transformation since the RF and LO signals are still within 10 % of each other, which is needed to obtain perfect Isolations.

4.1. AWR Schematics of Microwave Balanced Diode Mixer (BDM) and Double-Balanced Diode Mixer (DBDM) with Simulation results

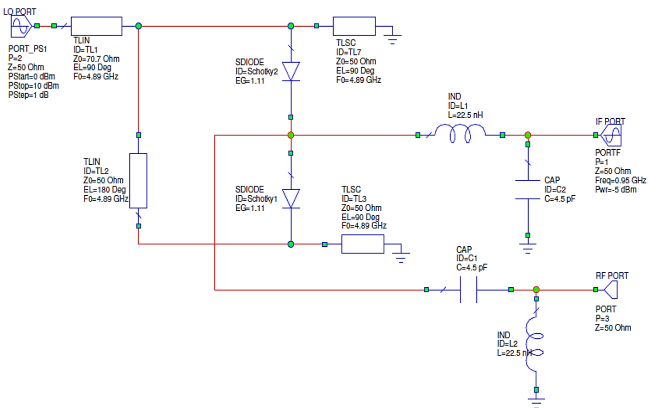

Fig. 30 AWR circuit diagram analogous to BDM in Fig. 17, of the Microwave BDM as an Up-Converter Mixer using Transmission Lines (TLIN) and Transmission Shorted Line Circuit (TSLC) elements [1], [16], [23]

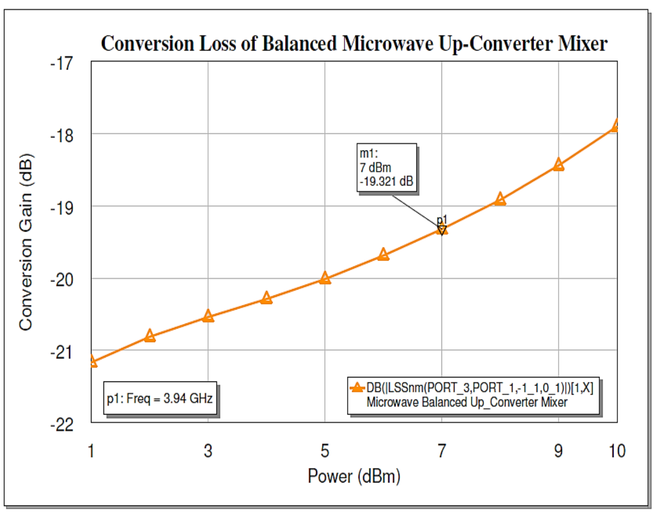

Fig. 31 Conversion losses (port 1 to port 3) in dB as a function of LO power levels for the Microwave BDM Up-Converter in Fig. 30. Marker m1 depicts dB value in the range, comparable to the value of standard BDM in Fig. 21 for the same power level of 7 dBm

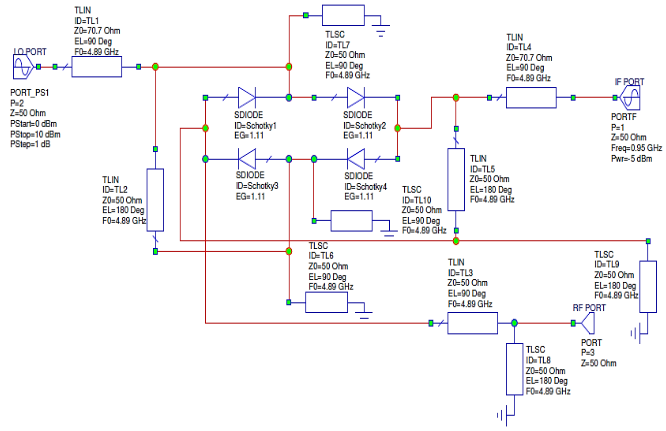

Fig. 32 AWR circuit diagram analogous to DBDM in Fig. 24, of Microwave DBDM as an Up-Converter Mixer using SDIODES, Transmission Lines (TLIN) and Transmission Shorted Line Circuit (TSLC) elements [1], [16], [23]

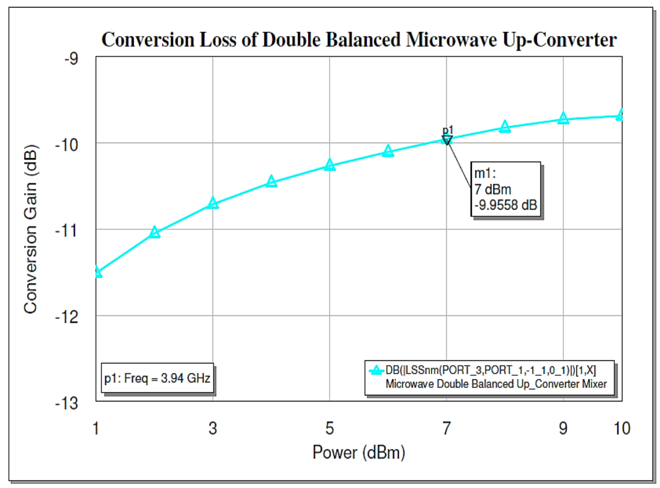

Fig. 33 Conversion losses (port 1 to port 3) in dB as a function of LO power levels for Microwave DBDM Up-Converter in Fig. 32. Increasing LO power drive at port 2 results in Conversion loss decrease, however high LO source power increases Mixer power consumption

4.2. Layout of DBDM

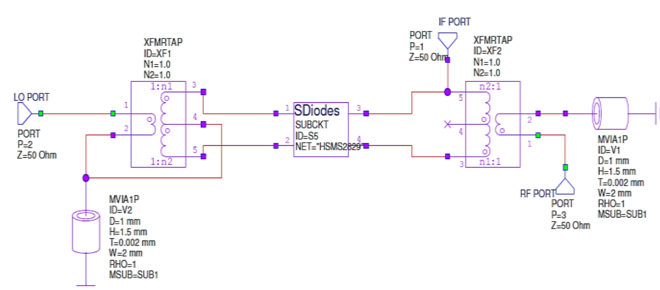

Fig. 34 AWR schematic for layout generation of DBDM in Fig. 24, as an Up-Converter Mixer using 1 port cylindrical Microstrip VIA and sub-circuit of SDIODES "HSMS2829" [1], [16]-[17], [23]

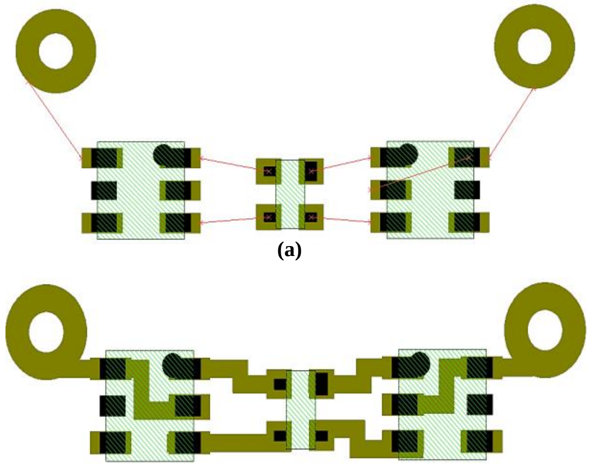

Fig. 35 AWR Layout views of DBDM in Fig. 34 with Microstrip pads (closed form) (a). Logical Orientation with red lines indicating schematic connections and vias represented by round circles (b). Signal routing layers across Diode Bridge, drawn by Cu top lines [1], [16], [23]

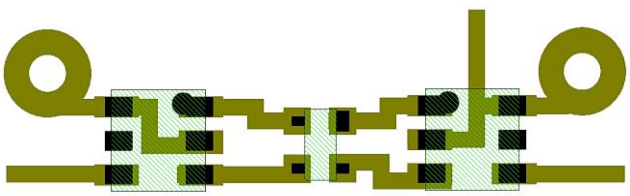

Fig. 36 AWR layout view of DBDM in Fig. 34, with the addition of three ports along with trace visibility by the free hand-drawn layers of routing signals using square cooper top line, bends with a path width of 0.6 mm, having 0.5 mm offset [1], [16], [23]

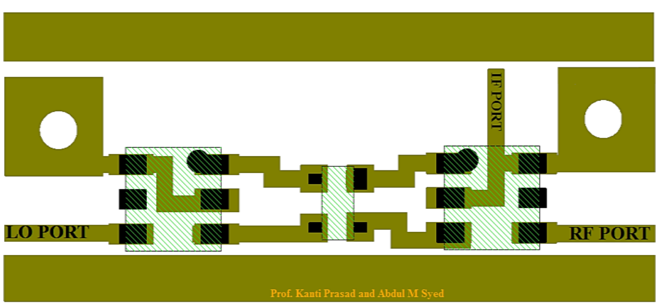

Fig. 37 Final AWR layout diagram of DBDM as an Up-converter Mixer in Fig. 34 with IF, LO and RF ports and via holes drilled inside the square Microstrip pads. Mixer layout is ready for mask preparation and attaching SMA connector accessory for testing on a Network Analyzer, subsequent to the post-fabrication process using an external PCB metal housing or through cleanroom etching method [1], [16], [23]

5. Conclusion and Future Work

Different avenues were looked at to realize the best possible solutions for devising a well-suited Mixer topology for an integrated 5G MMIC Transceiver chipset. Based on a review of the Current State-of-the-Art and literature search, there is a potential for a high-end RF Power Amplifier (PA) to fulfil the described necessities of Next Generation (G) Wireless technologies, including 6G Communications. Detailed simulations presented for an RF input power of 1 mw (0 dBm) establish a baseline: the transmitter output power of 0.2 W (23 dBm). The RF output power of TX plays a dynamic role in the functioning of Microstrip Patch Antennas and SPDT switch in terms of matching networks design and effective MMIC integration with the RFFE RX section along with the fulfillment of the maximum power handling capacity of 6.25 W of GaAs substrate. Based on the Baseband excitation of 10 mW (10 dBm), the IF processing stage should be further developed using Verilog-VHDL coding for RF ADC-DAC and Modulator-de-Modulator pairs. It should then strongly articulate the 5G standards in the Power Budget Analysis of consummate RF Transceiver Link encompassing the Front-End and Backend systems. They also fulfill prerequisites of shared Antenna and Bandwidth in the Internet of Things (IOT) applications in next G Wireless Communications systems and explicitly the 5G "New Radio" concepts.

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