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Original Article

Study of Hot Carrier Degradation in N-Channel LDMOS Transistor under Thermal Stress

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Abstract *- Thermal constraints, special in high-temperature levels, are the majority detected degradation phenomenon in Radio Frequency power devices. To assess the shift level, the focal sign results from the on-state resistor (RDSON) methodically related to the internal device structure evolution. This evaluates thermal constraints properties on current-voltage behaviors of power RF N-LDMOS components, particularly of the $R_{DSON.}$ The resistor parameter, a principal restriction of the N-channel LDMOS components in the greatest temperature procedures, can partly or entirely modify the reliability of the physical and electrical components. R_{DS-on} is highly dependent on temperature. The measurement characteristics significant to the thermal evaluation behavior of the component are described and confirmed through the elementary physical performance. The experimental results investigation is presented and used to study the physical aspect of temperature effects on N-channel LDMOS reliability. Physical quantities such as current lines, concentration, and mobility are considered depending on the temperature reliance. To finish, the study of the initial effects is presented and discussed.*

Keywords *- Reliability, Characterization, LDMOS, Temperature effects, Hot carrier phenomenon.*

1. Introduction

MOSFETs components are the best generally used devices in the height RF power field. The charge of MOSFETs signifies a substantial benefit over III-V advanced structure for system degrees max to everywhere 4 GHz. The semi-conductor behavior is sensitive to thermal effects, mainly the RF power devices [1-3]. Thermal phenomenon are again the main origin of degradation in maximum situations. The temperature affects significant evaluations in characteristic behavior and vastly impacts performance, directing partial failure or entire. It confines the lifespan and acting a vital part in numerous failure processes of semi-conductors.

Approaching the usually aging and under control silicon industry area, it is an edition of elementary MOSFET advanced for radio frequency power systems. In addition to its little engineering charge, the MOSFET device has the electrical and thermal behaviors requisite for difficult modulations due to its frequency, thermal permanency, and respectable linearity. The exceptional linearity of the LDMOS transistor places it the greatest candidate to come across some severe terms of mobile phone ideals. This technology pointedly reduces power depletion and thermal problems in base stations, thus increasing power density by 50%, efficiency by 6-8%, and power gain by 2 dB compared to other technologies [4]. In a MOS transistor, when the current line is drilled per the drain electrode, and the power dissipated is captivated at the channel region and the warm at the channel structure. The current increase is due to high dependence and irregular temperature inside the transistor [5,6]. Important studies are made to increase the breakdown voltage and decrease the ON resistance, with proof and physical explanation [7,8], making it a suitable candidate for high-voltage and power-integrated circuit (IC) applications. In on state (linear region), the MOSFET can be considered a resistor, and the R_{DS-on} is the resistance between drain and source when this one is in on state. This resistor is some of the vital behavior of RF MOSFETs transistors; the important defiance in progress is to decrease this resistor to bounds the self-heating phenomenon, and the voltage dropped in the on state [1,3,6].

This work is offered in the resulting method: the measurement parameters of N-channel LDMOSFET are comprehensive in part two. The outcomes argument is detailed in part three. The conclusion is mentioned in part four.

2. Experimental Characterization of Power N-LDMOSFET

The experimental measurement must be as accurate as probable and is the property of environmental constrictions, like humidity, temperature, etc. To ensure this experimental

measurement technique, we used for method instruments the IC-CAP software border (Integrated Circuit… Characterization…Analysis... Program). This task designates the principal characteristics of the current voltage of the RF power MOSFET component. This characterization method aims to estimate the component performance and analyze their behavior in the different operational modes, especially in linearity and saturation region. However, to find some parameters essential, such as the I_{DS} current, the V_{th} voltage, the transconductance, the R_{DSON} resistor, etc. That will be amongst the main criteria for the degradation study. All measurements in this sector are implemented on the component of RF power equipment of N-channel type. The investigational measurement stage comprises an analyzer Agilent E5270 Direct Current, with 20 Watts presenting the maximum power output, determined with IC-CAP equipment and a Peltier element controlled in temperature value, from 0 °C to 200 °C, organized through a BILT chassis, totally connected via GPIB bus to a regulator PC (Fig. 1). When the component is in the characterization phase, it's positioned on a thermal Peltier unit through interaction by fixative per an interstitial liquid; it's conductive of silicone grease to keep a continuous thermal level. The block unit conduit Direct Current provides temperature level directives and power.

The greatest electrical characteristic is the Ohmic area, where the IDS drain-source current sincerely increases relies on the V_{ds} drain-source voltage. The R_{DSON} resistor of the power MOSFET component is definite by way of the entire resistor, flanked by the source electrode and drain electrode. The component functions in a linear model (Fig. 2(a)) with less V_{DS} drain-source voltage mode. Therefore this equivalent voltage inclines to zero. The value is calculated by the ratio:

$$R_{DS-on} = (V_{ds}/I_{ds})_{Vds \to 0} \quad (1)$$

The channel foundational determines the RDS-on resistor level; it is mostly an experimental measurement for V_G gate voltages like the channel is completely open; therefore, one is at the saturation level. Fig. 2(b) shows R_{DS-on} decreases vs gate potential rises. The resistor is too much higher at the Vgs level under the Vth voltage, evading a transient current under the threshold V_{th}; the transistor is completely obstructed.

3. Outcomes Analysis and Discussion

Failures produced through thermal phenomena are not the individual reasons for the component behavior's degradation. In contrast, thermal aspects are the major reason for defects in most tests. The analysis objective is the R_{DSON} estimation of RF N-channel MOSFETs components per thermal and physic effect. R_{DSON} is the entire resistor that looks concerning drain and source block for the component are at direct mode (less V_{DS} voltage). It is principally the totality of two parts: the drift area resistor R_{Drift} and the inversion Channel Resistance R_{ch} (see Fig.3).

$$R_{DS-on} = R_{ch} + R_{Drift} \quad (2)$$

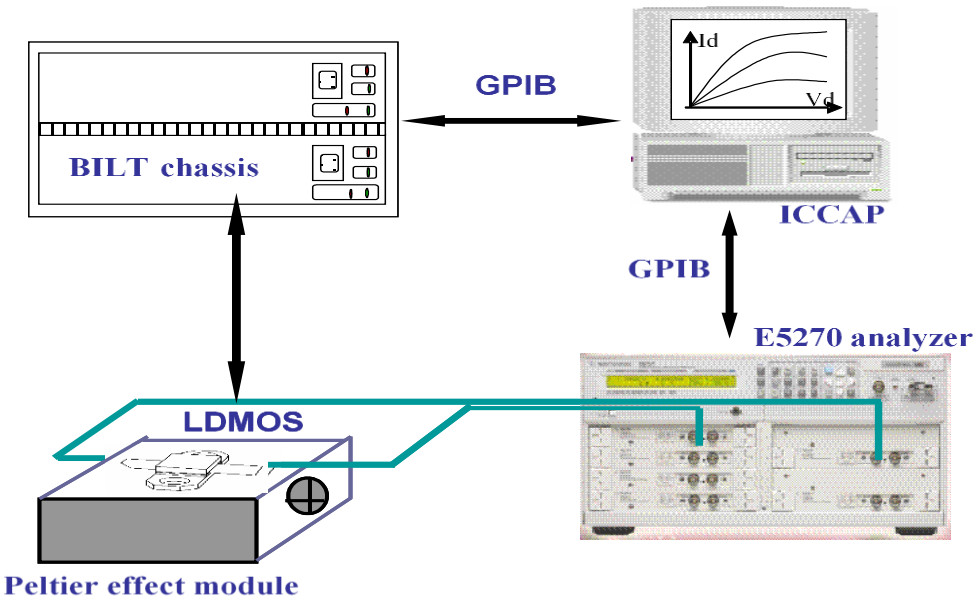
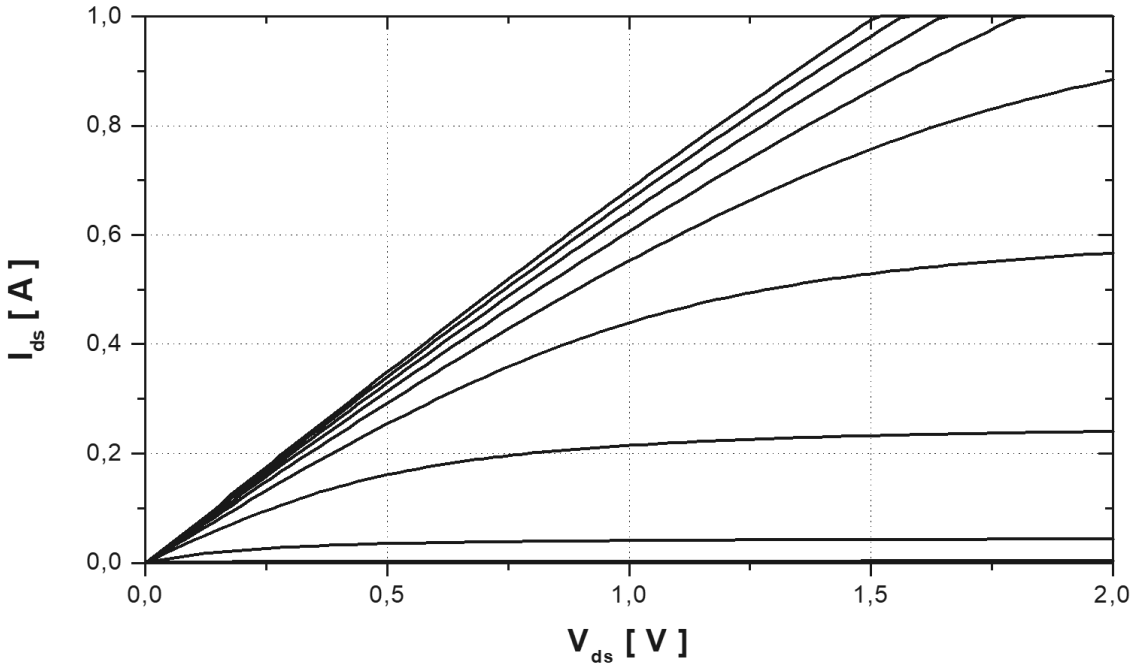
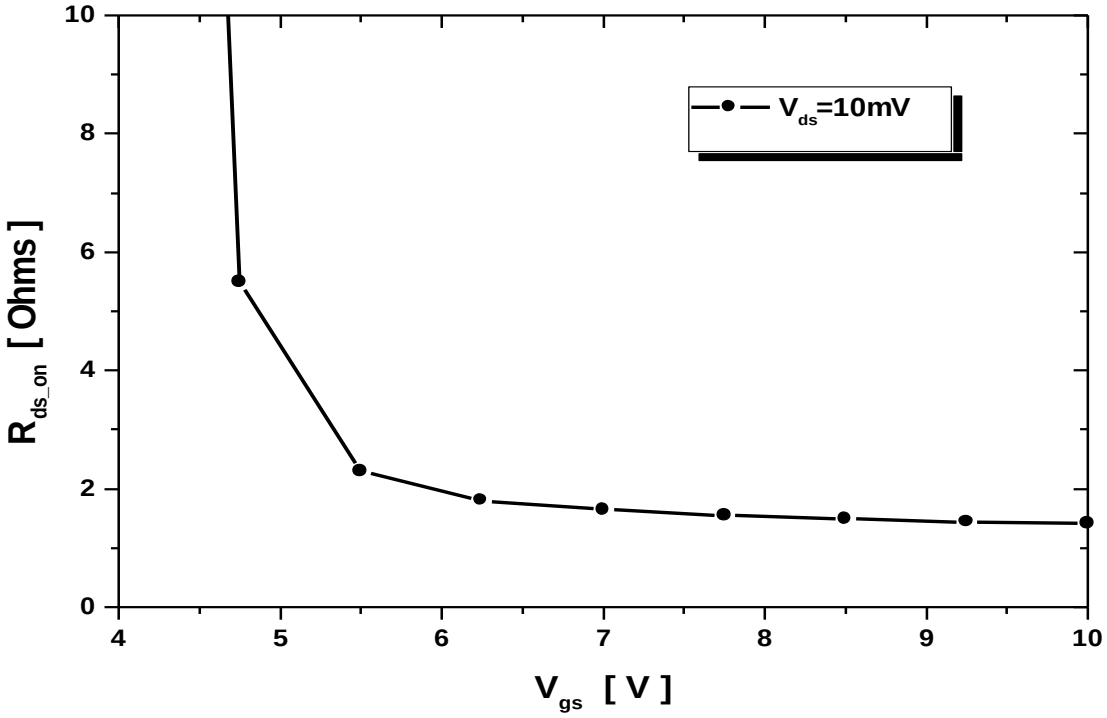


Fig. 1 Bench of the measurement of the I-V parameters



(a)



(b)

Fig. 2 The experimental $R_{DS\text{-}on}$ resistance: (a) Slope from the I_{ds} vs V_{ds} in Ohmic part, V_{gs} [3;10V], step=1V, (b) Experimental variations vs V_{gs} voltage

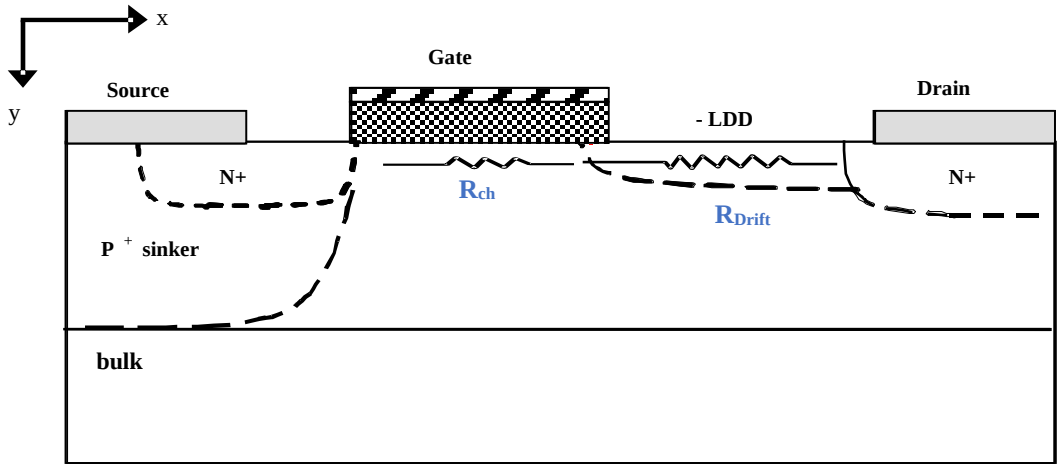


Fig. 3 Cross-section observation of RF LDMOSFET through various components of R_{DS-on} resistance

The resistor (R_{ch}) of the inversion channel is governed by the structural material, the temperature, and the V_{GS} voltage, which is adjusted by the resulting [9]:

$$R_{ch} = \frac{L}{W\mu_{EFF}(T)C_{OX}(V_{gs}-V_{th}(T))} \quad (3)$$

The R_{Drift} presents the resistor of the N-nature faintly doped area. The meaning of drain bias: at V_{DS} polarization rises, the resistor of the channel is determined by the V_{GS} voltage, whereas the VDS voltage determines the RDrift resistor. These dependency outcomes control the carrier's rapidity in the drift area because of the peak electric field and the area being smaller. If this field parameter is greater, the mobility phenomena of the carrier are lesser, which losses the resistive zone performance; consequently, the resistor value is more important to supplementary resistive devices. The typical equation improvement of the potential orderly resistor is fined through lettering the current one-dimensional calculated at the drift area [9]:

$$I_{ds} = q.\mu.n.S.\frac{dV}{dy} \quad (4)$$

With q presents the charge of electron elementary, μ shows the mobility of electrons at drift area, S presents the measured unit, n mince the density of electrons, V presents the voltage potential, and dy is a basic percentage in the configuration in longitudinal mode. As a result of integration, the current form above the drift zone dimension and difference of potential at its blocks, to infer the expression dorm resulting in the drift resistor [9]:

$$R_{Drift} = R_{d0} + K(V_{ds} - V_1) \quad (5)$$

Where V_{ds}-V_1 is the difference of potential transversely to the drift area and K is a constant parameter. The part R_{d0} principally Be determined by the length of drift area, doping resistor, which is a direct linear equation of V_{DS} potential. The current Ohmic is located at the linear mode of output experimental measurement I_{ds} vs V_{ds}, as shown In Fig.2-a. This zone is defined via the relation equation under, with a drain polarization is functional in as a method that $V_{ds}<V_{ds-sat}$, then:

$$I_{ds} \approx \frac{W}{L}\mu_{EFF}C_{OX}[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}] \quad (6)$$

With μ_{EFF} the .carrier's mobility .of the .conduction channel [9]:

$$\mu_{EFF} = \frac{\mu_0}{\left[1+\frac{|E_X|}{E_C}\right]\left[1+\frac{|E_Y|}{E_0}\right]} \quad (7)$$

W is the width of these equations, and L is the conduction channel length. C_{OX} presents the oxide capacity of the gate, μ_0 is the low-slung mobility of the field electron, E_Y and E_X signify the longitudinal and transverse devices for the electric field, and E_C and E_0 present the transverse and the longitudinal grave field level, respectively, afar that the saturation of electron velocity is detected. Equation (7).can also be written as [10]: which highlights the temperature dependence of the conduction channel mobility:

$$\mu_{EFF}(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \quad (8)$$

For the LDMOS device, m = 2.5 leads to a temperature dependence of electron mobility in the conduction channel of the $T^{-2.5}$ form. The LDMOS experiences a greater reduction in carrier mobility at a higher temperature than CMOS. In comparison, CMOS mobility follows a $T^{-1.5}$ type law [9]. Fig.4 shows that the I_{ds} at low current levels vary linearly with temperature. It is due to the reduction of the threshold voltage.

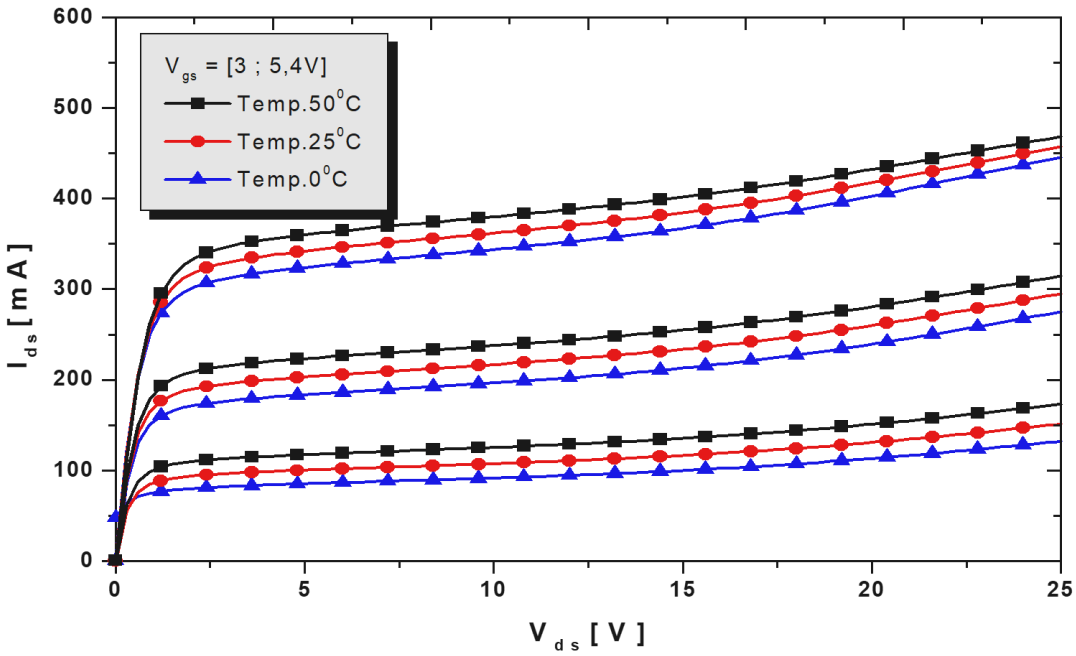


Fig. 4 Variation of channel current with different temperatures

The threshold voltage V_{th} relates to the V_{GS} voltage level. Beyond that, the MOSFET transistor starts to lead (inversion channel creation permitting the current flow from drain to source). The area where the acceptance of concentration impurity is the maximum enforces the threshold voltage Vth, which relates to the extreme doping value N_{max}. In the MOSFET transistor case, the concentration peak is at the conduction channel. It is assumed through [9]:

$$V_{th}(T) = \emptyset_{ms} + 2\emptyset_f + \frac{\sqrt{2\varepsilon q N_{max}(x)(2\emptyset_f)}}{C_{ox}} - \frac{Q_{ox}}{Q_{ox}} \quad (9)$$

The temperature addiction of the expression (9) approaches principally by the Fermi potential, which is transcribed by

$$\emptyset_f = \frac{KT}{q} \ln\left(\frac{N(x)}{n_i(T)}\right) \quad (10)$$

The V_{th} is an electrical parameter depending on the temperature. In these relations, ϕ_f is the Fermi potential, ϕ_{ms} is the difference of output work between the metal and the semi-conductor, ε is the silicon dielectric constant, kT/q is the thermodynamic unit, and n_i is the intrinsic concentration.

Which is strongly related to temperature effects; therefore is written through [9-11]:

$$n_i(T) = 3.87x10^{16} T^{3/2} e^{-E_g/2kT} \quad (11)$$

The energy gap variation through the temperature is low, not considering the error introduced with E_g, which is autonomous of the temperature effect [10]. The evolution of the MOSFET threshold voltage V_{th} vs temperature evolution is encountered with grouping (9)-(11) and differentiate that gives:

$$\frac{dV_{th}}{dT} = \left[\frac{\emptyset_f}{T} - \frac{K}{q}\left(\frac{E_g}{2KT} + \frac{3}{2}\right)\right]\left(2 + \frac{\sqrt{2\varepsilon q N_{max} 2\emptyset_f}}{2\emptyset_f C_{ox}}\right) \quad (12)$$

The V_{th} is a physical and technological characteristic of MOSFET displays which diminutions per thermal effects (Figure 5). Therefore, the evolutions are direct linear vs the thermal phenomenon, therefore be able to present under with [9]:

$$V_{th}(T) = V_{T0} + (V_{tT} T_j) \quad (13)$$

With T_0 presenting the temperature in ambient mode, V_{T0} means the threshold potential at T_0, V_{tT} is the function factor, and T_j shows the temperature level of the junction. Figure 6 shows the threshold potential V_{th} measured for classic N-channel MOSFET components completed from 20 °C to 150 °C. The V_{th} development is linear; however, reductions in the temperature rise (Figure 6).

The $R_{DS\text{-}on}$ is definite at the linear zone of the drain current (Eq.1) when it is contrariwise relative; the on-state resistor in the reductions if the V_{GS} potential rises, displayed in Figure 7-a, presents the on-state resistor measured of the MOSFET geometric at Figure 3. At great

V_g is equivalent to high reverse; therefore, mobility phenomenon properties are mostly, so (Eq.2) - (Eq.3) envisage a rise in the on-state resistor via temperature (Figure 7-b). The setting R_{DS-on} relies on the distribution and heat dispersal, which signifies the heat flow inside the device [5-12]. The numerical simulations were performed for RF power MOSFET geometry to analyze the thermal behavior, therefore, their properties. With numerical simulation and the shifts, the study of the characteristic quantity progresses, in terms of the practical temperature, to explain the relationship between the electrical parameter shifts and the main physical mechanism.

Enough maximum of the electric field is located in the area charging region reasons of the electron pairs holes through the collision enter the crystal lattice and the carriers [12]. It leads to doubling the carrier quantity; consequently, high currents are produced. The process at a risky level of potential and power, a thermoelectric response phenomenon, can make the current tighter at determining the hot spots [12,13]. This phenomenon changes the reliability or destroys the device. While this mechanism is identified for MOSFETs transistors, its reflection for N-channel LDMOS has become necessary because of the latter practice in the power RF systems. A drift section is needed to detect residents 'hot spots to know the thermal aspect dispersal in the structure.

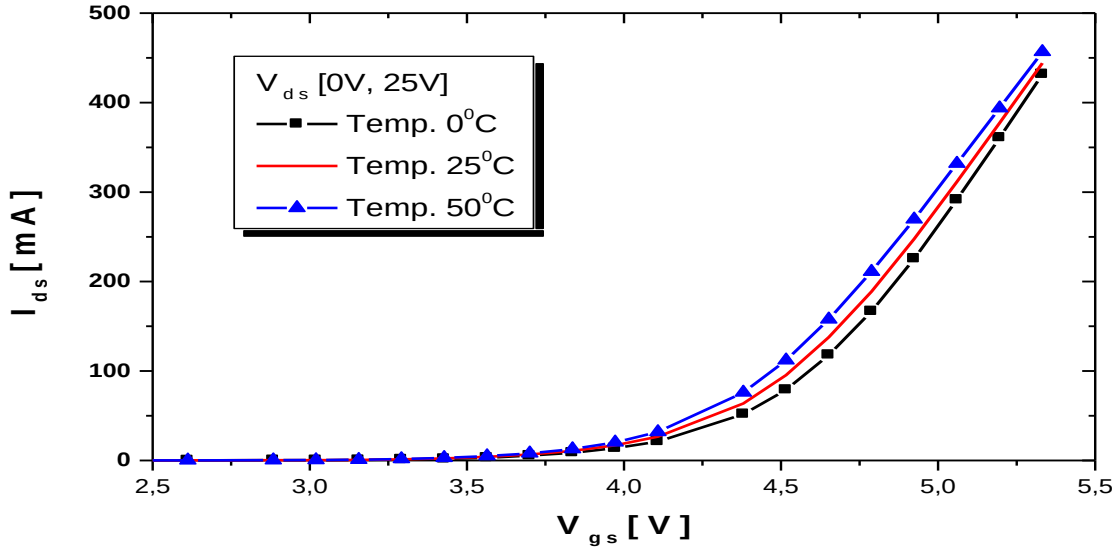


Fig. 5 Temperature effect on the V_{th} voltage

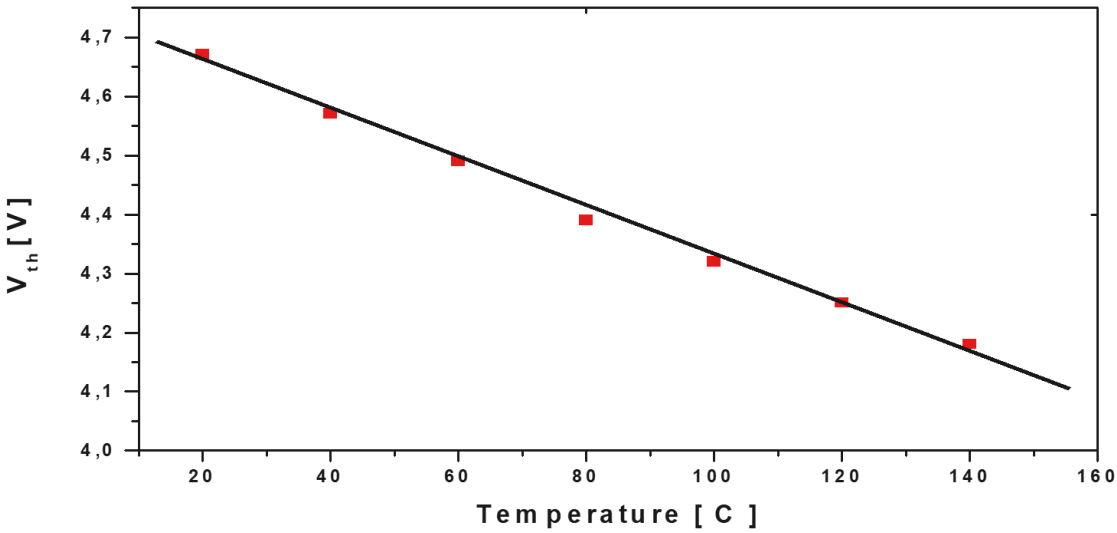
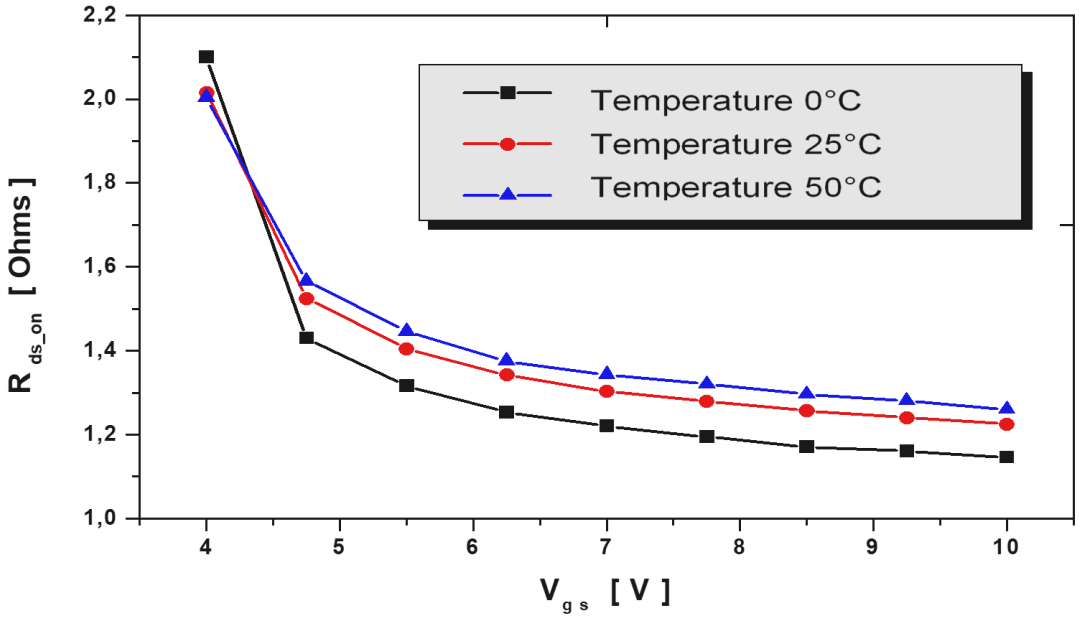
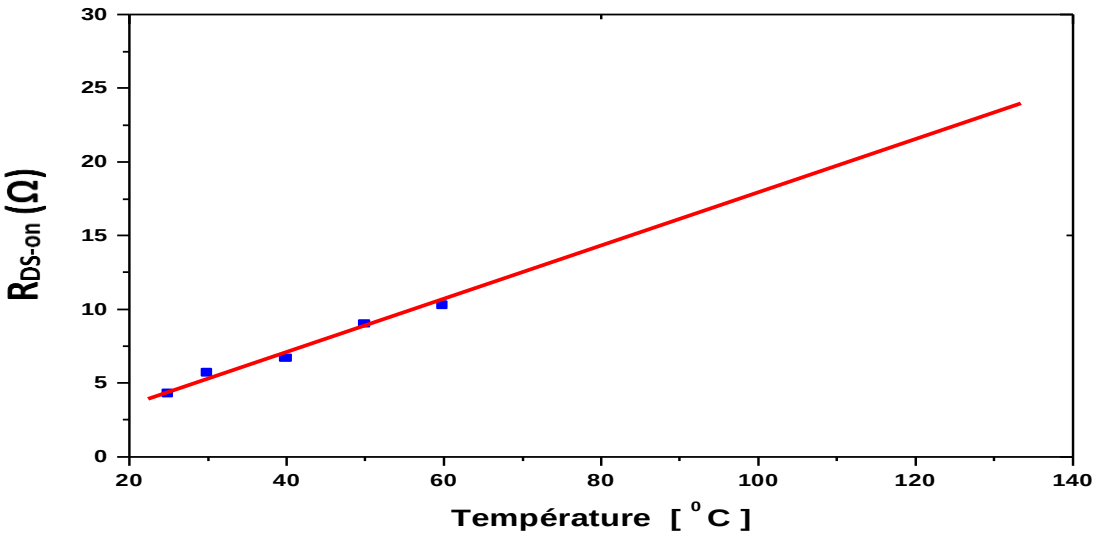


Fig. 6 Evolution of V_{th} threshold voltage through temperature level



(a)



(b)

Fig. 7 R_{DSON} resistor evolution of RF N-channel LDMOS: (a) according to V_{gs} potential at diverse temperature values, (b) in terms of temperature

The dissipation power in the drift area was located in a manner of non-uniform distribution [5,11] because the breakdown voltage effect can carry out the thermal defects [2-3-9] if the channel temperature rises superior enough. The temperature level increase caused by the self-heating proceeds inside the power LDMOS dynamic zone, shifting the device's electrical behaviors. In the end, modifying the reliability to a significant amount [13]. The current-voltage characteristics caused by physical behavior change, touching the RDSon principally.

The IDS drain current value increases the temperature rate caused by the reduction of threshold V_{th} voltage in the less current area, decreasing because of the effective mobility deterioration in the high current area [2]. The characteristics evolve over the electric field level, increasing the carrier injection phenomenon ingrown the silicon dioxide layer (SiO2) in the interface state Si/SiO_2 [13-15]. The current flow lines are located most of the percentage through and under the $Si\text{-}SiO_2$ interface. We can observe that the concentration is very high, located near the gate side, at the drain cross, providing a manner for a major rise at the gate edge of the surface current density [14,15].

The manifestation of a strong electric field below gate oxide via maximum at zone LDD [1,3,5], great electrons concentration in the SiO_2/LDD area [3-5] participated in the presence of hot carrier is created by the impact ionization [5,9]. Regarding test situations (bias, thermal, etc.) provided, all advantages are consistent with the degradation caused by the hot carriers. Employing the current lines, overcrowding is superior at low-slung temperature levels in the SiO_2/LDD interface area; many electrons are accelerated to great rates by this maximum electric field [5-11]. The cause of the detected degradation correlated with a max electric field that raises the carrier injection on the side of full-grown silicon dioxide level (SiO2) in the interface state Si/SiO_2 [1,5,10]. The impact ionization failure properties are strictly correlated to the current density. The largest quantity of allowed electrons is in the silicon oxide zone. The maximum electrons are quintessentially deep inside the drift area [5,10,16]. So results in the negative charge accumulation at the $Si\text{-}SiO_2$ interface [3,10,17].

Therefore, numerous electrons are speeded to maximum rates by this high electric field peak [1,5,16]. So, they become tall and energized and must be augmented away from their standard flow. The analysis of relevant electrical parameters (I_{ds}, V_{th}, G_m, $R_{DS\text{-}on}$) powerfully interconnected to a structural zone allowed us to detect the failure area and distinguish the prevailing degradation phenomenon designated in the interface SiO_2/N-LDD. Ultimately failure mechanism is by way of the hot carriers.

4. Conclusion

An Investigation of temperature dependence on the R_{DSON} parameter of RF power N-channel LDMOS devices has been studied. The outcomes acquired signified that R_{DSON} is delicate to rising temperatures, and the foundation of these shifts is correlated to the physical behavior mechanism. The V_{th} voltage was presented to diminution monotone through temperature. However, the current I_{ds} and the resistor R_{DSON} have augmented per temperature level. These outcomes display dependability via experimental and physical results and reflect that most applications' thermal properties are the main degradation reason. The N-channel LDMOS electron of the concentration dissemination and the mobility has presented a strong thermal necessity at the I_{DS} current, precisely at the drain side. To improve the performance, we can find the middle ground between the great of the current gain and the evolution frequency; however, the low-slung of the resistor in pass mode. Studying the Drift area construction is necessary since doping to engross a maximum electric field at the I_{DS} current. Still, like any component exploited in RF power systems, the devices have operational borders particularly correlated with a thermal pheromone that diverges extremely of component electrical behaviors. That reflection strategy has grown into essential RF power MOSFET components, especially to diminish the on-state resistor as less probable.

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