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Original Article

Reliability Evaluation of NLDMOS Transistor Based on Advanced Aging Test Including Hot Carrier Phenomenon

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Abstract - *This manuscript treats the relative performance analysis of the hot carrier persuaded electrical behavior failure in RF power NLDMOS components afterwards innovative procedures of accelerated aging tests under various conditions (electrical and thermal stress). The results show the performances shift for critical electrical parameters such as the Miller C_{rss} capacitance and the C_{gd} gate-drain capacitance under various aging tests. To understand the parameter shift that appears during aging, we used a new electro-thermal perfect model executed by Agilent's Advanced Design System (ADS) software as a reliability tool beneath form SDD, meaning Symbolic Defined Device, also with a physical numerical simulation (2D Silvaco-Atlas software) to prove qualitatively degradation phenomena, which are resulted through the generation of interface state also stuck electrons, then outcomes in a buildup at Si/SiO_2 border of negative charge.*

Keywords - *Reliability, Characterization, LDMOS, Thermal effects, Hot carrier phenomenon.*

1. Introduction

In microelectronic engineering, the power is dissipated, and the current tendency is to downscaling electronic components and increases power. It is acknowledged that the thermal effects touched through the power component underneath process tests extensively affect reliability components and performances [1,2], which modify and degrade transistor behavior. This element can border the lifecycle of components and impacts a critical portion of degradation phenomena [3,4]. Previously, the models of channel current founded in analytic equations have been described by Miller et al., which presents the Motorola model [3] and Angelov et al., which details the Chalmers model [5]. Therefore have presented advanced respectable results. It would benefit radars systems, the area domains, microprocessors and civic applications such as communications and the automotive industry. Temperature is a critical phenomenon, principally in power RF electronic components. For many causes, temperature shock aging tests and cycling situations are fetching significantly for the RF power MOSFET in numerous applications. The loading current can be unlimited.

Consequently, it's prominent to the grave danger of degradation [1,4]. The electric parameters of MOSFET components are ever more delicate to failings destined to the charges in the oxide of the gate electrode and the Si/SiO_2 interface [5,6]. The objective of this manuscript is a relative performance analysis of different aging test environments based on advanced test systems, including the hot carrier phenomenon. Finally, our work methodology characterises the experimental parameters and extraction from the device model before-after aging.

2. Conditions and Thermal Aging of Bench

The experimental aging test is considered to control; equally, the electrical and thermal aging of NLDMOS components are presently realized (Fig. 1). Three types of enhanced aging experiments (Thermal Shock Tests TST and Thermal Cycling Tests TCT through practical, direct current I_{ds} polarization, High-Temperature Storage Life HTSL) were executed. The advanced aging test suggested can obtain the temperature-ended zone through great time precision (rising and falling rate times a lesser amount of 3 seconds) and respectable thermal precision (a lesser amount of 10 °C). A set period contains the beginning at thermal environmental chamber temperature (T_{amb}), continuing to the cold level (T_{min}), so to the hot level (T_{max}), or else consecutively continuing to the hot level, to the cold, without interruption (figure 2). For HTSL, the temperature level packing is 750 °C for 700 hours inside the thermal room (SUN SYSTEM EC11). For the rest of the tests: TST, TCT and HTSL are examined in several situations (see Table 1) to create a clear decision from the comparison and expand the influence of

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diverse aging tests. The accelerated aging experiments were implemented through a PTFS system THERMONICS mode T-2820 (Precision Temperature Forcing System); the organism is considered for distress allowed thermal testing of electronic devices (Thermal Shock Tests TST and TCT: Thermal Cycling Tests). The tools are analysed through the control lines of IEEE-488 and directed via LabVIEW software. Five types of enhanced aging assessments (TST and TCT with or deprived of DC polarization; HVD: V_{ds} = 40 V, V_{gs} = 3.5 V, 15 h) were performed with various conditions. A cycle consists of beginning at thermal chamber temperature (T_{amb}), continuing to the cold level (T_{min}), or else consecutively continuing to the hot level, to the cold, minus disruption (Figure 2).

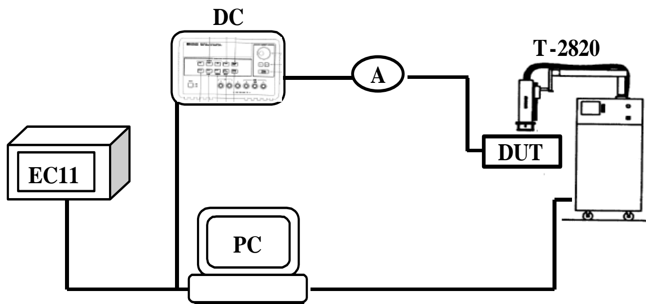


Fig. 1 Synoptic of thermal aging bench

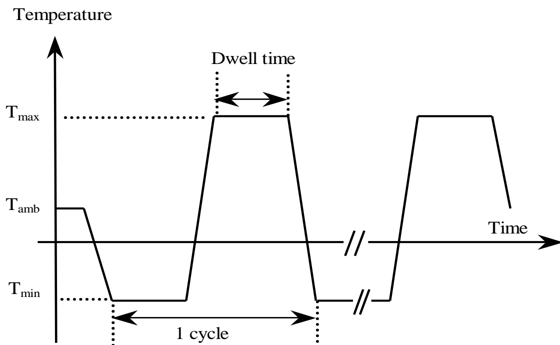


Fig. 2 Typical temperature profile

Table 1. Several aging tests situations through the equal phase quantity and dwell duration

Aging test	Thermal level
TST hot	T_{amb} / +75^{0}C
TST cold	T_{amb} / -75^{0}C
TST	-75^{0}C / +75^{0}C
TCT	-75^{0}C / +75^{0}C
HTSL	75^{0}C

3. Device Electrical Characterization and Parameters Extraction

This phase must relate aging tests to some prototypical behavior degradation or detect a failure phenomenon [4]. The significant experimental parameters of this component may be listed in this fashion: frequencies able to 2 GHz, 10 Watts is the output power, and 75 V presents the breakdown voltage that can be supported. Current Voltage I-V, Capacity Voltage C-V characteristic and S-parameters experimental parameters were completed through an Agilent E5270 Direct Current analyzer, HP technology 4194 impedance Analyzer also Network Analyzer E8362B from Agilent accompany, respectively, funneled by way of IC-CAP Agilent software. A correspondent model of an original electro-thermal circuit of RF power MOSFET components is presented in figure 3. It was executed in Agilent's accompanied by Advanced Design System ADS via the SDD (Symbolic Defined Device), providing an extra correct and supple model [3]. To measure the experimental parameter change, which looks at aging stress afterward, a novel advance electro-thermal model has been designed to RF power LDMOS components using a reliability tool [3,4]. Evaluations between measurements and numerical data for Current -Voltage experimental behavior are exposed in Figures 4 (Crss, Cos) and 5.

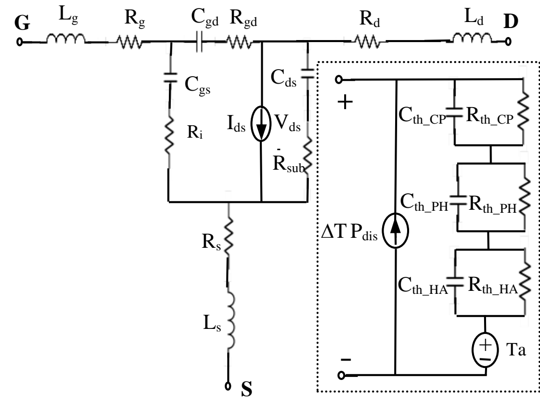


Fig. 3 Advance equivalent model of the RF power MOSFET transistor through a thermal circuit counting 3 RC cells

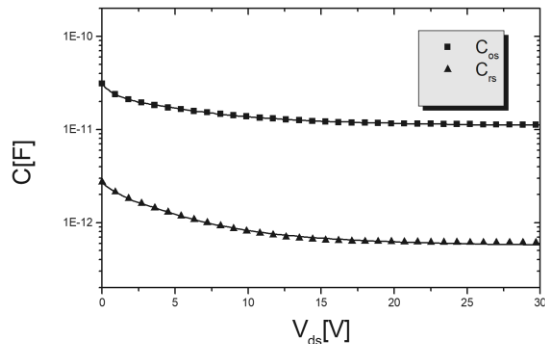


Fig. 4 C_{os}, C_{rrs} capacities experimental (dashed) and modelled (line form), per Frequency = 1MHz

For individually ageing test situations, ten tested device samples have been used to confirm the reproducibility of the measurement results (fault level less than 2%).

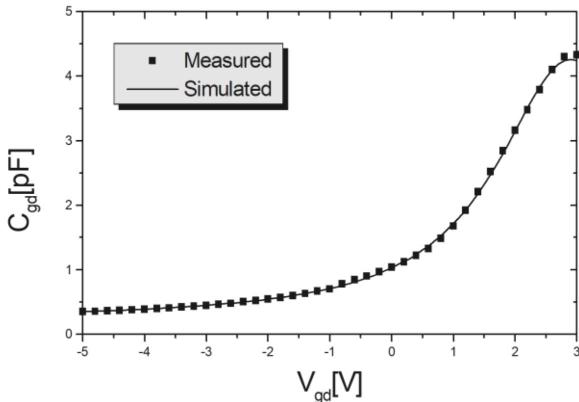


Fig. 5 Measured and simulated C_{dg} capacitance, using Frequency = 1MHz

4. Discussion and Analysis of the Degradation Phenomenon

The initial outcomes attained significant degradation of critical experimental behavior (75°C-700 hours for the HTSL test, ten cycles dwell-duration 10 min for TST and TCT tests). According to the producers' data, the degradation principles must be verified and founded on the characteristics of value shifts. The fundamental capacitances: C_{os} output drain-source, C_{gs} gate-source and drain-source C_{ds} are accessible, respectively, in Figure 6. These results show that the C-V characteristic (Cos, Cgs) have almost not changed after different accelerated tests. The C_{gd} capacitance gate-drain variation under the aging test is offered in figure 7.

For example, at zero polarization gate-drain, the variation is 2.56 pF in the cold TST test; nevertheless, it is 2.62 pF in the hot TST test. Table 2 shows the Miller capacitance C_{rss} failure through different aging tests. The attained outcomes present that this failure at TST and TCT tests are around equivalent, signifying a related failure phenomenon for the two aging accelerated tests. The C_{rrs} at zero drain-source bias is diminished from 2.72 pf toward 2.50 pf at the TCT test, signifying a variation of 8%. At 28 V polarization, the C_{rrs} diminishes from 0.609 pf toward 0.510 pf (change via 16 %). In Table 2, we observe the obtained values deviations of the various aging tests. Therefore, the putative failure phenomena lay in the hot carrier-generated boundary statuses and stuck electron charge, resulting in a buildup of negative charge at the Si-interface [6,7]. The position of this charge is probable to be at the area of the impact ionization intersection through the Si-interface [8,9]. The experimentally detected degradation source may well correlate to the existence of a max electric field that raises the carrier injection obsessed by the developed thermal SiO_2 (silicon dioxide layer) and at state boundary Si/SiO_2 [10,11,12]. An aspect of lateral electric field circulation for RF power MOSFET component of dynamic silicon film inside channel and drift zones is given away in Fig. 9-a, single utilizing a numerical simulation 2D (software Silvaco-Atlas). This important electric field foundations the peer group of charge conditions at the silicon-oxide border [13,14]. In the meantime, the component is tested in these situations; anywhere the drain electrode is predisposed by great bias (breakdown bias) concurrently through thermal phenomena exciting because the shock and cycling (variety tranquil the current line flow) of thermal aspect level, explained the relationship between the electrical phenomena and thermal aspect. The hot carriers' failure influence is strictly correlated to the current density. Through the full quantity of allowed electrons in the silicon-oxide border, anywhere maximum of the electrons are focused profoundly privileged the drift zone [7,15,16]. The outcomes are demonstrated by numerical Silvaco-Atlas (Fig. 9 a-b-c). Therefore, The V_{DS} drain-source potential raises the electric field rate at the drift zone, close to the oxide film, and then the thermal aspect increases, improving the hatching procedure. Accordingly, the failure level is augmented [9,17,18]. Test TCT and TST appear to be the same due to the speciously generated similar failure phenomena. The cold TST aging seems to encourage nearer failure than the hot TST aging test. Test HTSL appears slower than the rest of accelerated aging through the environments (75 °C – 700 hours). Accelerated aging tests in development at complex thermal aspects (more than 75 °C) and extended duration (superior to 700 hours) must infect extra failure phenomenon. Consequently, this manuscript permits analyses of reliability evaluation based on advanced aging tests after different accelerated tests and an evaluation per supplementary research in the references; it makes the invisible appear.

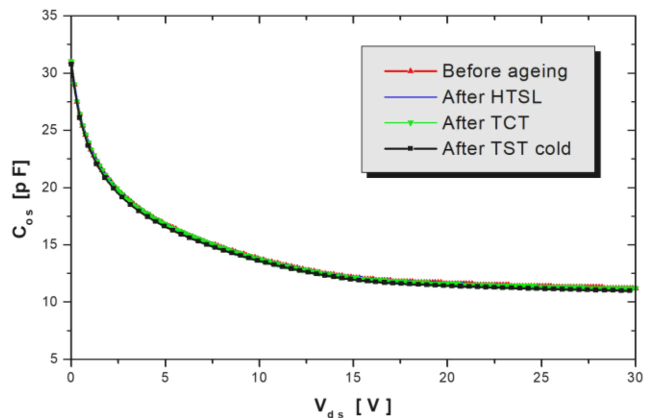


Fig. 6 Output capacitance Cos before and after aging, with Freq=1MHz

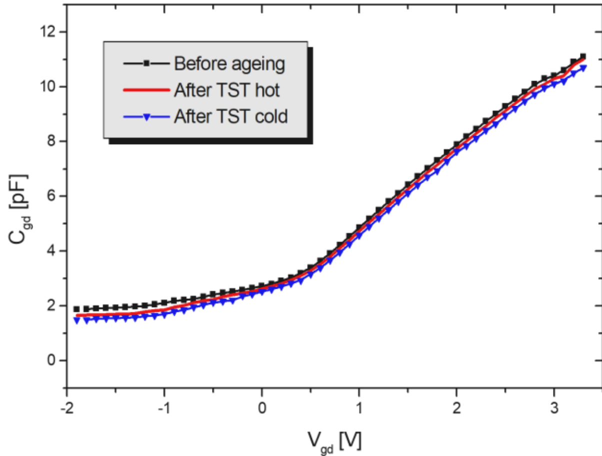


Fig. 7 C_{gd} variation through accelerated tests, Frequency equal 1MHz

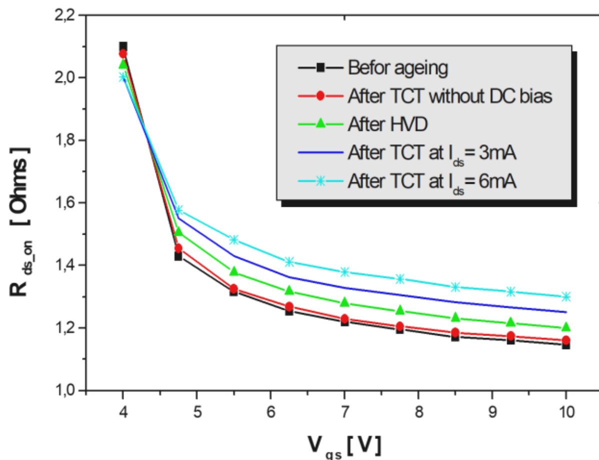


Fig. 8 R_{dson} variation under accelerated tests at different I_{ds} values, with V_{ds}=10mV

Table 2. Summary of the parameters values variations obtained after aging tests

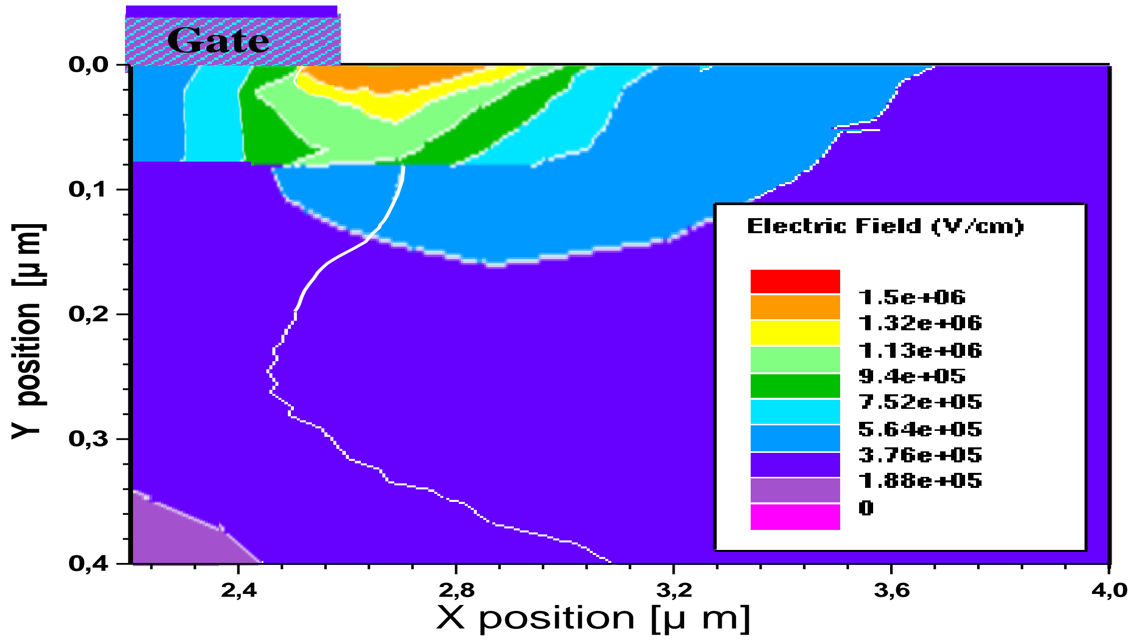
Parameter	Before aging	After aging				
		TST	TCT	TST hot	TST cold	HTSL
C_{rss}(pF) V_{ds}=0V	2.72	2.50	2.52	2.65	2.60	2.70
V_{ds}=28V	0.609	0.510	0.520	0.573	0.545	0.602
C_{os}(pF) V_{ds}=0V	31.10	30.94	30.96	31.07	31.05	31.10
V_{ds}=28V	11.33	11.27	11.24	11.31	11.30	11.33
C_{gd}(pF) V_{gd}=0V	2.72	2.48	2.49	2.62	2.56	2.71
C_{gs}(pF) V_{gs}=0V	21.51	21.50	21.50	21.48	21.46	21.51
C_{ds}(pF) V_{ds}=0V	28.89	28.87	28.86	28.87	28.87	28.88

After having presented the physical properties of the defects induced by the hot carriers injection, properties obtained by methods of defects characterization in the submicron MOSFETs (and more particularly, by a new approach using the technique of optical measurements), we will examine the conditions for creating faults as a function of the aging conditions [19,20]. The creation of defects will be correlated with the I-V degradations measured experimentally and by a 2D simulation in which we will consider these different defects. The defects parameters extracted from the measurements will be taken as input data for the Silvaco simulator [15,20,21]. The I-V characteristics thus simulated will be compared to the experimental I-V characteristics to have a self-consistent approach to the defects- electrical characteristics of the components.

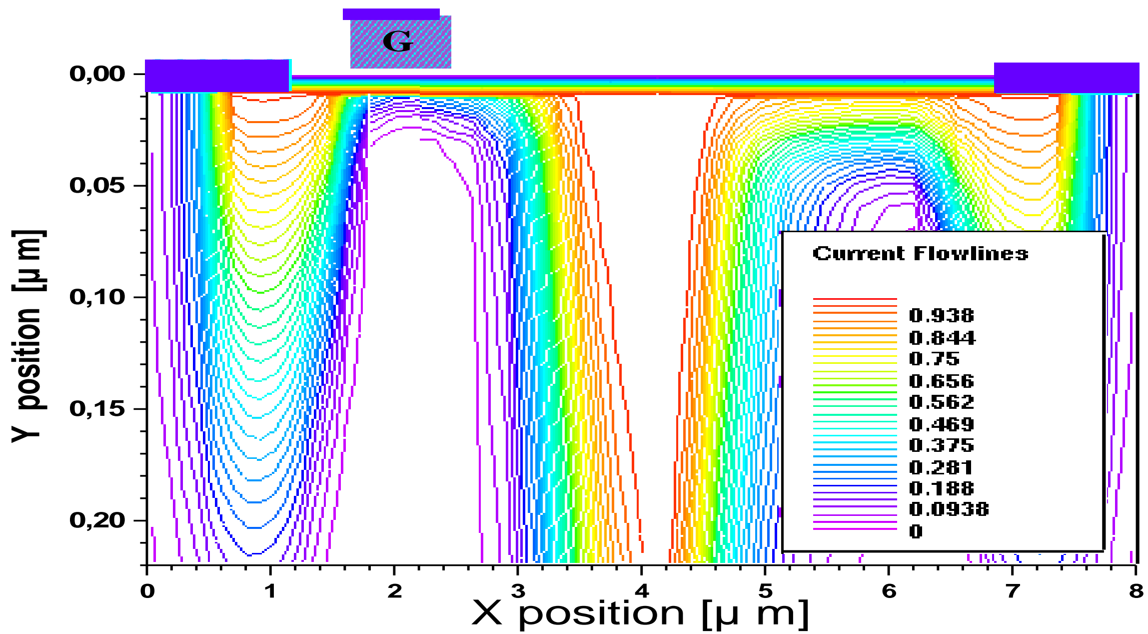
Positively charged, and the acceptors created are negatively charged. The results pant of the aging test and 2D simulations for the localization of the electrons injection points and the holes along the interface [21], the rough physical diagrams of the localization of the maximum electric fields and concentration of electrons. The two distributions likely overlap at the drain-channel junction. To analyze the behavior of the I-V characteristics. 2D simulations [3,4,13] and Monte Carlo simulations [3,13] have shown that the electron injection point moves towards the channel when V_{th} decreases. The amplitude of this displacement is more or less important, with values between 0.02 µm and 0.15 µm the injection point is located [5,15,17].

We used the simulator [9, 12], which allows us to account for localized distributions of the physical phenomena in the oxide and the interface [11, 14]. In the present case, the interface states and the donors in the oxide are modeled by a Gaussian distribution in the channel 0.07 µm from the drain. The acceptor oxide defects are modeled by a Gaussian above the drain, centered on the position of the maximum lateral field. This study shows that the acceptor-like defects localized above the drain in the gate-drain cap oxide are particularly important in explaining the degradation mechanisms of LDD MOSFET devices. It agrees with the work of Doyle et al. for non-LDD structures [13]. In the case of LDD structures, it is known that the phenomenon of electron trapping is relatively more important than in conventional structures [10,12]. Then, in the case of LDD structures, the oxide quality is essential concerning the creation phenomena of acceptor defects. A clear difference in behavior is observed in the I-V characteristics of the two devices [17]. Finally, we highlight very recent work confirming our conclusions on the creation of acceptor defects in the oxide. Measurements of C-V characteristic drifts between the gate and drain [18] and measurements of drain current induced by isolated defects in MOSFETs of very small geometries (0.35 µm x 0.5 µm) [19] have demonstrated the acceptor nature of the defects induced during the MOSFETs aging by hot carriers injections.

Our studies have essentially focused on the reliability evaluation of NLDMOS transistors based on advanced aging. Therefore, the physical properties characterization of the defects induced in the gate oxide by the hot carrier's injection. These defects had been less highlighted in previous studies, although their existence had been repeatedly suggested. It is due to their location above the drain in the overlap zone between the gate and drains.



(a)



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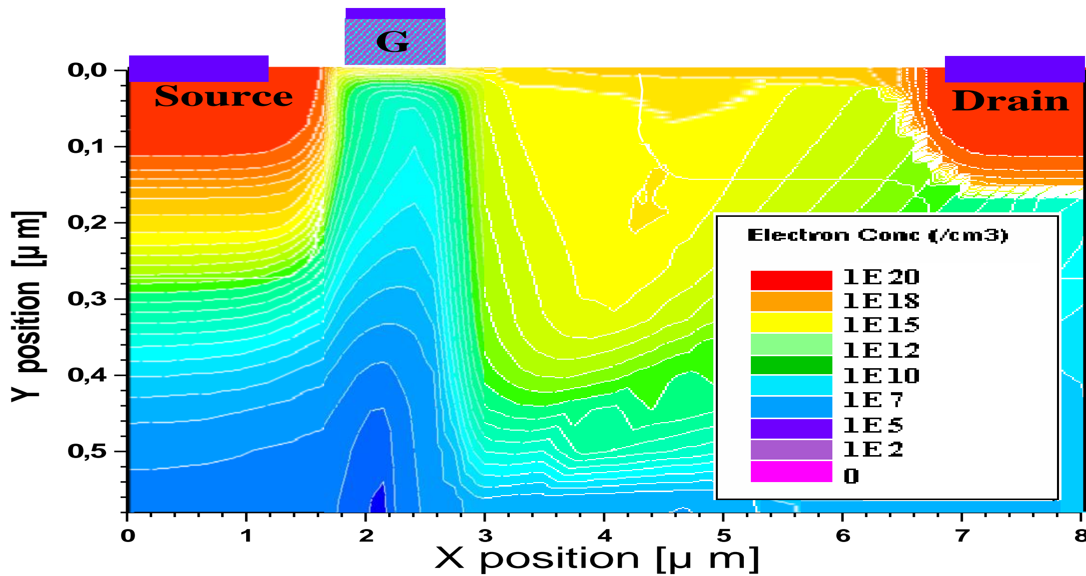

(c)

Fig. 9 Numeric Simulation of NLDMOS, per V_{ds} = 40V V_{gs} = 3.5V : (a) electric field contour, (b) drain current flow lines, (c) Electron concentration distribution

5. Conclusion

This manuscript organizes a substantial study designed to investigate the failure of the accelerated tests method of RF LDMOS devices. We enlightened the evolution liaison to the most significant electrical parameters and the degradation phenomena.

The outcomes got marked as a variation of critical electrical behavior as G_m, R_{ds_on}, C_{gd}, and C_{rss}. Therefore, the characteristic is delicate toward the electrons inoculated at the gate/SiO_2 boundary. Immediately, when the drain electrode is at a higher voltage bias, a max electric field acts that favors the hot carrier injection aspect. The ΔT (temperature difference) and Ids (quiescent current) influence the behaviour variation. The S-parameter failure is principal because of diminution in transconductance parameter, raising the capacitances Cgd and Crss, also rising at Lightly Doped Drain area (LDD) boundary positions. We have reported the link between the different aging tests and the effects of the hot carrier on the electrical performance in the NLDMOS device (current-voltage, capacity-voltage and RF). The device's progress of the significant characteristic permits estimating the component performance (lifetime without failure), making it possible to obtain a relationship between the variation of the electrical characteristic and the stress used. Afterwards, we can reduce the risk of electrons being trapped at the silicon oxide interface, decreasing the risk of device performance degradation and improving reliability.

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